PROCESS SPECIFICATION

SPECIAL CONDITIONING OF NOR GATES

(FLAT PACKS)

Record of Revisions

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This specification consists of pages 1 to 19 inclusive

APPROVALS	NASA/MSC		MIT/IL	

PROCESS SPECIFICATION
SPECIAL CONDITIONING OF NOR GATES
(Flat Packs)

1. SCOPE

1.1 PURPOSE

This specification establishes the minimum requirements for the acceptance of integrated circuit Nor gates and Nor gate expanders for use in flyable deliverable end items. The procedures described herein shall be performed by the G&N Industrial Contractor as part of incoming inspection, screen, and burn-in.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES

The following documents of the issue in effect on the date of this document form a part of this specification to the extent specified herein.

SPECIFICATIONS

Military

MIL-STD-750	Test methods for semiconductor devices

Apollo G&N

ND1002358	Leak test procedures for nor gates.
ND1002257	Internal visual rejection criteria for integrated circuits.

DRAWINGS

Apollo G&N

1006321	Specification control drawing for dual nor gate (flat packs).
1006394	Specification Control Drawing for Dual Nor Gate Expander (Flat Pack).

REPORTS

MIT/IL E-1679	Progress Report on Attainable Reliability of Integrated Circuits for System Application.

3. REQUIREMENTS

3.1 GENERAL

The provisions of this specification shall be applicable to all phases of acceptance of integrated nor gates and Nor gate expaders to the extent specified herein. Specific requirements or provisions not covered by this specification shall be as specified on the applicable drawing or purchase order. In the event of conflict between the requirements of the applicable drawings, this specification and other documents cited herein, the requirements of the applicable drawings and this specification shall govern in that order.

3.2 PROCESS CONTROL

The process covered by this specification shall be controlled in accordance with the process control provisions of 4.2.

3.2.1 Lot Control

Each lot (6.2.1) of up to 5000 units as supplied by the vendor in compliance with 1006321 or 1006394 shall be identified and maintained by the contractor throughout the test sequence, 3.3.1.

3.2.2 Serialization

All units of a lot shall be serialized by the G & N contractor. A unit shall be identified by the lot number and the umit serial number.

3.3 TEST PROCEDURES

3.3 1 Test Sequence

Each lot of Nor gates or Nor gate expanders shall be subjected to tests in the following sequence:

a. External visual inspection (Test #1).

b. Physical dimension, lead tension, and fatigue inspection (Test #2).

c. Electrical test (test #3).

d. Thermal cycle test (test #4).

e. High temperature bake test (test #5).

f. Centrifuge Y_1 test (test #6).

g. Continuity open and short test (test #7).

h. Centrifuge Y_2 test (test #8).

i. Electrical test (test #9).

j. Propagation delay (test #10).

k. Emitter base back bias (test #11).

l. DC Current Gain Measurement (Test #12).

m. Helium Leak test (Test #13).

n. Gross Leak Test (Test #14).

o. Operation life test (test #15).

p. Electrical test (Test #16).

q. Vibration test (test #17).

r. Shock test (test #18).

s. Continuity test (test #19).

t. Internal visual inspection (test #20).

A flow diagram of the above sequence is attached.

3.3.1.1 Removal of Failures

Catastrophic failures only shall be removed from the test sequence at the point of detection and subjected to failure analysis. The point in the test sequence 3.3.1 where the failure was detected must be recorded and a set of electrical reading as specified in paragraph 3.3.2.3 shall be performed. All electrical failures at the end of the test sequence 3.3.1 shall be subjected to failure analysis except the failures as defined in 6.2.3 (a), (b), & (d) may be returned to the vendor;

3.3.2 Tests

3.3.2.1 External Visual Inspection (Test #1)

Each lot of Nor gates shall be subjected to an external visual inspection in accordance with MIL-STD-750, method 2071 and the applicable Specification Control Drawing 1006321 or 1006394 with additional requirements to be negotiated with the vendor, and to be included in the purchase order.

3.3.2.2 Physical Dimension, Lead Tension, & Fatigue (Test #2)

A sample of 10 Nor gates shall be subjected to the physical dimension examination of MIL-STD-750, method 2066 and the applicable Specification Control Drawing 1006321 or 1006394. Five of the 10 units shall be subjected to the lead tension and lead fatigue tests. Test #2, as specified below. The five units subjected to the lead tension and lead fatigue tests are to be forwarded to test 20 of the test sequence 3.3.1. The remaining 5 units shall be forwarded to test 3 of the test sequence 3.3.1.

(a) Lead Fatigue. Leads shall be capable of withstanding the following test: The unit shall be held in a vertical position with a 2 ounce weight suspended from the lead to be tested. Two cycles of bending shall be performed. A cycle consisting of moving the body of the unit, 45 degrees from the vertical in one direction, and back 45 degrees to the original position. No mechanical damage shall be evidenced after the test.

(b) Lead Tension. Each lead shall be capable of withstanding an axial pull of 1 pound for a period of 30 seconds. No mechanical damage shall be evidenced after the test.

3.3.2.3 Electrical Test (Test #3 of 3.3.1)

a. The entire lot of Nor gates shall be subjected to electrical test as described in Specification Control Drawing 1006321 with the limits as specified. The test is to be performed on all base currents, I_B: all output voltages V_Q; both output currents I_O; both collector-emitter threshold currents I_{CEX}; and both collector-emitter sustaining voltages, V_{CEO} sust. D.C. current gain, h_{FE}, shall be measured on only one transistor of each gate and R_L shall be measured on one gate only.

b. The entire lot of Nor gate expanders shall be subjected to electrical test as described in the Specification Control Drawing 1006394. The test is to be performed on all base currents, I_{B2} with a 4.15 k ± 1% resistor from pin 1 or 9 to + 4 ± 0.1V; all output voltages, V_O; both collector-emitter threshold currents I_{CEX} and both collector-emitter sustaining voltages, V_{CEO} sust. D.C. current gain, h_{FE}, shall be measured on only one transistor of each gate expander and Z_L shall be measured on one gate only.

3.3.2.4 Electrical Test (Test #9 and #16 of 3.3.1)

The electrical test shall be the same as performed for 3.3.2.3 except that the maximum limits as defined in the applicable Specification Control Drawing 1006321 or 1006394 shall be raised 4%, the minimum limit decreased 4%, and the V_{CEO} sust. test will not be performed.

3.3.2.5 Thermal Cycle Test (Test #4)

The units shall be subjected to thermal cycle consisting of 3 cycles of the following: The units shall be stabilized for 30 minutes minimum at +150°C ± 5°C in an oven. They shall then be transferred to an oven operating at -65 ± 5°C in less than 10 seconds. The units shall stabilize for not less than 30 minutes and then be returned to the +150 ± 5°C oven in less than 10 seconds transfer time.

3.3.2.6 Helium Leak Test (Test #13)

The helium leak test shall be performed in accordance with ND 1002358 using a rate of 5×10^{-8} cc/atm/sec. as the upper limit.

3.3.2.7 Gross Leak Test (Test #14)

The Nitrogen Bomb Test [redacted] and Gross Leak Test [redacted] shall be performed in accordance with ND 1002358 (Para. 3.7 and 3.8). The Nitrogen bomb test shall be performed first.

3.3.2.8 High Temperature Bake Test (Test #5)

The high temperature bake test shall be performed in accordance with MIL-STD-750, method 1031, except the temperature shall be 150 ± 5°C and the time shall be 168 ± 8 hours.

3.3.2.9 Centrifuge Y_1 Test (Test #6)

The centrifuge Y_1 test shall be performed with an acceleration of 20,000g in accordance with MIL-STD-750, method 2006. Plane Y_1 is defined as a force attempting to push the internal lead wires toward the bottom of the device.

3.3.2.10 Continuity Open and Short Test (Test #7)

The continuity test shall be performed to detect open bonds and shorts between leads, leads and case, and leads and chip. At test #9 check 100%, at test #19 check 77 units from test #18.

3.3.2.11 Centrifuge Y_2 Test (Test #8)

The centrifuge Y_2 axis test shall be performed with an acceleration of 20,000g in accordance with MIL-STD-750, method 2006. Plane Y_2 is a force opposite to Y_1 as defined in paragraph 3.3.2.9.

3.3.2.12 Propagation Delay (Test #10)

Propagation delay shall be performed according to the applicable Specification Control Drawing 1006321 or 1006394 on a sample of 200 units * from each lot.

3.3.2.13 Emitter Base Back Bias Test (Test #11)

The emitter base back bias test shall be performed on 200 units * as follows. Each base input shall be connected to minus 6 volts with respect to common emitter via a 10K series resistor in each base. The units shall be operated with voltage applied at a temperature of 25°C ± 5°C for a period of 72 hours.

3.3.2.14 Beta Measurement (Test #12)

The D.C. current gain measurement shall be performed in accordance with the applicable Specification Control Drawing 1006321 or 1006394 on the same transistors as measured at 3.3.2.4.

3.3.2.15 Operation Life Test (Test #15)

a. Dual Nor Gate, SCD 1006321

An odd number of units (Gates) shall be connected in series with the output of the last unit supplying the input to the first unit, thus forming a "Ring" oscillator with 8 VDC ± 5% applied continuously to the power terminal of all units in the circuit (Fig. 3 of SCD 1006321). "Ring" oscillation must occur at the initiation of the test. This test shall be performed on all units for a period of 168 hours ± 8 hours. The ambient temperature shall be maintained at 25 ± 10°C.

b. Dual Nor Gate Expander, SCD 1006394

An odd number of units (Gate expanders) shall be connected in series with the output of the last unit supplying the input to the first unit, thus forming a "Ring" oscillator with 8 VDC ± 5% applied continuously to the output terminal of all units in the circuit via a 2.7 k resistor (Fig. 3 of SCD 1006394). Ring oscillation must occur at the initiation of the test. This test shall be performed on all units for a period of 168 hours ± 8 hours. The ambient temperature shall be maintained at 25 ± 10°C.

* When samples are selected for tests #10, #11, & 17, the samples shall be representative of all diffusion sub-lots in the shipment lot.

3.3.2.16 Vibration Test (Test #17)

The vibration test shall be performed on random sample of 77 units.* The vibration test shall be performed in accordance with MIL-STD-750, Method 2056, 30g's from 5 to 2000 cps limited to 0.12 inch double amplitude, 3 cycles, 15 minutes per cycle minimum.

3.3.2.17 Shock Test (Test #18)

The shock test shall be performed on the same units tested in 3.3.2.16. The shock test shall be performed in accordance with MIL-STD-750, Method 2016, 1500 g's, 0.5 m sec 5 blows in all axis directions, 30 blows total.

3.3.2.18 Internal Visual Inspection (Test #20)

The internal visual inspection shall be performed on the 82 units from test 3.3.2.17 and 3.3.2.3 and in accordance with ND 1002257.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL

In order to assure proper control of the acceptance process covered by this specification, the contractor shall meet all the requirements specified herein and shall provide continuous audit of the acceptance process to assure compliance with the requirements of this specification.

4.1.1 Inspection

The contractor, through his quality assurance or control agency shall be responsible for the performance of all inspection requirements and tests specified herein.

4.2 FAILURE CRITERIA

4 2.1 Failure Analysis

All Nor gates or Nor gate expancers failing in the electrical tests specified in 3.3.2 (test #3, 7, 9, 12, and 16) except the non-catastrophic failures as defined in 6.2.3 (a,b, & d), shall be subjected to a failure analysis sufficient to identify cause and mode of failure. For failure definitions refer to Section 6.2.

* When samples are selected for tests #10, #11, & 17, the samples shall be representative of all diffusion sub-lots in the shipment lot.

4.2.2 Failure Modes

After failure analysis all failures detected at test 3,7,9 and 16 of test sequence 3.3.1, except induced failures and non-catastrophic failures as defined in 6.2.3 (a,b, & d), shall be classified as to the following failure modes which are described in MIT/IL report E-1679.

a. Class A failure modes (class A failure modes are generally of a type readily weeded out during screen and burn-in).

1. Open bonds due to poor metalization adhesion to the silicon dioxide.
2. Open bonds due to underbonding.
3. Open bonds due to gold-aluminum eutectic formation.
4. Open bonds due to overbonding.
5. Opens due to nicks and cuts in the bonding wire.
6. Leads shorting to the edge of the chip or leads shorting to the package lid.
7. Open interconnects detected only during test 3.3.2.3 due to only scratches with no evidence of metalization corrosion at the open.
8. Shorts due to metalization scratching and smearing.
9. Shorts induced by the collector to emitter sustaining voltage test of paragraph 3.3.2.3.
10. Failures due to cracked chip.
11. Opens due to the thinning of lead wire due to poor bonding procedure.
12. Non-catastrohpic failures due to surface instabilities that are not included in 6.2.3 (a and c).

4.2.2 Failure Modes (Cont'd)

b. Class B failure modes (Class B failure modes are of a type less readily detected during screen and burn-in as compared with Class A).

1. Shorts resulting from leads touching any other leads and shorts resulting from leads touching metal interconnects.

2. Opens in the interconnect due to the gold-aluminum eutectic formation at the neck of an interconnect.

3. Shorts through the silicon dioxide due to poor oxide dielectric strength.

4. Shorts through the oxide because the bonds are too close to the chip edge.

5. Shorts, intermittent or otherwise, due to particles in the package.

6. Shorts, intermittent or otherwise, due to free lead material and fixed extra leads or lead material.

7. Catastrophic failures due to surface instabilities.

8. Opens in interconnect at oxide steps detected during test 3.3.2.3.

c. Class C failure modes (Class C failure modes are of a type which are time dependent and/or are not easily detected during screen and burn-in).

1. Opens in the interconnect due to corrosion.

2. Opens in the interconnect detected after test 3.3.2.3 at oxide steps.

3. Opens in the interconnect detected after test 3.3.2.3 at scratches.

4. Any failures due to electrically insulating or electrically high resistance layers forming at the silicon oxide window between the metal contact and the silicon or between the layers of metal.

5. Die separated from package header.

4.2.3 Failure Mode Grouping

4.2.3.1 Classification

Following the classification of failure modes from a lot the electrical failures will be divided into Group I - IV below and the percentage failure for the lot in each group shall be determined. Group O contains special cases of non-catastrophic failures.

a. Group 0. Test 3 and 10

Non-catastrophic failures as defined in 6.2.3 (a) and propagation delay failure of Test 10.

Group 0 Test 9 and 16

Non-catastrophic failures as defined in 6.2.3(b)

b. Group I Class A failure Modes.

c. Group II Class B Failure modes.

d. Group III — Class C failure modes.

e. Group IV — Any failure, except induced failures, not listed in Section 4.3.2 or any failure for an unknown cause.

TABLE I

Test Number (See Para.3.3.1)	*Maximum Percent of Failures				
	Group 0	Group I	Group II	Group III	Group IV
3	0.5%	0.3%	0.08%	0.04%	0%
7,9,and 16	0.5%	0.3%	0.04%	0.02%	0%

*For shipment lots of from 4000 to 5000 units, use the same number of allowable failures as applied to lots of 5000. For smaller lots, use percentages as shown in Table I. If the number of unit failures allowable is calculated to be a mixed number, a combination of an integer and a fraction, use the integer only.

TABLE II

Test Number (See Paragraph 3.3.1	Maximum Percent of Failures or Maximum Allowable rejects
2	1 defective unit, Physical Dimensions
2	1 defective unit, Lead fatigue and tension
12	10 Units
19	1 unit
20	8 units

4.3 REJECTION CRITERIA

4.3.1 Lot Rejection

The failures of a lot shall be classified as specified in 4.2.2 such that the failures can be identified with the groupings specified in 4.2.3. The maximum allowable percentages of failures from test number 3,7,9 and 16 of paragraph 3.3.1 according to the failure mode groupings of 4.2.3 are given in Table I. The maximum allowable percentages of failures from test numbers 2,12, ,19 and 20 of paragraph 3.3.1 are given in Table II where the failure definitions are given in 6.2. Failure to meet any one of the maximum allowable percentages of Tables I and II or failure to comply with the test sequence of 3.3.1, the test procedure 3.3.2, the flight qualification requirements of 4.4, or the data requirements of 4.5 shall be cause for lot rejection.

4.3.1.1 Conformance to ND 1015404

Disclosure of any violation of previously agreed to Contractor-Supplier ND 1015404 "Critical Process" list without prior notification automatically fails the entire lot. Notice of such deviation must be made by the contractor to MIT/IL within 24 hours of disclosure.

4.3.2 Sub-lot Removal

If the reason for shipment lot rejection can be assigned to failure modes which are traceable to a diffusion sub-lot(s), the entire diffusion sub-lot(s) shall be removed from the shipment lot and the provisions of paragraph 4.3.1 shall be reapplied to the remainder of the shipment lot. For example, failure modes which are traceable to diffusion sub-lot(s) are described in paragraph 4.2.2 sub-paragraphs, a1, b3, b8, c2, and c4.

4.4 FLIGHT QUALIFICATION

A Nor gate or Nor gate expander is flight qualified when the lot, of which the Nor gate or Nor gate expander is part, is not rejected according to 4.3 and the Nor gate or Nor gate expander does not fail and test of the sequence of Paragraph 3.3.1.

4.4.1.1 Failure Traceability

Any Nor gate or Nor gate expander failure detected in qualified flight hardware must be traceable to a lot as identified in paragraph 3.2.1.

4.4.2 Qualification Report

Two copies of a report justifying the acceptance or rejection of a lot as flight qualified shall be forwarded to MIT/IL prior to use in deliverable end items.

4.4.2 Qualification Report (Cont'd)

The report shall include the following:

a. A summary of screen and burn-in data.

b. A detailed list of the screen and burn-in results which includes the number of failures at each test station of test sequence 3.3.1.

c. A failure report of all electrical failures, by unit serial number including induced failures as specified in 4.3.1 which includes:

   1. Photographs of each category of each photographable failure. A minimum of two photographs for each category is required where more than one exists.

   2. Analysis of each failure.

   3. Classification of each failure according to 4.3.2.

   4. All electrical test data of each failure.

d. Number of failures in the failure mode groups according to 4.2.3.

e. Date of purchase.

f. Total number of ordered parts.

g. Date code of parts received.

h. Lot identification number.

i. Allocation of all parts from the lot updated to the date of issue of qualification report indicating the number of units which passed screen and burn-in, the number of failed units, the number of induced failures and the number of units removed from the lot for any other reason.

j. Vendor supplied Table I and Table II, sub group 1 and 3 test data.

k. A report by lot of all internal visual inspection failures (test #20 in test sequence 3.3.1) by unit serial number which includes.

   1. Photograph of each failure category detected.

   2. Classification of each failure according to ND 1002257.

l. A list of all process changes allowed by the contractor in accordance with 1015404, paragraph 3.3.2.2.

m. Report of Leak Test audit results including justification for acceptance or rejection.

4.5 DATA

4.5.1 DATA STORAGE

Incoming inspection, screen, and burn-in data shall be maintained and stored by lot number and unit serial number for three years.

4.5.2 Cataloging

Not gates or Nor gate expanders failing the tests specified herein with the exception of the external visual inspection and leak tests shall be cataloged and stored by lot number and serial number for three years. The devices must be readily accessible for future reference.

5. PREPARATION FOR DELIVERY

This section is not applicable to this specification.

6. NOTES

6.1 INTENDED USE

This process conditions nor gates used in Apollo Guidance and Navigation Equipment.

6.2 DEFINITIONS

6.2.1 Lot

A shipment lot is defined as a group of Nor gates or Nor gate expanders submitted by a vendor in compliance with SCD 1006321 or SCD 1006394.

6.2.2 Catastrophic Failures

A catastrophic failure is defined as any device which fails the electrical tests of Table II of the applicable Specification control Drawing 1006321 or 1006394 by twice the maximum or one half the minimum limits of that table.

6.2.3 Non-Catastrophic Failures

A non-catastrophic failure is any device which cannot be classed as a catastrophic failure by definition 6.2.2 but which fails according to the definitions described below:

(a) SCD 1006321 or 1006394

A non-catastrophic failure at test 3.3.2.3 exceeds the limits of Table II of the applicable Specification Control Drawing 1006321 or 1006324 and does not become a catastrophic failure during test sequence 3.3.1.

(b) A non-catastrophic failure at 3.3.2.4 exceeds the limits in 3.3.2.4 but does not change in parametric value from 3.3.2.3 by more than ± 15% for base current (I_b) or output voltage (V_0), ± 10% for output current (I_0 when applicable) and ± 20% for collector to emitter threshold current. A unit which shows a collector to emitter threshold current of less than 1 μ amp shall be assumed to have a leakage current of 1 μ amp for drift failure determination.

(c) A non-catastrophic failure at 3.3.2.4 exceeds the limits in 3.3.2.4 and changes in parametric value from 3.3.2.3 by more than ± 15% for base current (I_b) or output voltage (V_0), ± 10% for output current (I_0) when applicable) and ± 20% for collector to emitter threshold current. A unit which shows a collector to emitter threshold current of less than 1 μ amp shall be assumed to have a leakage current of 1 μ amp for drift failure determination.

(d) SCD 1006321 or 1006394

A non-catastrophic failure at test 3.3.2.14 exceeds a change in D.C. current gain by ± 20% in test sequence 3.3.1 test number 9 and test number 12.
NOTE: The ± 20% includes the 4% raised max. limits and 4% decreased min. limits specified in test #9.

6.2.4 Induced Failures

An induced failure is a failure which through failure analysis can be proven to be caused by exceeding the stress limits of the applicable Specification Control Drawing 1006321 or 1006394.

6.2.5 Leak Test Failures

A failure at test 13 of paragraph 3.3.1 is failure to meet the leak rate therein. A failure at test 14 of paragraph 3.3.1 is the failure to meet the criteria as specified in ND 1002358..

6.2.6 External Visual Inspection Failures

A failure at test 1 of paragraph 3.3.1 is failure to meet the visual and mechanical examination criteria of the applicable Specification Control Drawing 1006321 or 1006394 and additional requirements negotiated with the applicable vendor.

6.2.7 Physical Dimension Failures

A physical dimension failure of test 2 of paragraph 3.3.1 is a package which does not meet the physical dimension criteria of the applicable Specification Control Drawing 1006321 or 1006394.

6.2.8 Lead Tension, Lead Fatigue Failures

The lead tension, lead fatigue failures of test 2 of paragraph 3.3.1 is a partial or complete severing of a lead from the package.

6.2.9 Propagation Delay Failures

A failure at test 10 of paragraph 3.3.1 is a failure to meet the criteria of the applicable Specification Control Drawing 1006321 or 1006394.

6.2.10 Failures

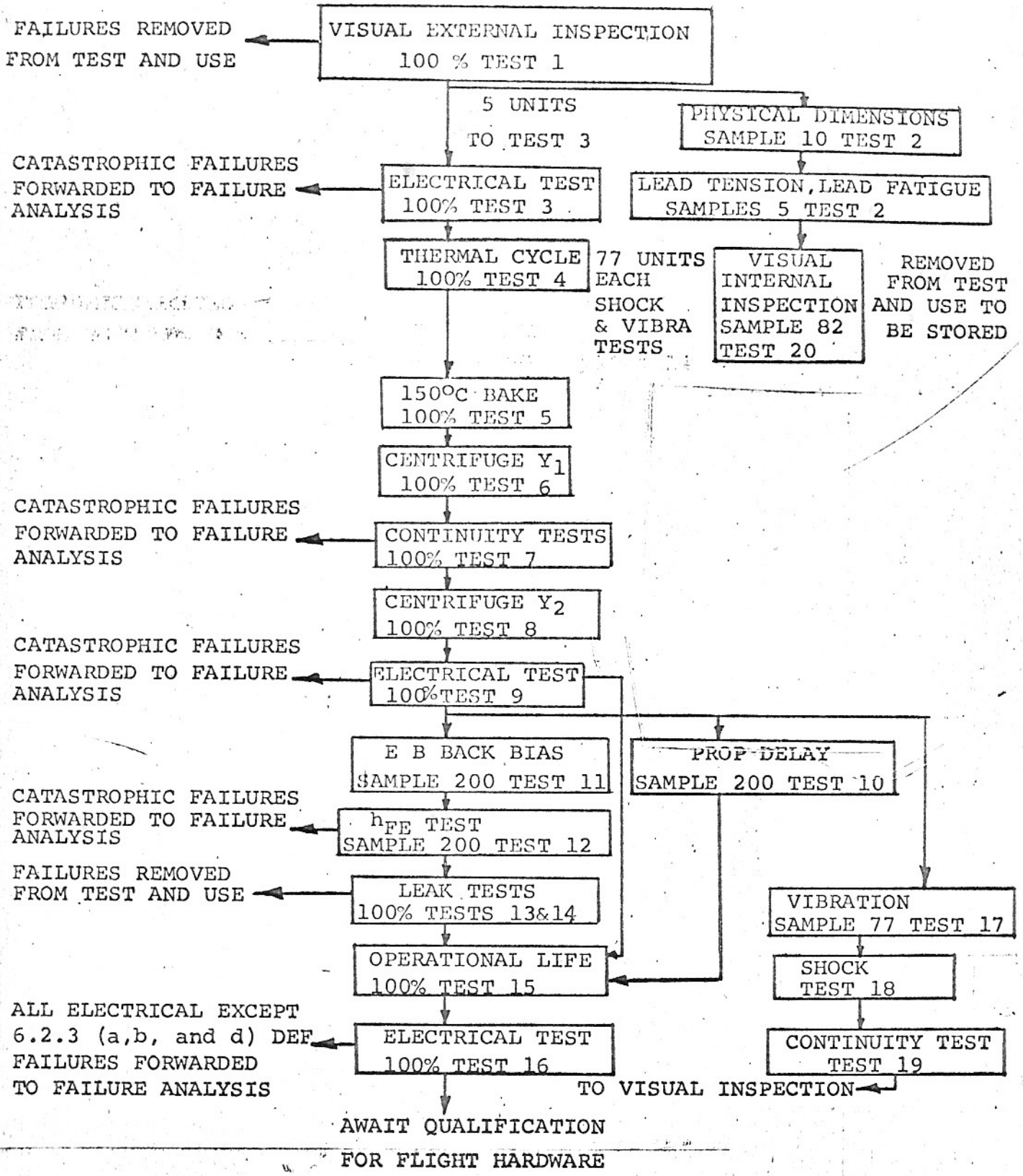
Failure of a unit in one or more tests will be charged as a single failure. A unit which could be classed by several failure modes shall be classed in the highest alphabetical mode as listed in 4.2.2. A unit which meets the definition of 6.2.3 (a) and does not change in parametric value more than the amount specified in paragraph 6.2.3 (c) shall be counted in Group 0 only.

6.2.11 Internal Visual Inspection Failures

A Failure at test #20 of paragraph 3.3.1 is a failure to meet the criteria of ND 1002257.

6.2.12 Continuity Failure

A failure of the continuity test is the detection of an open or a short.



FLOW DIAGRAM FOR THE TEST SEQUENCE 3.3.1