METHOD 3024

SIMULTANEOUS SWITCHING NOISE MEASUREMENTS
FOR DIGITAL MICROELECTRONIC DEVICES

1. Purpose. This method establishes the procedure for measuring the ground bounce (and V_{CC} bounce) noise in digital microelectronic devices or to determine compliance with specified ground bounce noise requirements in the applicable acquisition document. It is also intended to provide assurance of interchangeability of devices and to eliminate misunderstanding between manufacturers and users on ground bounce noise test procedures and requirements. This procedure is not intended to predict the amount of noise generated on an end product board, but for use in measuring ground bounce noise using a standardized method for comparing noise levels between logic families and vendors.

1.1 Definitions. The following definitions shall apply for the purposes of this test method:

a. Ground bounce noise. The voltage amplitude (peak) of extraneous signals present on a low-level non-switching output with a specified number of other outputs switching. Ground bounce noise on a logic low output can be of sufficient amplitude to exceed the high level threshold of a receiver, or cause latch-up on unprotected CMOS inputs.

b. V_{CC} bounce noise. The voltage amplitude (peak) of extraneous signals present on a high-level non-switching output with a specified number of other outputs switching. V_{CC} bounce on a logic high output can be of sufficient amplitude to exceed the low level threshold of a receiver, or cause latch-up on unprotected CMOS inputs.

c. Simultaneous switching noise. Noise generated across the inductance of a package pin as a result of the charge and discharge of load capacitance through two or more transitioning output pins.

d. Quiet low. A non-switching output which is driving a nominal low level.

e. Quiet high. AQ non-switching output which is driving a nominal high level.

f. Signal skew. The amount of time measured between any two signal transitions at the 1.5 V voltage level (for TTL threshold devices) and at $V_{CC}/2$ (for CMOS threshold devices).

1.2 Symbols. The following symbols shall apply for the purposes of this test method:

1.2.1 Logic levels.

V_{IL} max: The maximum allowed input low level on a digital microelectronic device.

V_{IL} min: The minimum allowed input low level on a digital microelectronic device.

V_{IH} max: The maximum allowed input high level on a digital microelectronic device.

V_{IH} min: The minimum allowed input high level on a digital microelectronic device.

1.2.2 Noise levels.

V_{OLP} max: The largest positive amplitude transient allowed on a logic low output.

V_{OLV} max: The largest negative amplitude transient allowed on a logic low output.

V_{OHP} max: The largest positive amplitude transient allowed on a logic high output.

V_{OHV} max: The largest negative amplitude transient allowed on a logic high output.

1.2.3 Transition times.

T_{TLH}: The transition time of a rising edge (rise time) measured from 10 percent to 90 percent.

T_{THL}: The transition time of a rising edge (fall time) measured from 90 percent to 10 percent.

2. Apparatus. The apparatus used for ground bounce noise measurements shall include a suitable source generator (see 2.1), loads (see 2.2), an oscilloscope (see 2.3) and a low noise test fixture (see 2.4). See figure 3024-1 for proper connections.

2.1 Source generator. The pulse or pattern generator for this test shall be capable of supplying the required input pulses with transition times of 3.0 ±0.5 ns to minimize skew due to input threshold differences.

2.2 Loads. Loads shall consist of 50 pF capacitance (-0,+20%) and a 500 ohm (±1%) low inductance resistor from each output to ground. Capacitance value should include probe and test fixture capacitance. The 500 ohm resistor may be made up of a 450 ohm resistor in series with a 50 ohm oscilloscope input channel or 50 ohm termination.

2.3 Oscilloscope. The oscilloscope and probe combination shall have a minimum bandwidth of 1 GHz. Probes (if used) must be calibrated using the manufacturers instructions before accurate measurements can be made.

2.4 Test fixture. Test fixture construction has a large impact on the accuracy of the results. Therefore, the standard ESH test fixture or an equivalent approved fixture (one which demonstrates results within 10% of the standard) must be used to perform these tests. (The ESH fixture for DIP devices is LAB-350-28. Other standard fixtures will be determined at a later date.) Lead lengths should be 0.25 inches or less. The devices under test may be clamped to the test fixture, soldered to the fixture, or installed in a socket on the fixture. Use of a socket may result in higher readings.

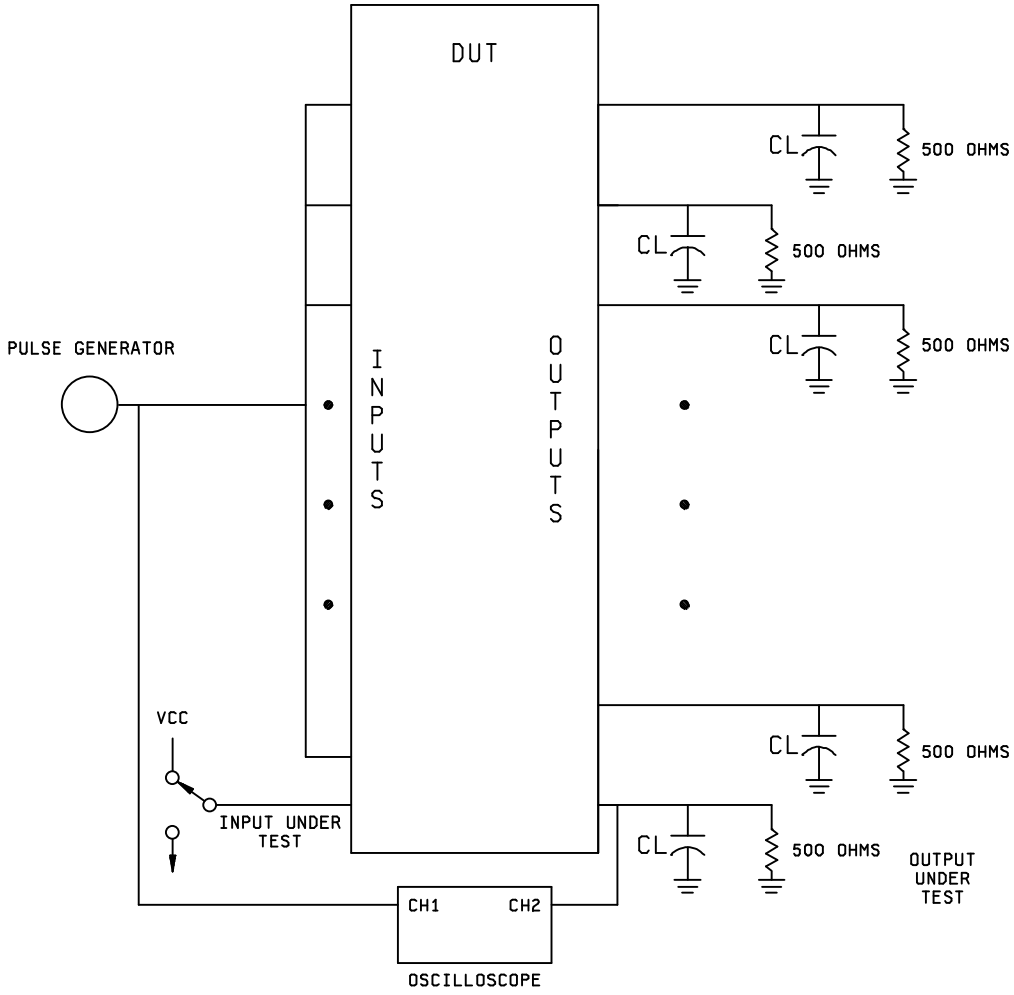
3. Procedure. The device shall be installed on the low noise fixture. All outputs of the device under test shall be loaded as specified in 2.2. All outputs (as many as functionally possible) shall be conditioned to switch using the setup information in 3.1. Tests shall be performed using the procedures in 3.2.

3.1 Setup parameters.

3.1.1 Supply voltage. Power supply voltage shall be at nominal operating voltage (5.0 volts for most families).

3.1.2 Test temperature. All tests shall be performed at 25°C.

3.1.3 Input conditioning. Input voltage levels shall be 0.0 V low level and V_{CC} for CMOS and 3.0 V for TTL for high level for both static and switching inputs. Switching inputs shall be driven by 1 MHz signals with 2.0 ±0.5 ns transition times. Maximum skew (made at the device package inputs) between any two input signals (including out-of-phase signals) shall be less than 1 ns. See figure 3024-2.



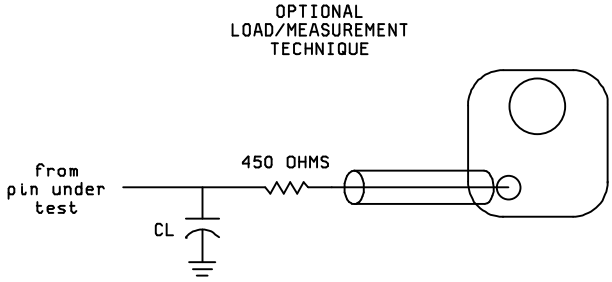


FIGURE 3024-1. Simultaneous switching noise test setup.

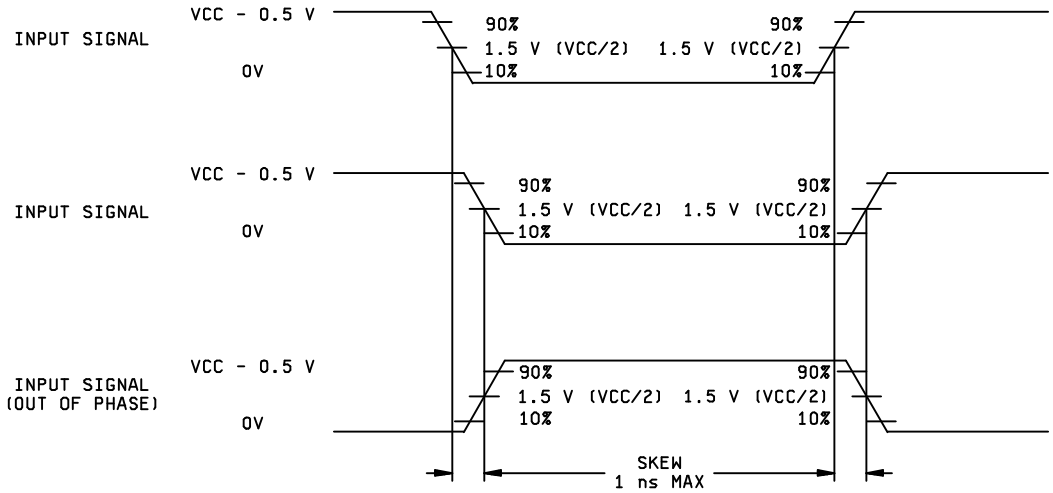


FIGURE 3024-2. Input waveforms.

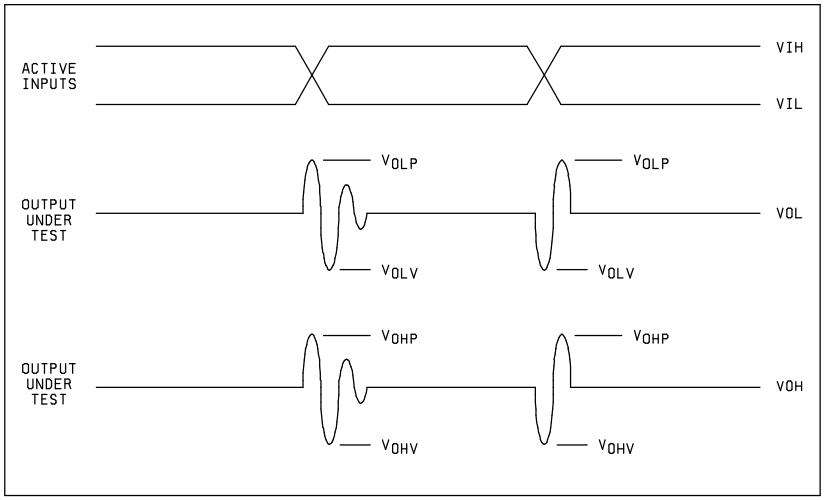


FIGURE 3024-3. Noise measurement technique.

3.2. Ground bounce test procedure. The output to be tested should be conditioned to a low level. The scope probe (if used) shall be connected to the output under test no more than 0.25 inches from the pin. The probe ground lead shall be attached to a suitable location (ground plane or pin) and have a maximum length of 1 inch. The ground bounce noise is the peak voltage in the positive (V_{OLP}) and negative (V_{OLV}) directions measured from the nominal V_{OL} level (see figure 3024-3). The noise must be measured at both the LOW to HIGH and the HIGH to LOW transition of the switching outputs. (Two consecutive areas of disruption need to be analyzed for the largest peak. If a second scope channel is available, it can be used to monitor the switching outputs and ease synchronization of the noise.) This test shall be repeated with each output at a low level with all others (functionally possible) switching. The largest peak on the worst output is the device ground bounce noise. Engineering judgement or experience may be used to reduce the number of pins tested provided that the rationale for this reduction of pins tested is documented and made available to the preparing activity or the acquiring activity upon request. (Generally, the noisiest pin on one device will be the noisiest pin on all devices of that type.)

3.3 V_{CC} bounce test procedure. The output to be tested should be conditioned to a high level. The scope probe (if used) shall be connected to the output under test no more than 0.25 inches from the pin. The probe ground lead shall be attached to a suitable location (ground plane or pin) and have a maximum length of 1 inch. The V_{CC} bounce noise is the peak voltage in the positive (V_{OHP}) and negative (V_{OHV}) directions measured from the nominal V_{OH} level. The noise must be measured at both the LOW to HIGH and the HIGH to LOW transition of the switching outputs. (Two consecutive areas of disruption need to be analyzed for the largest peak. If a second scope channel is available, it can be used to monitor the switching outputs and ease synchronization of the noise.) This test shall be repeated with each output at a high level with all others (functionally possible) switching. The largest peak on the worst output is the device V_{CC} bounce noise. Engineering judgement or experience may be used to reduce the number of pins tested provided that the rationale for this reduction of pins tested is documented and made available to the preparing activity or the acquiring activity upon request. (Generally, the noisiest pin on one device will be the noisiest pin on all devices of that type.)

4. Summary. The following details, when applicable, shall be specified in the acquisition document:

a. V_{CC} Supply voltage.

b. Test temperature.

c. Input switching frequency.

d. Number of outputs switching.

e. Package style of devices.

f. Conditioning levels of non-switching inputs.

g. Output pin(s) to be tested.