REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35	36	37	38	39															
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	26	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV															
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Jeff Bowling

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
98-11-06

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 28000 GATE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-98509**

SHEET 1 OF 39

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	98509	01	Q	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	XQ4028EX-4	28,000 gate programmable array	4.0 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a non-traditional performance environment encapsulated in plastic
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, JEDEC Publication 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA12-P299	299	Pin grid array package
Y	See figure 1	228	Quad flat package
Z	See figure 1	228	Quad flat package
U	LBGA-B-352 (JEDEC MO-192-BAR-2)	352	Ball grid array with four rows on each side (plastic)
T	PQFP-G-240 (JEDEC MS-029-GA)	240	Quad flat package with heat sink molded in the package (plastic)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V to V_{CC} + 0.5 V
Voltage applied to three-state output(V_{TS})	-0.5 V to V_{CC} + 0.5 V
Lead temperature (soldering, 10 seconds)	+260EC
Power dissipation (P_D)	2.0 W
Thermal resistance, junction-to-case (1_{JC}):	
Case outline X	See MIL-STD-1835
Case outlines Y, Z	20EC/W 3/
Case outlines U	0.8EC/W 3/
Case outlines T	1.5EC/W 3/
Junction temperature (T_J) Ceramic packages	+150EC 4/
Junction temperature (T_J) Plastic packages	+125EC 4/
Storage temperature range	-65EC to +150EC

1.4 Recommended operating conditions.

Supply voltage relative to ground(V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Input high voltage (V_{IH})	2.0 V dc to V_{CC}
Input low voltage (V_{IL})	0 V dc to 0.8 V dc
Maximum input signal transition time (t_{IN})	250 ns
Case operating temperature range (T_C)	-55EC to +125EC
Junction operating temperature range (T_J)	-55EC to +125EC for Plastic packages

1.5 Digital logic testing for device classes N, Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	99.9 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ All voltage values in this drawing are with respect to VSS
2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Blvd., Arlington, VA 22201.

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
High-level output voltage (TTL)	VOH	IOH = -4 mA, VCC=min (LVTTL)	1, 2, 3	01	2.4		V
High-level output voltage (CMOS)		IOH = -1.0 mA, VCC= min (LVCMOS)	1, 2, 3	01	V_{CC} - 0.5		V
Low-level output voltage (TTL)	VOL	IOL = 12 mA, VCC=min (LVTTL) 1/	1, 2, 3	01		0.4	V
Low-level output voltage (CMOS)		IOL = 12 mA, VCC=min (LVCMOS)	1, 2, 3	01		0.4	V
Data Retention Supply Voltage (below which configuration data may be lost)	VDR	(Read back mode only)	1, 2, 3	01	3.0		V
Quiescent FPGA Supply current 2/	ICCO		1, 2, 3	01		50	mA
Input or output leakage current	IL		1, 2, 3	01	-10	+10	FA
Input capacitance (sample tested) U and T packages	C_{IN}, C_{OUT}	See 4.4.1e, f = 1.0 Mhz, V_{OUT} = 0 V	4	01		10	pf
Input capacitance (sample tested) X, Y, Z packages	C_{IN}, C_{OUT}	See 4.4.1e, f = 1.0 Mhz, V_{OUT} = 0 V	4	01		16	pf
Pad pull-up (when selected)	IRPU	VIN = 0V (sample tested)	1, 2, 3	01	0.02	0.25	mA
Pad pull-down (when selected)	IRPD	VIN = 5.5 V (sample tested)	1, 2, 3	01	0.02	0.25	mA
Horizontal Longline pull-up (when selected) @ logic Low	IRLL		1, 2, 3	01	0.3	2.0	mA
Functional test	FT	See 4.4.1c	7, 8A, 8B	01			

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
CLB Switching Characteristic Guidelines							
Combinatorial Delays							
F/G inputs to X/Y outputs	TILO	See figures 3 and 4 as applicable 4/ 5/	9, 10, 11	01		2.2	ns
F/G inputs via H' to X/Y outputs	TIHO					3.8	
F/G inputs via transparent latch to Q outputs	TITO	See figures 3 and 4 as applicable 6/				3.2	
C inputs via SR/HO via H to X/Y outputs	THH0O	See figures 3 and 4 as applicable 4/ 5/				3.6	
C inputs via HI via H to X/Y outputs	THH1O					3.0	
C inputs via DIN/H2 via H to X/Y outputs	THH2O					3.6	
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	TCBYP					2.0	
CLB Fast Carry Logic							
Operand inputs (F1, F2, G1, G4) to COUT	TOPCY	See figure 3 as applicable 6/	9, 10, 11	01		2.5	ns
Add/Subtract input (F3) to COUT	TASCY	See figure 3 as applicable 6/				4.1	
Initialization inputs (F1,F3) to COUT	TINCY	See figure 3 as applicable 4/ 5/				1.9	
CIN through function generators to X/Y outputs	TSUM	See figure 3 as applicable 4/ 5/				3.0	
CIN to COUT, bypass function generators	TBYP	See figure 3 as applicable 6/				0.6	
Sequential Delays							
Clock K to Flip-Flop outputs Q	TCKO	See figures 3 and 4 as applicable 4/ 5/	9, 10, 11	01		2.2	ns
Clock K to Latch outputs Q	TCKLO	See figure 3 6/				2.2	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Setup Time before Clock K							
F/G inputs	TICK	See figure 3 6/	9, 10, 11	01	1.3		ns
F/G inputs via H'	TIHCK				3.0		ns
C inputs via H0 through H'	THH0CK				2.8		ns
C inputs via H1 through H'	THH1CK				2.2		ns
C inputs via H2 through H'	THH2CK				2.8		ns
C inputs Via DIN	TDICK				1.2		ns
C inputs via EC	TECCK				1.2		ns
C inputs via S/R, going Low (inactive)	TRCK				0.8		ns
CIN input via F'/G'	TCCK				2.2		ns
CIN input via F'/G' and H'	TCHCK				3.9		ns
Hold Time after Clock K							
F/G inputs	TCKI	See figure 3 6/	9, 10, 11	01	0		ns
F/G inputs via H'	TCKIH				0		ns
C inputs via SR/HO through H'	TCKHH0				0		ns
C inputs via H1 through H'	TCKHH1				0		ns
C inputs via DIN/H2 through H'	TCKHH2				0		ns
C inputs via DIN/H2	TCKDI				0		ns
C inputs via EC	TCKEC				0		ns
C inputs via SR, going Low (inactive)	TCKR				0		ns
Clock							
Clock High time	TCH	See figure 3 6/	9, 10, 11	01	3.5		ns
Clock Low time	TCL				3.5		ns

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Set/Reset Direct (The following table must be used to adjust output parameters and output switching characteristics.)							
Width (High)	TRPW	See figure 3 6/	9, 10, 11	01	3.5		ns
Delay from C inputs via S/R, going High to Q	TRIO					4.5	ns
Global Set/Reset							
Minimum GSR Pulse Width	TMRW	See figure 3 6/	9, 10, 11	01	13		ns
Delay from GSR input to any Q 7/	TMRQ					22.8	ns
Delay from GSR input to any Pad 8/	TRPO					30.2	ns
Toggle Frequency (MHz) 9/	FTOG					143	MHz
Propogation Delays (IOB Output Switching Characteristic Guidelines)							
Clock (OK) to Pad	TOKPOF	See figure 3 6/ 8/	9, 10, 11	01		7.4	ns
Output (O) to Pad	TOPF					6.2	
3 state to Pad hi-Z (slew-rate independent)	TTSHZ					4.9	
3-state to Pad active and valid	TTSONF					6.2	
Output (O) to Pad via Fast Output MUX	TOFPF					6.7	
Setup and Hold Times							
Output (O) to clock (OK) setup time	TOOK	See figure 3 6/ 8/	9, 10, 11	01	0.6		
Output (O) to clock (OK) hold time	TOKO				0		
Clock Enable (EC) to clock (OK) setup	TECOK				0		
Clock Enable (EC) to clock (OK) hold	TOKEC				0		

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Output Level and Slew Rate Adjustment							
For TTL output FAST add	TTTLOF		9, 10 11	01		0	ns
For TTL output SLOW add	TTTLO					2.9	
For CMOS FASToutput add	TCMOSOF					1.0	
For CMOS SLOW output add	TCMOSO					3.6	
BENCHMARK PATTERNS (100% Tested) Conditions							
Core + TILO+TIHO	TILHO1	See figure 4 as applicable 4/ 5/ 10/	9, 10, 11	01		68.4	ns
Core + TILO+TIHO	TILHO2					69	
Core + TILO+TIHO	TILHO3					68.4	
Core + TILO+TIHO	TILHO4					69.0	
Core + TILO+TIHO	TILHO5					66.6	
Core + THH0O +THECQO	THH0O					103.1	
Core + THH10 + THH2QO	THH10					103.4	
Core + THH20 + THELQO	THH20					102.4	
Core + TINCY + TSUM	CRY1					71.1	
Local Line Patterns							
Core + Local Line 1	LOCAL 1	See figure 4 as applicable 4/ 5/ 10/	9, 10, 11	01		143.1	ns
Core + Local Line 2	LOCAL 2					157.7	
Core + Local Line 3	LOCAL 3					151	
Core + Local Line 4	LOCAL 4					161.6	
Core + Local Line 5	LOCAL 5					178.7	
Core + Local Line 6	LOCAL 6					153.9	
Core + Local Line 7	LOCAL 7					166.5	
Core + Local Line 8	LOCAL 8					139.5	
Core + Local Double Line 1	DBL 1					108.8	
Core + Local Double Line 2	DBL 2					107.5	
Core + Horizontal Quad A	QHA					101.9	
Core + Horizontal Quad B	QHB					99.4	
Core + Horizontal Quad C	QHC					95.6	
Core + Verticle Quad A	QVA					90.2	
Core + Verticle Quad B	QVB					122.6	
Core + Verticle Quad C	QVC					83.5	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Long-Line patterns							
Core + Horizontal Long Line 1	HLL1	See figure 4 as applicable 4/ 5/ 10/	9, 10, 11	01		147.8	ns
Core + Horizontal Long Line 2	HLL2					235.4	
Core + Horizontal Long Line 3	HLL3					384.6	
Core + Horizontal Long Line 4	HLL4					369.8	
Core + Horizontal Long Line 5	HLL5					300.2	
Core + Horizontal Long Line 6	HLL6					226.5	
Core + Vertical Long Line 1	VLL1					113.2	
Core + Vertical Long Line 2	VLL2					114.1	
Core + Vertical Long Line 3	VLL3					122.1	
Core + Vertical Long Line 4	VLL4					106.4	
Core + Vertical Long Line 5	VLL5					117.1	
Core + Vertical Long Line 6	VLL6					115.2	
Core + Vertical Long Line 7	VLL7					116.6	
Core + Vertical Long Line 8	VLL8					111.4	
Core + Vertical Long Line 9	VLL9					108.6	
Core + Vertical Long Line 10	VLL10					109.2	
Core + Horizontal Long Line 3 (Loaded)	HLL3_L					380.9	
Core + Vertical Long Line 7 (Loaded)	VLL7_L	See figure 4 as applicable 4/ 5/ 10/				116.6	
Core + Vertical Long Line 9 (Loaded)	VLL9_L					106.9	
Core + Vertical Long Line 10 (Loaded)	VLL10_L					109.2	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Clock Patterns							
Global Low Skew Clock	GLS	See figure 4 as applicable 4/ 5/	9, 10, 11	01		97.6	ns
KB Clock Line	KB_K					111.8	
Edge Line Patterns							
Core + Edge Long Line	EDGELL	See figure 4 as applicable. 4/ 5/ and (10/ where applicable)	9, 10, 11	01		248.0	ns
Octal 1	OCTAL 1					269.9	
Core + Top Edge Double Line	T_EDBL					110.1	
Core + Left Edge Double Line	L_EDBL					112.6	
Core + Bottom Edge Double Line	B_EDBL					135.8	
Core +Right Edge Double Line	R_EDBL					115.9	
Top Left Half Wide Decoder	TL_HWD2					127.5	
Top Right Half Wide Decoder	TR_HWD2					123.1	
Full Wide Decoder	R_WD2					171.6	
Buffer Patterns							
Full Length Tbuf at HLL3	F_TBUF3	See figure 4 as applicable 4/ 5/	9, 10, 11	01		114	ns
Full Length Tbuf at HLL4	F_TBUF4					114.8	
Left Half Length Tbuf at HLL3 with 4 Pullup	L_TBUF3_4					97.4	
Left Half Length Tbuf at HLL4 with 4 Pullup	L_TBUF4_4					97	
Left Half Length Tbuf at HLL3 with 1 Pullup	L_TBUF3_1					79.7	
Left Half Length Tbuf at HLL4 with 1 Pullup	L_TBUF4_1					80.8	
Right Half Length Tbuf at HLL3 with 4 Pullup	R_TBUF3_4					97.3	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Right Half Length Tbuf at HLL4 with 4 Pullup	R_TBUF4_4	See figure 4 as applicable 4/ 5/	9, 10, 11	01		96.8	ns
Right Half Length Tbuf at HLL3 with 1 Pullup	R_TBUF3_1					82.1	
Right Half Length Tbuf at HLL4 with 1 Pullup	R_TBUF4_1					83.6	
Clock/Setup/Hold Patterns							
GLS Clock Setup	GLSTSU	See figure 4 as applicable 4/ 5/	9, 10, 11	01	8.0		ns
GE Clock Setup	GETSU				8.1		
GLS Clock Hold	GLSHOLD				0		
GE Clock Hold	GEHOLD				0		
OFF Clock To Out (rise)	TCKRISE	See figure 4 as applicable 4/ 5/	9, 10, 11	01		17.7	ns
OFF Clock To Out (fall)	TCKFALL					18	
IOB Patterns (CMOS)							
TPPLI To TOPS	TPPLI_TOPS	See figure 4 as applicable 4/ 5/ and (11/ where applicable)	9, 10, 11	01		25.2	ns
TPLI To Out Thru EC	TPLI_TECI					13.6	
TPPLI To Out Thru EC	TPPLI_TEC					24.5	
TPDLI To TOPF	TPDLI_TOPF					27	
TPFLI to TOPF	TPFLI_TOPF					24.6	
TPID To Out Thru MUX	TPID_TMUXO					12.1	
TPPFLI To TOPF	TPPFLI_TOPF					12.6	
TPID To TOPF	TPID_TOPF					28.4	
IOB Patterns (TTL)							
TPPLI TO TOPS	TPPLI_TOPS	See figure 4 as applicable 4/ 5/ and (11/ where applicable)	9, 10, 11	01		23.9	ns
TPLI TO OUT THRU EC	TPLI_TECI					12.3	
TPPLI TO OUT THRU EC	TPPLI_TEC					23.2	
TPDLI TO TOPF	TPDLI_TOPF					25.7	
TPFLI TO TOPF	TPFLI_TOPF					23.3	
TPID TO OUT THRU MUX	TPID_TMUXO					10.8	
TPPFLI TO TOPF	TPPFLI_TOPF					11.3	
TPID TO TOPF	TPID_TOPF					27	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
TBUF driving half a Horizontal Longline (Horizontal Longline Switching Characteristics Guidelines)							
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T HI01	See figure 4 as applicable 4/ 5/ 12/	9, 10, 11	01		6.3	ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low	T HON					7.2	
TBUF driving a Horizontal Longline							
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T I0I	See figure 4 as applicable 4/ 5/ 12/	9, 10, 11	01		13.7	ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T ON					14.7	
Setup Times (IOB Input Switching Characteristic Guidelines)							
Pad to Clock (IK), no delay	TPICK	See figure 3 as applicable 6/ 13/ 14/	9, 10, 11	01	2.5		ns
Pad to Clock (IK), partial delay	TPICKP				10.8		
Pad to Clock (IK), full delay	TPICKD				15.7		
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	TPICKF				3.9		
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	TPICKFP				12.3		

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Pad to Fast Capture Latch Enable (OK), no delay	TPOCK	See figure 3 as applicable 6/ 13/ 14/	9, 10, 11	01	0.8		ns
Pad to Fast Capture Latch Enable (OK), partial delay	TPOCKP				9.1		
Set-up times (TTL and CMOS)							
Clock Enable (EC) to Clock (IK)	TECIK	See figure 3 as applicable 6/ 13/ 14/	9, 10, 11	01	0.3		ns
Hold Times							
Pad to Clock (IK),		See figure 3 as applicable 6/ 13/ 14/	9, 10 ,11	01			ns
no delay	TIKPI				0		
partial delay	TIKPIP				0		
full delay	TIKPID				0		
Pad to Clock (IK) via transparent Fast Capture Latch,							
no delay	TIKFPI				0		
partial delay	TIKFPIP				0		
full delay	TIKFPID				0		
Clock Enable (EC) to Clock (IK),							
no delay	TIKEC				0		
partial delay	TIKECP				0		
full delay	TIKECD				0		
Pad to Fast Capture Latch Enable (OK),							
no delay	TOKPI				0		
partial delay	TOKPIP				0		
Propagation Delays							
Pad to I1, 12 via transparent FCL and input latch, no delay 15/	TPFLI	See figures 3 and 4 as applicable 4/ 5/ 13/ 14/	9, 10, 11	1		5.3	ns
Pad to I1, 12 via transparent FCL and input latch, partial delay 15/	TPPFLI					13.6	
Clock (IK) to I1, 12 (flip flop)	TIKRI	See figures 3 and 4 as applicable 6/ 13/ 14/				3.0	
Clock (IK) to I1, 12 (latch enable, active Low)	TIKLI					3.2	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
FCL Enable (OK) active edge to I1, 12 (via transparent standard input latch) 15/	TOKLI	See figures 3 and 4 as applicable 6/ 13/ 14/				6.2	
Minimum GSR Pulse Width	TMRW				13.0		
Delay from GSR input to any Q	TRRI					22.8	
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge 16/	TOKIK				3.2		
Pad to I1, 12	TPID	See figures 3 and 4 as applicable 4/ 5/ 13/ 14/				2.2	
Pad to I1, 12 via transparent input latch, no delay	TPLI					3.8	
Pad to I1, 12 via transparent input latch, partial delay	TPPLI					13.3	
Pad to I1, 12 via transparent input latch, full delay	TPDLI					18.2	
Output Flip-Flop, Clock to Out (Pin to Pin Output parametrics Guidelines)							
Global Low Skew Clock to TTL Output (fast) using OFF 17/	TICKOF	See figures 3 and 4 as applicable 4/ 5/ 8/ 18/ 19/	9, 10, 11	01		16.6	ns
Global Early Clock to TTL Output (fast) using OFF 17/ 20/	TICKEOF					13.1	
Output/Output Mux/Clock to out							
Global Low Skew Clock to TTL Output (fast) using OMUX 21/	TPFPF	See figure 3 as applicable 6/ 8/ 18/ 19/	9, 10, 11	01		15.9	ns
Global Early Clock to TTL Output (fast) using OMUX 20/ 21/	TPEFPF					12.4	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 4.5 V#Vcc#5.5 V (-55EC#T_C #+125EC for ceramic packages) (-55EC#T_J #+125EC for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Global Low Skew Clock, Set-Up and Hold (Pin to pin input parameters guidelines)							
Input Setup Time, using Global Low Skew clock and IFF (full delay) 16/	TPSD	See figure 3 as applicable 6/ 14/ 19/	9, 10, 11	01	8.0		ns
Input Hold Time, using Global Low Skew clock and IFF (full delay) 16/	TPHD				0		
Global Early Clock, Set-Up and Hold for IFF							
Input set-up time, using global early clock and IFF (partial delay) 16/	TPSEP	See figure 3 as applicable 6/ 14/ 19/ 20/ 22/	9, 10, 11	01	6.5		ns
Input hold time, using global early clock and IFF (partial delay) 16/	TPHEP				0		
Global Early Clock, Set-Up and Hold for FCL							
Input set-up time, using global early clock and FCL (partial delay) 15/	TPFSEP	See figure 3 as applicable 6/ 14/ 19/ 23/	9, 10, 11	01	3.4		ns
Input hold time, using global early clock and FCL (partial delay) 15/	TPFHEP				0		
Input Threshold Adjustments (The following table must be used to adjust output parameters and output switching characteristics.)							
For TTL input add	TTTLI		9, 10, 11	01	0		ns
For CMOS input add	TCMOSI					0.3	
Global Buffers Switching Characteristic Guidelines							
From pad through Global Low Skew buffer, to any clock K	TGLS	See figure 4 as applicable 4/ 5/	9, 10, 11	01		9.2	ns
From pad through Global Early buffer, to any clock K in same quadrant	TGE					5.7	

See notes at end of table.

1/ With up to 64 pins simultaneously sinking 12 mA.

2/ With no output current loads, no active input or Longline pull-up resistors, all package pins at VCC or GND.

3/ These delays are specified from the decoder input to the decoder output. Fewer than the specified number of pull up resistors can be used, if desired. Using fewer pull ups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pull ups are used.

4/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark timing patterns are then used to determine the compliance of this parameter. Characterization data is taken at initial device introduction, and after any design or process changes which may affect this parameter.

5/ Benchmark patterns are used to determine compliance to this parameter.

6/ Parameter is not tested but is guaranteed by design through simulation.

7/ For values per device, see Globals Set/Reset entries.

8/ Output timing is measured at TTL threshold, with 35 pF external capacitive loads. For CMOS output levels, see the "Output Level and Slew Rate Adjustments".

9/ Maximum flip-flop toggle rate for export control purposes.

10/ Core = TILO + TCKO

11/ These delays are specified from the decoder input to the decoder ouput. For pad-to-pad delays, add the input delay (TPID) output delay (TOPF or TOPS) .

12/ These values include a minimum load of one output, spaced a far as possible from the active pullup(s). Use the static timing analyzer to determine the delay for each destination.

13/ For setup and hold time with respect to the clock input pin, see the Global Low Skew clock and Global Early clock setup and hold tables.

14/ For CMOS input levels, see the "Input threshold Adjustments".

15/ FCL = Fast Capture Latch

16/ IFF = Input Flip-Flop or Latch

17/ OFF = Output Flip Flop

18/ These are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net. Output timing is measured at ~50% VCC threshold with 35 pF external capacitive load.

19/ Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold time under given design conditions .

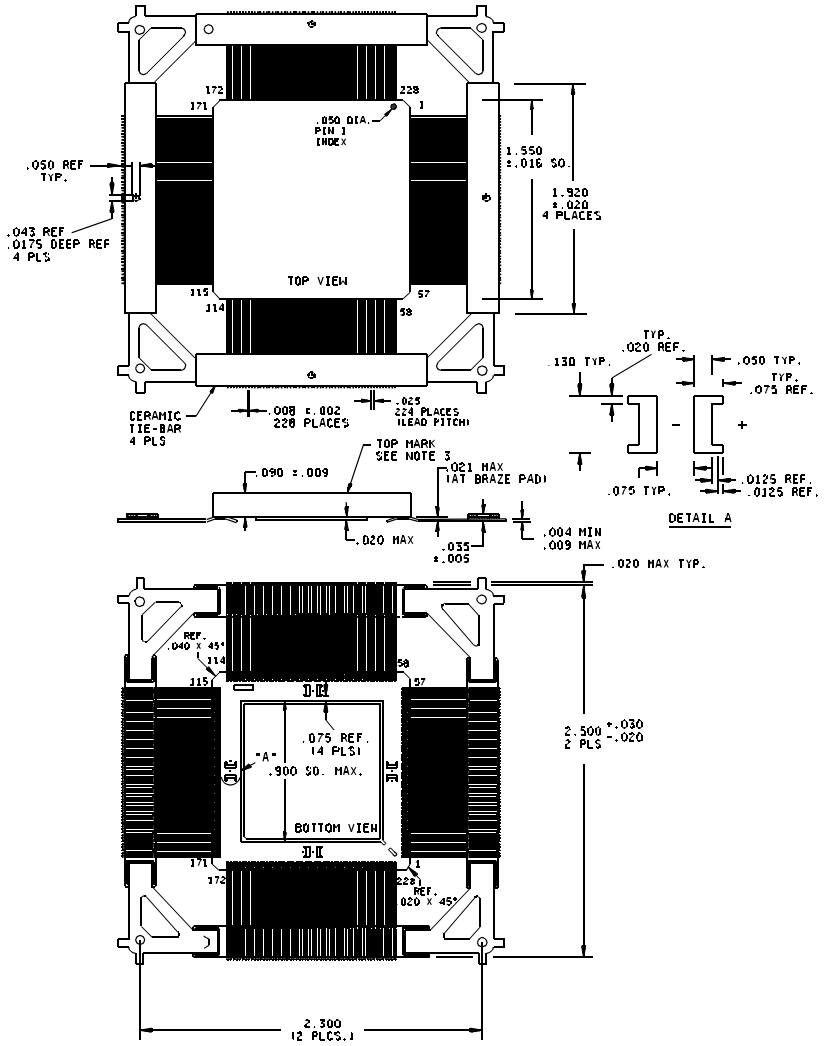
20/ BUFGE = Global Early Buffers

21/ OMUX = Output MUX

22/ Parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

23/ Setup parameters are for BUFGE #s 3, 4, 7, and 8. Add 1.2 ns for BUFGE #s 1, 2, 5, and 6.

Cases Y and Z



NOTES:
1. Dimensions are in inches.
2. Packages are shipped flat as depicted
3. Lead dimensions call out includes lead finish.
4. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.
5. Case Y represents marking the device on the nonlid side of device, i.e., lid side facing down. When mounted in this position, the pin out is clockwise. Case Z represents marking the device on the lid side of the device i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise.

FIGURE 1. Case outline.

Inch to metric conversion table for convenience only.

Inches	Metric mm
2.500	63.50
2.300	58.42
1.920	48.77
1.550	39.37
.900	22.86
.130	3.30
.125	3.18
.090	2.29
.075	1.91
.050	1.27
.043	1.09
.040	1.02
.035	.89
.030	.76
.025	.64
.021	.53
.020	.51
.0175	.44
.016	.41
.0125	.32
.009	.23
.008	.20
.005	.13
.004	.10
.002	.05

FIGURE 1. Case outline - Continued.

Case U

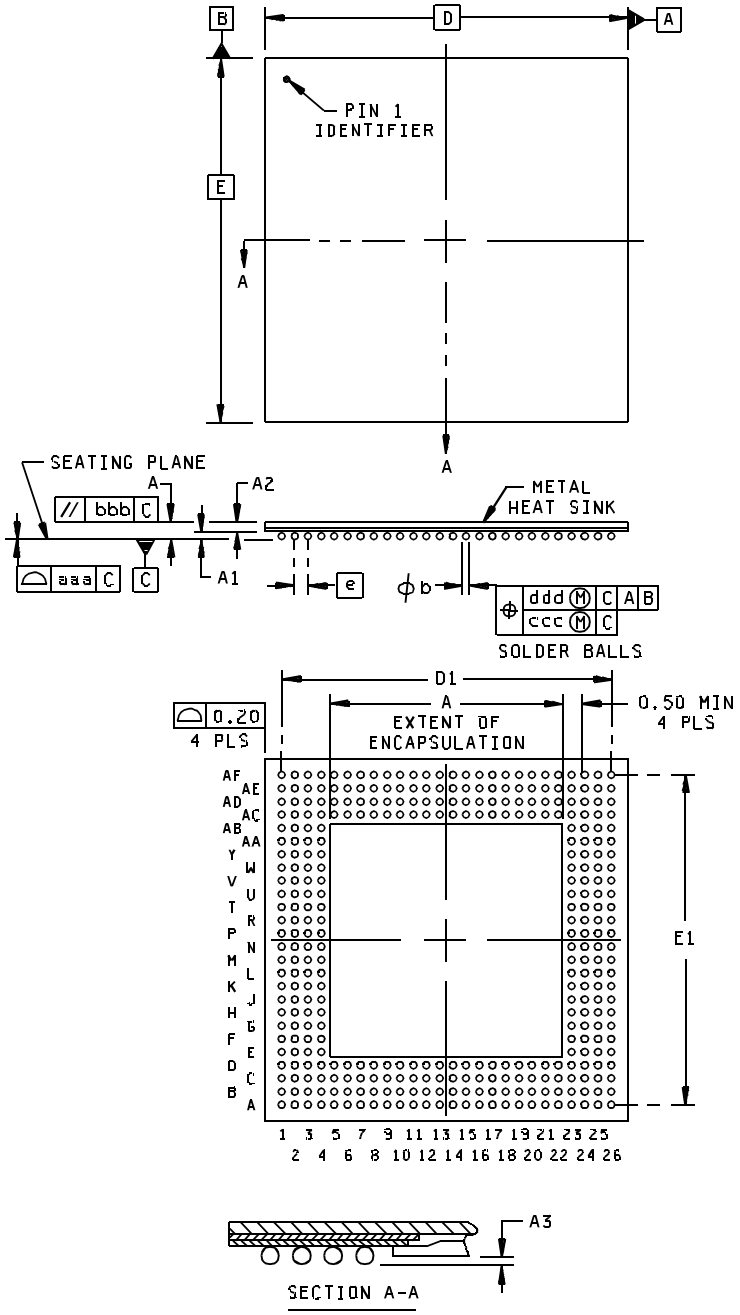


FIGURE 1. Case outline - Continued.

BG352			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	1.10	1.40	1.70
A1	0.50	0.60	0.70
A2	0.60	---	1.00
A3	0.20	---	---
D/E	35.00 BSC		
D1/E1	31.75 REF		
e	1.27 BSC		
i b	0.60	0.75	0.90
aaa	---	---	0.20
bbb	---	---	0.25
ccc	---	---	0.15
ddd	---	---	0.30
M	26		
REF	JEDEC MO-192-BAR-2		

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1994.
2. Symbol "M" is the pin matrix size.
3. Conforms to JEDEC MO-192 (Depopulated).

FIGURE 1. Case outline - Continued.

Device type	All	Device type	All	Device type	All
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	VCC	C10	I/O	E17	I/O
A3	I/O	C11	I/O	E18	I/O
A4	I/O	C12	I/O	E19	I/O
A5	GND	C13	I/O	E20	GND
A6	VCC	C14	I/O	F1	GND
A7	I/O	C15	I/O	F2	I/O
A8	I/O	C16	I/O	F3	I/O
A9	I/O	C17	BUFGS_BL_GCK2_ I/O	F4	I/O
A10	GND			F5	I/O
A11	VCC	C18	M0	F16	I/O
A12	I/O	C19	HDC_I/O	F17	I/O
A13	I/O	C20	&&&_I/O	F18	I/O
A14	I/O	D1	I/O	F19	I/O
A15	GND	D2	I/O	F20	VCC
A16	VCC	D3	A14_I/O	G1	I/O
A17	I/O	D4	BUFGP_TL_ GCK1_A16_I/O	G2	I/O
A18	I/O			G3	I/O
A19	GND	D5	TDI_I/O	G4	I/O
A20	M1	D6	I/O	G5	A12_I/O
B1	GND	D7	I/O	G16	I/O
B2	A17_I/O	D8	I/O	G17	I/O
B3	I/O	D9	I/O	G18	I/O
B4	I/O	D10	I/O	G19	I/O
B5	I/O	D11	I/O	G20	I/O
B6	I/O_FCLK1	D12	I/O	H1	A10_I/O
B7	I/O	D13	I/O_FCLK2	H2	I/O
B8	I/O	D14	I/O	H3	I/O
B9	I/O	D15	I/O	H4	I/O
B10	I/O	D16	I/O	H5	I/O
B11	I/O	D17	M2	H16	I/O
B12	I/O	D18	I/O	H17	I/O
B13	I/O	D19	I/O	H18	I/O
B14	I/O	D20	I/O	H19	I/O
B15	I/O	E1	VCC	H20	I/O
B16	I/O	E2	I/O	J1	I/O
B17	I/O	E3	I/O	J2	I/O
B18	I/O	E4	I/O	J3	A11_I/O
B19	BUFGP_BL_ GCK3_I/O	E5	VCC	J4	I/O
		E6	I/O	J5	I/O
B20	VCC	E7	I/O	J16	I/O
C1	A13_I/O	E8	I/O	J17	I/O
C2	I/O	E9	I/O	J18	I/O
C3	BUFGS_TL_ GCK8_A15_I/O	E10	I/O	J19	I/O
		E11	I/O	J20	I/O
C4	TCK_I/O	E12	I/O	K1	VCC
C5	I/O	E13	I/O	K2	A8_I/O
C6	I/O	E14	I/O	K3	A9_I/O
C7	TMS_I/O	E15	I/O	K4	A18_I/O
C8	I/O	E16	GND	K5	A19_I/O
C9	I/O				

FIGURE 2. Terminal connections.

Device type	All	Device type	All	Device type	All
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
K16	I/O	P5	I/O	U4	TDO
K17	I/O	P16	I/O	U5	I/O
K18	I/O	P17	I/O	U6	D1_I/O
K19	&&&&_I/O	P18	I/O	U7	I/O
K20	GND	P19	I/O	U8	I/O
L1	GND	P20	I/O	U9	I/O
L2	A7_I/O	R1	VCC	U10	I/O
L3	A6_I/O	R2	I/O	U11	I/O
L4	A20_I/O	R3	I/O	U12	I/O
L5	I/O	R4	I/O	U13	I/O
L16	I/O	R5	I/O	U14	I/O
L17	I/O	R16	I/O	U15	I/O
L18	I/O	R17	I/O	U16	I/O
L19	I/O	R18	I/O	U17	&&&&
L20	VCC	R19	I/O	U18	I/O
M1	A21_I/O	R20	GND	U19	I/O
M2	I/O	T1	GND	U20	I/O
M3	A5_I/O	T2	I/O	V1	A3_I/O
M4	I/O	T3	I/O	V2	BUFGP_TR_
M5	I/O	T4	I/O		GCK7_A1_I/O
M16	I/O	T5	GND	V3	CCLK
M17	I/O	T6	I/O	V4	D0_DIN_I/O
M18	I/O	T7	I/O	V5	RDY_&&&&_
M19	I/O	T8	I/O		&&&&_I/O
M20	I/O	T9	I/O	V6	I/O
N1	A4_I/O	T10	I/O	V7	I/O
N2	I/O	T11	I/O	V8	I/O
N3	I/O	T12	D5_I/O	V9	I/O
N4	I/O	T13	I/O	V10	&&_I/O
N5	I/O	T14	I/O	V11	D4_I/O
N16	I/O	T15	I/O	V12	I/O
N17	I/O	T16	VCC	V13	I/O
N18	I/O	T17	I/O	V14	I/O
N19	I/O	T18	I/O	V15	I/O
N20	I/O	T19	I/O	V16	I/O
P1	I/O	T20	VCC	V17	I/O
P2	I/O	U1	I/O	V18	DONE
P3	I/O	U2	I/O	V19	I/O
P4	I/O	U3	CSI_A2_I/O	V20	I/O

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
W1	VCC	X1	BUFGS_TR_
W2	A0_&&_I/O		GCK6_DOUT_I/O
W3	I/O	X2	GND
W4	I/O	X3	I/O
W5	I/O	X4	I/O
W6	I/O	X5	VCC
W7	I/O_FCLK4	X6	GND
W8	D2_I/O	X7	I/O
W9	I/O	X8	I/O
W10	D3_I/O	X9	I/O
W11	I/O	X10	VCC
W12	I/O	X11	GND
W13	I/O	X12	I/O
W14	I/O_FCLK3	X13	I/O
W15	I/O	X14	&&&_I/O
W16	I/O	X15	VCC
W17	D6_I/O	X16	GND
W18	BUFGP_BR_GCK5_ I/O	X17	I/O
		X18	I/O
W19	D7_I/O	X19	VCC
W20	GND	X20	BUFGS_BR_ GCK4_I/O

FIGURE 2. Terminal connections - Continued.

Case outlines Y and Z

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	VSS		51	I/O		101	I/O
2	BUFGP_TL_A16_GCK1_I/O		52	I/O		102	I/O
3	A17_I/O		53	I/O		103	I/O
4	I/O		54	BUFGS_BL_GCK2_I/O		104	I/O
5	I/O		55	M1		105	I/O
6	TDI_I/O		56	VSS		106	I/O
7	TCK_I/O		57	M0		107	I/O
8	I/O		58	VCC		108	I/O
9	I/O		59	M2		109	I/O
10	I/O		60	BUFGP_BL_GCK3_I/O		110	I/O
11	I/O		61	HDC_I/O		111	I/O
12	I/O		62	I/O		112	BUFGS_BR_GCK4_I/O
13	I/O		63	I/O		113	VSS
14	VSS		64	I/O		114	DONE
15	I/O_FCLK1		65	&&&_I/O		115	VCC
16	I/O		66	I/O		116	&&&&
17	TMS_I/O		67	I/O		117	D7_I/O
18	I/O		68	I/O		118	BUFGP_BR_GCK5_I/O
19	I/O		69	I/O		119	I/O
20	I/O		70	I/O		120	I/O
21	I/O		71	I/O		121	I/O
22	I/O		72	VSS		122	I/O
23	I/O		73	I/O		123	D6_I/O
24	I/O		74	I/O		124	I/O
25	I/O		75	I/O		125	I/O
26	I/O		76	I/O		126	I/O
27	VSS		77	I/O		127	I/O
28	VCC		78	I/O		128	I/O
29	I/O		79	I/O		129	VSS
30	I/O		80	I/O		130	I/O
31	I/O		81	I/O		131	I/O
32	I/O		82	I/O		132	I/O_FCLK3
33	I/O		83	I/O		133	I/O
34	I/O		84	&&&&_I/O		134	D5_I/O
35	I/O		85	VCC		135	&&&_I/O
36	I/O		86	VSS		136	I/O
37	VCC		87	I/O		137	I/O
38	I/O		88	I/O		138	I/O
39	I/O		89	I/O		139	I/O
40	I/O		90	I/O		140	D4_I/O
41	I/O_FCLK2		91	I/O		141	I/O
42	VSS		92	I/O		142	VCC
43	I/O		93	I/O		143	VSS
44	I/O		94	I/O		144	D3_I/O
45	I/O		95	VCC		145	&&_I/O
46	I/O		96	I/O		146	I/O
47	I/O		97	I/O		147	I/O
48	I/O		98	I/O		148	I/O
49	I/O		99	I/O		149	I/O
50	I/O		100	VSS		150	D2_I/O

FIGURE 2. Terminal connections.

Case outlines Y and Z Continued.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
151	I/O		177	I/O		203	A9_I/O
152	VCC		178	CSI_A2_I/O		204	A19_I/O
153	I/O		179	A3_I/O		205	A18_I/O
154	I/O_FCLK4		180	I/O		206	I/O
155	I/O		181	I/O		207	I/O
156	I/O		182	I/O		208	A10_I/O
157	VSS		183	I/O		209	A11_I/O
158	I/O		184	I/O		210	VCC
159	I/O		185	I/O		211	I/O
160	I/O		186	VSS		212	I/O
161	I/O		187	I/O		213	I/O
162	I/O		188	I/O		214	I/O
163	I/O		189	I/O		215	VSS
164	D1_I/O		190	I/O		216	I/O
165	RDY_&&&&_&&&&_I/O		191	VCC		217	I/O
166	I/O		192	A4_I/O		218	I/O
167	I/O		193	A5_I/O		219	I/O
168	D0_DIN_I/O		194	I/O		220	A12_I/O
169	BUFGS_TR_GCK6_DOUT_I/O		195	I/O		221	A13_I/O
170	CCLK		196	A21_I/O		222	I/O
171	VCC		197	A20_I/O		223	I/O
172	TDO		198	A6_I/O		224	I/O
173	VSS		199	A7_I/O		225	I/O
174	A0_&&_I/O		200	VSS		226	A14_I/O
175	BUFGP_TR_GCK7_A1_I/O		201	VCC		227	BUFGS_TL_GCK8_A15_I/O
176	I/O		202	A8_I/O		228	VCC

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	GND	C4	BUFGP_TR_GCK7	E4	BUFGS_TR_
A2	GND		_A1_I/O		GCK6_DOUT_I/O
A3	I/O	C5	NO CONNECT	E23	I/O
A4	I/O	C6	A3_I/O	E24	TCK_I/O
A5	GND	C7	I/O	E25	I/O
A6	I/O	C8	NO CONNECT	E26	GND
A7	I/O	C9	I/O	F1	I/O
A8	GND	C10	I/O	F2	I/O
A9	I/O	C11	NO CONNECT	F3	D1_I/O
A10	VCC	C12	A5_I/O	F4	I/O
A11	I/O	C13	A21_I/O	F23	NO CONNECT
A12	I/O	C14	A9_I/O	F24	I/O
A13	A6_I/O	C15	I/O	F25	I/O
A14	GND	C16	I/O	F26	I/O
A15	A19_I/O	C17	I/O	G1	I/O
A16	A10_I/O	C18	I/O	G2	I/O
A17	VCC	C19	I/O	G3	I/O
A18	NO CONNECT	C20	I/O	G4	RDY_&&&&_
A19	GND	C21	A13_I/O		&&&&_I/O
A20	I/O	C22	I/O	G23	VCC
A21	I/O	C23	I/O	G24	I/O
A22	GND	C24	BUFGS_TL_GCK8	G25	I/O
A23	I/O		_A15_I/O	G26	I/O
A24	NO CONNECT	C25	A17_I/O	H1	GND
A25	GND	C26	TDI_I/O	H2	I/O
A26	GND	D1	NO CONNECT	H3	I/O
B1	GND	D2	I/O	H4	VCC
B2	VCC	D3	D0_DIN_I/O	H23	I/O
B3	A0_&&_I/O	D4	TDO	H24	I/O
B4	NO CONNECT	D5	I/O	H25	TMS_I/O
B5	I/O	D6	CSI_A2_I/O	H26	GND
B6	I/O	D7	VCC	J1	D2_I/O
B7	I/O	D8	I/O	J2	I/O
B8	I/O	D9	I/O	J3	I/O_FCLK4
B9	I/O	D10	I/O	J4	I/O
B10	NO CONNECT	D11	I/O	J23	I/O_FCLK1
B11	I/O	D12	A4_I/O	J24	I/O
B12	I/O	D13	VCC	J25	I/O
B13	A20_I/O	D14	A8_I/O	J26	NO CONNECT
B14	A7_I/O	D15	I/O	K1	VCC
B15	A18_I/O	D16	NO CONNECT	K2	NO CONNECT
B16	A11_I/O	D17	I/O	K3	I/O
B17	I/O	D18	I/O	K4	I/O
B18	I/O	D19	VCC	K23	I/O
B19	I/O	D20	I/O	K24	I/O
B20	I/O	D21	I/O	K25	I/O
B21	I/O	D22	A14_I/O	K26	VCC
B22	A12_I/O	D23	BUFGP_TL_A16_	L1	I/O
B23	NO CONNECT		GCK1_I/O	L2	I/O
B24	I/O	D24	I/O	L3	I/O
B25	VCC	D25	NO CONNECT	L4	NO CONNECT
B26	GND	D26	I/O	L23	NO CONNECT
C1	NO CONNECT	E1	GND	L24	I/O
C2	I/O	E2	I/O	L25	I/O
C3	CCLK	E3	I/O	L26	I/O

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
M1	I/O	W1	GND	AC24	BUFGS_BL_ GCK2_I/O
M2	I/O	W2	I/O		
M3	I/O	W3	I/O	AC25	NO CONNECT
M4	I/O	W4	I/O	AC26	I/O
M23	I/O	W23	VCC	AD1	I/O
M24	I/O	W24	I/O	AD2	D7_I/O
M25	I/O	W25	I/O	AD3	DONE
M26	I/O	W26	GND	AD4	I/O
N1	GND	Y1	I/O	AD5	I/O
N2	D3_I/O	Y2	I/O	AD6	I/O
N3	I/O	Y3	D6_I/O	AD7	I/O
N4	&&_I/O	Y4	VCC	AD8	I/O
N23	VCC	Y23	I/O	AD9	I/O
N24	I/O	Y24	I/O	AD10	I/O
N25	I/O	Y25	I/O	AD11	I/O
N26	I/O	Y26	I/O	AD12	I/O
P1	I/O	AA1	I/O	AD13	I/O
P2	D4_I/O	AA2	I/O	AD14	I/O
P3	I/O	AA3	I/O	AD15	I/O
P4	VCC	AA4	I/O	AD16	NO CONNECT
P23	I/O	AA23	I/O	AD17	I/O
P24	I/O	AA24	I/O	AD18	I/O
P25	I/O	AA25	I/O	AD19	I/O
P26	GND	AA26	I/O	AD20	I/O
R1	I/O	AB1	GND	AD21	NO CONNECT
R2	I/O	AB2	I/O	AD22	I/O
R3	I/O	AB3	NO CONNECT	AD23	HDC_I/O
R4	I/O	AB4	I/O	AD24	M0
R23	I/O	AB23	M1	AD25	I/O
R24	I/O	AB24	I/O	AD26	NO CONNECT
R25	I/O	AB25	I/O	AE1	GND
R26	I/O	AB26	GND	AE2	VCC
T1	I/O	AC1	I/O	AE3	I/O
T2	I/O	AC2	NO CONNECT	AE4	NO CONNECT
T3	NO CONNECT	AC3	BUFGP_BR_ GCK5_I/O	AE5	I/O
T4	NO CONNECT			AE6	I/O
T23	I/O	AC4	&&&&	AE7	I/O
T24	NO CONNECT	AC5	BUFGS_BR_ GCK4_I/O	AE8	I/O
T25	I/O			AE9	I/O
T26	I/O	AC6	NO CONNECT	AE10	NO CONNECT
U1	VCC	AC7	I/O	AE11	I/O
U2	I/O	AC8	VCC	AE12	I/O
U3	I/O	AC9	I/O	AE13	I/O
U4	I/O_FCLK3	AC10	I/O	AE14	I/O
U23	I/O_FCLK2	AC11	NO CONNECT	AE15	I/O
U24	I/O	AC12	I/O	AE16	I/O
U25	NO CONNECT	AC13	I/O	AE17	I/O
U26	VCC	AC14	VCC	AE18	I/O
V1	&&&_I/O	AC15	I/O	AE19	I/O
V2	D5_I/O	AC16	NO CONNECT	AE20	I/O
V3	I/O	AC17	I/O	AE21	I/O
V4	I/O	AC18	I/O	AE22	I/O
V23	I/O	AC19	I/O	AE23	&&&_I/O
V24	I/O	AC20	VCC	AE24	BUFGP_BL_ GCK3_I/O
V25	I/O	AC21	NO CONNECT		
V26	I/O	AC22	I/O	AE25	VCC
		AC23	M2	AE26	GND

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AF1	GND	AF10	VCC	AF18	I/O
AF2	GND	AF11	I/O	AF19	GND
AF3	I/O	AF12	I/O	AF20	I/O
AF4	I/O	AF13	GND	AF21	I/O
AF5	GND	AF14	&&&&_I/O	AF22	GND
AF6	I/O	AF15	I/O	AF23	I/O
AF7	I/O	AF16	I/O	AF24	I/O
AF8	GND	AF17	VCC	AF25	GND
AF9	I/O			AF26	GND

THE END OF CASE (U) IS ABOVE - THE START OF CASE (T) IS BELOW

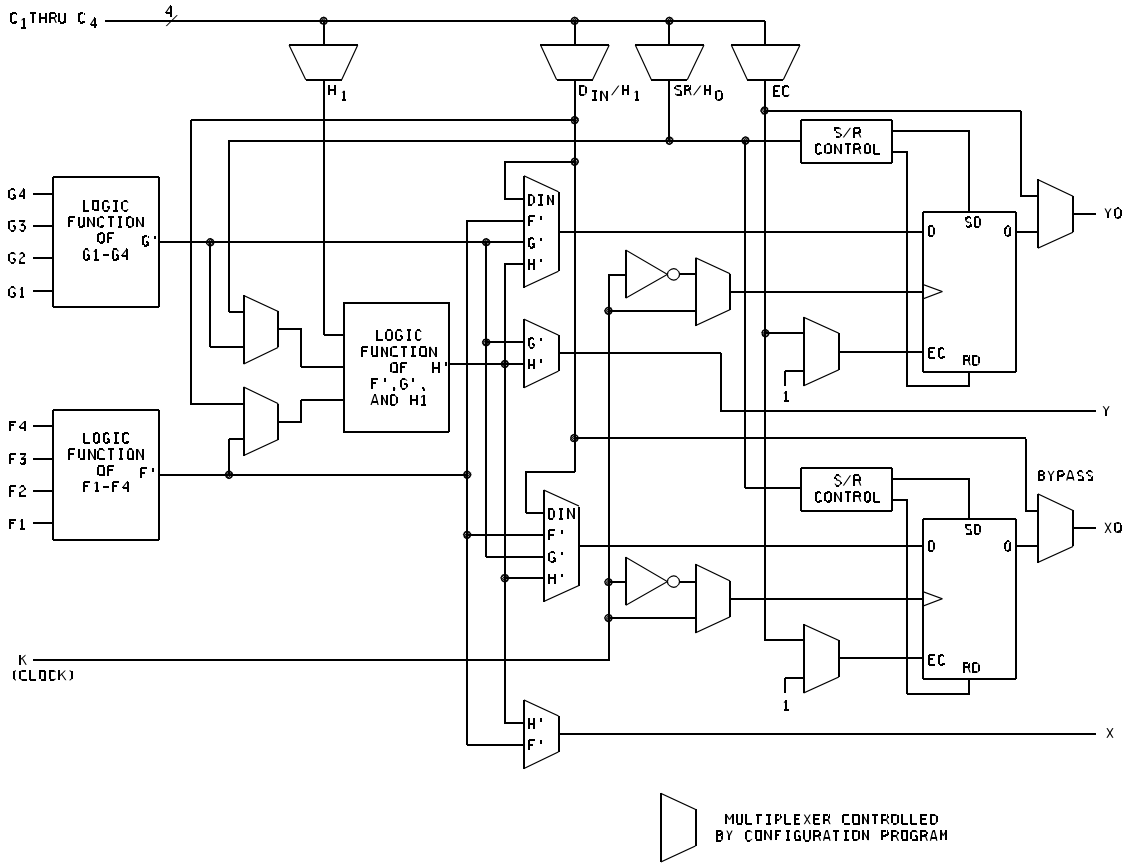
Device type	All	Device type	All	Device type	All
Case outline	T	Case outline	T	Case outline	T
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P1	VSS	P36	I/O	P70	I/O
P2	BUFGP_TL_A16 _GCK1_I/O	P37	VSS	P71	I/O
		P38	I/O	P72	I/O
P3	A17_I/O	P39	I/O	P73	I/O
P4	I/O	P40	VCC	P74	I/O
P5	I/O	P41	I/O	P75	VSS
P6	TDI_I/O	P42	I/O	P76	I/O
P7	TCK_I/O	P43	I/O	P77	I/O
P8	I/O	P44	I/O_FCLK2	P78	I/O
P9	I/O	P45	VSS	P79	I/O
P10	I/O	P46	I/O	P80	VCC
P11	I/O	P47	I/O	P81	I/O
P12	I/O	P48	I/O	P82	I/O
P13	I/O	P49	I/O	P83	VSS
P14	VSS	P50	I/O	P84	I/O
P15	I/O_FCLK1	P51	I/O	P85	I/O
P16	I/O	P52	I/O	P86	I/O
P17	TMS_I/O	P53	I/O	P87	I/O
P18	I/O	P54	I/O	P88	I/O
P19	VCC	P55	I/O	P89	&&&&_I/O
P20	I/O	P56	I/O	P90	VCC
P21	I/O	P57	BUFGS_BL_	P91	VSS
P22	VSS		GCK2_I/O	P92	I/O
P23	I/O	P58	M1	P93	I/O
P24	I/O	P59	VSS	P94	I/O
P25	I/O	P60	M0	P95	I/O
P26	I/O	P61	VCC	P96	I/O
P27	I/O	P62	M2	P97	I/O
P28	I/O	P63	BUFGP_BL_	P98	VSS
P29	VSS		GCK3_I/O	P99	I/O
P30	VCC	P64	HDC_I/O	P100	I/O
P31	I/O	P65	I/O	P101	VCC
P32	I/O	P66	I/O	P102	I/O
P33	I/O	P67	I/O	P103	I/O
P34	I/O	P68	&&&_I/O	P104	I/O
P35	I/O	P69	I/O	P105	I/O

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	T	Case outline	T	Case outline	T
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P106	VSS	P151	VSS	P195	I/O
P107	I/O	P152	D3_I/O	P196	VSS
P108	I/O	P153	&&_I/O	P197	I/O
P109	I/O	P154	I/O	P198	I/O
P110	I/O	P155	I/O	P199	I/O
P111	I/O	P156	I/O	P200	I/O
P112	I/O	P157	I/O	P201	VCC
P113	I/O	P158	VSS	P202	A4_I/O
P114	I/O	P159	D2_I/O	P203	A5_I/O
P115	I/O	P160	I/O	P204	GND
P116	I/O	P161	VCC	P205	I/O
P117	I/O	P162	I/O	P206	I/O
P118	BUFGS_BR_GCK4_I/O	P163	I/O_FCLK4	P207	A21_I/O
		P164	I/O	P208	A20_I/O
P119	VSS	P165	I/O	P209	A6_I/O
P120	DONE	P166	VSS	P210	A7_I/O
P121	VCC	P167	I/O	P211	VSS
P122	&&&&	P168	I/O	P212	VCC
P123	D7_I/O	P169	I/O	P213	A8_I/O
P124	BUFGP_BR_GCK5_I/O	P170	I/O	P214	A9_I/O
		P171	I/O	P215	A19_I/O
P125	I/O	P172	I/O	P216	A18_I/O
P126	I/O	P173	D1_I/O	P217	I/O
P127	I/O	P174	RDY_&&&&_	P218	I/O
P128	I/O		&&&&_I/O	P219	GND
P129	D6_I/O	P175	I/O	P220	A10_I/O
P130	I/O	P176	I/O	P221	A11_I/O
P131	I/O	P177	D0_DIN_I/O	P222	VCC
P132	I/O	P178	BUFGS_TR_	P223	I/O
P133	I/O		GCK6_DOUT_I/O	P224	I/O
P134	I/O	P179	CCLK	P225	I/O
P135	VSS	P180	VCC	P226	I/O
P136	I/O	P181	TDO	P227	VSS
P137	I/O	P182	VSS	P228	I/O
P138	I/O_FCLK3	P183	A0_&&_I/O	P229	I/O
P139	I/O	P184	BUFGP_TR_	P230	I/O
P140	VCC		GCK7_A1_I/O	P231	I/O
P141	D5_I/O	P185	I/O	P232	A12_I/O
P142	&&&_I/O	P186	I/O	P233	A13_I/O
P143	VSS	P187	CSI_A2_I/O	P234	I/O
P144	I/O	P188	A3_I/O	P235	I/O
P145	I/O	P189	I/O	P236	I/O
P146	I/O	P190	I/O	P237	I/O
P147	I/O	P191	I/O	P238	A14_I/O
P148	D4_I/O	P192	I/O	P239	BUFGS_TL_GCK8_A15_I/O
P149	I/O	P193	I/O		
P150	VCC	P194	I/O	P240	VCC

FIGURE 2. Terminal connections - Continued.

Simplified block diagram of CLB



Note: The CLB storage elements can also be configured as latches. The two latches have common clock (CK) and clock enable (EC) inputs. (RAM and Carry logic functions not shown)

FIGURE 3. Logic block diagrams.

Fast Carry Logic

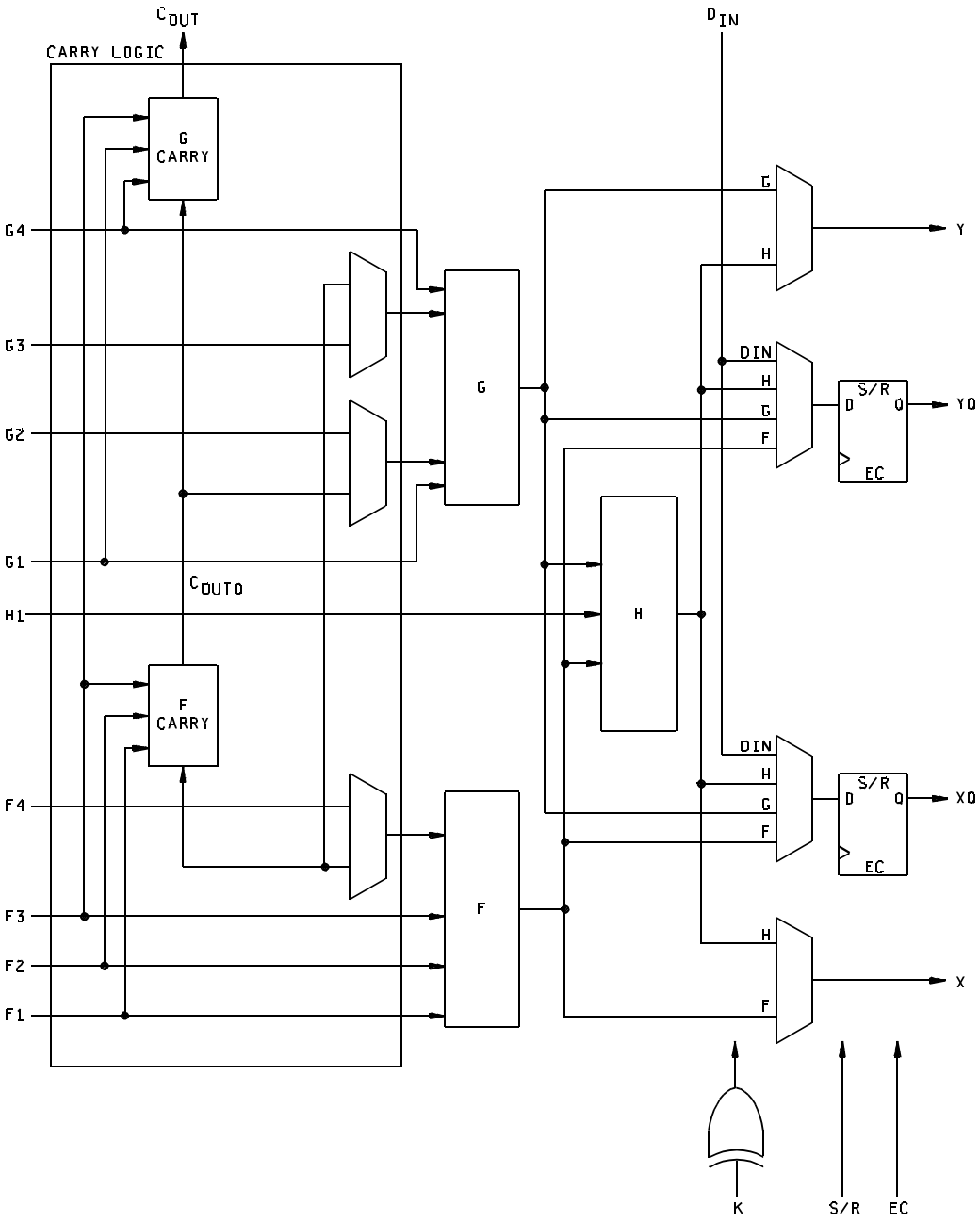


FIGURE 3. Logic block diagrams - Continued.

Simplified block diagram of IOB

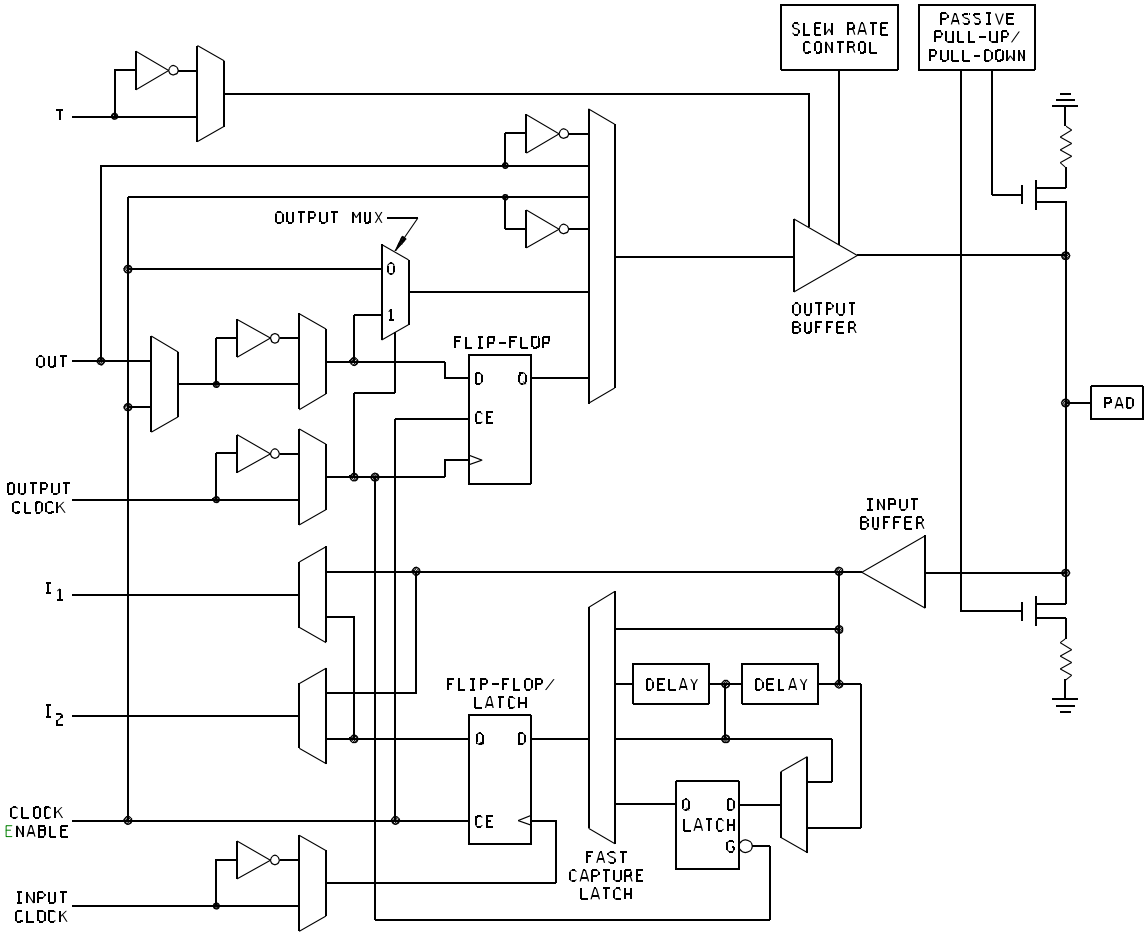
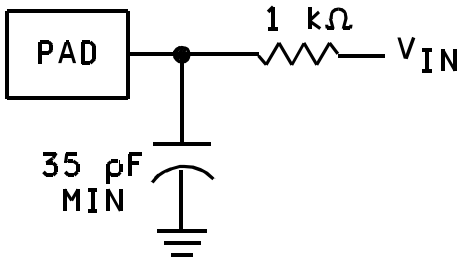
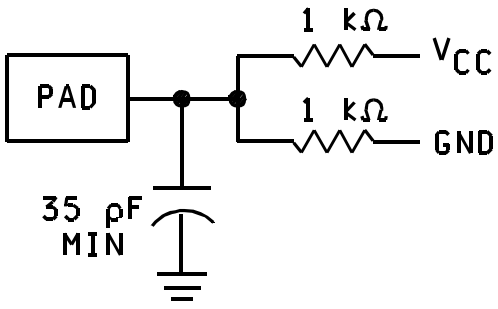


FIGURE 3. Logic block diagrams - Continued.



CIRCUIT A



CIRCUIT B

FIGURE 4. Load circuits.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and the device manufacturers QM plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes N, Q, and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

(1) The following shall apply to device class N only. Sample size is five devices with no failures. For C_{IN} and C_{OUT}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125EC, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class M	Device class N	Device class Q	Device class V
1	Interin electrical parameters (see 4.2)				1, 7, 9
2	Static burn-in I and II (method 1015)	Required	Not Required	Required	Required
3	Same as line 1				1*, 7*)
4	Dynamic burn-in (method 1015)	Not Required	Not Required	Not Required	Required
5	Same as line 1				1*, 7*)
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	2, 8A, 10	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test parameters	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	2, 8A, 10	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11)
9	Group D end-point electrical parameters	2, 3, 8A, 8B		2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9		1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/) indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB Delta limits at +25

Parameter 1/	Device types
	All
ICCO standby	± 1 mA of specified limit in table I.
IL	± 1 µA of specified limit in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25EC ±5EC, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331.

V_{CC} ---------- V SUPPLY VOLTAGE.
GND ---------- GROUND
CCLK ---------- CONFIGURATION CLOCK
DONE ---------- DONE
PROGRAM ---------- PROGRAM
RCLK ---------- READ CLOCK.
M0 ---------- MODE 0
M1 ---------- MODE 1
M2 ---------- MODE 2

6.5 Abbreviations, symbols, and definitions - Continued.

TDO	TEST DATA OUTPUT
TDI	TEST DATA IN
TCK	TEST CLOCK
TMS	TEST MODE SELECT
HDC	HIGH DURING CONFIGURATION
LDC	LOW DURING CONFIGURATION
RTRIG	READ TRIGGER.
INIT	INIT
GCK1-GCK8	GLOBALLow-Skew buffer
CSO	CHIP SELECT, WRITE
CS1	CHIP SELECT, WRITE
WS	WRITE STROBE
RS	READ STROBE
A0-A21	ADDRESS
D0-D7	DATA
DIN	DATA INPUT
DOUT	DATA OUTPUT
I/O	INPUT/OUTPUT
RDY/BUSY	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written into it. After configuration is complete, this pin becomes a user programmed I/O pin.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional operating data.

a. Power on delay is 2^{14} cycles from the non-master mode. This provides 11 to 33 ms of wait time.

b. Power on delay is 2^{16} cycles for the master mode. This provides 43 to 130 ms of wait time.

c. Clear is 375 cycles ±25 cycles and may take as long as 250 to 750 µs.

d. During normal power up, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 10 ms. If this does not occur, configuration must be delayed by using RESET.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 1998-NOV-06

Approved sources of supply for SMD 5962-98509 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revisions. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9850901QXC	68994	XQ4028EX-4PG299B
5962-9850901QYC	68994	XQ4028EX-4CB228B
5962-9850901QZC	68994	XQ4028EX-4CB228B
5962-9850901NUA	68994	XQ4028EX-4BG352N
5962-9850901NTB	68994	XQ4028EX-4HQ240N

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124