NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE *(YYMMDD)* 96-10-04

Form Approved
OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME *(First, Middle Initial, Last)*

b. ADDRESS *(Street, City, State, Zip Code)*
Defense Supply Center Columbus
3990 Broad Street
Columbus,OH 43216-5000

5. CAGE CODE 67268

6. NOR NO. 5962-R007-97

7. CAGE CODE 67268

8. DOCUMENT NO. **5962-92305**

9. TITLE OF DOCUMENT
MICROCIRCUIT, MEMORY, DIGITAL CMOS, PROGRAMMABLE LOGIC CELL ARRAY, MONOLITHIC SILICON

10. REVISION LETTER
a. CURRENT C
b. NEW D

11. ECP NO.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: **Revisions ltr column; add "D".**
Revisions description column; add "Changes in accordance with NOR 5962-R007-97".
Revisions date column; add "96-10-04".
Rev status above sheet numbers 1 and 15, delete "C", and add "D".
Revision level block; delete "C", and add "D".

Sheet 15: **Table I, footnote 6/ Delete the last sentence of this footnote and replace it with the following:**
"Characterization data is taken initially and after any design or process change which may affect this parameter."
Revision level block; delete "C", and add "D".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*
☒ (1) Existing document supplemented by the NOR may be used in manufacture.
☐ (2) Revised document must be received before manufacturer may incorporate this change.
☐ (3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT
DSCC-VAS

c. TYPED NAME *(First, Middle Initial, Last)*
Ray Monnin

d. TITLE
Microelectronics Team Chief

e. SIGNATURE
Ray Monnin

f. DATE SIGNED *(YYMMDD)*
96-10-04

15a. ACTIVITY ACCOMPLISHING REVISION
DSCC-VAS

b. REVISION COMPLETED *(Signature)*
Kenneth S. Rice

c. DATE SIGNED *(YYMMDD)*
96-10-04

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added changes in accordance with NOR 5962-R148-94.	94-04-21	M. A. Frye
B	Added changes in accordance with NOR 5962-R155-945	95-06-16	M. A. Frye
C	Added device type 03. Editorial changes throughout document.	95-09-26	M. A. Frye

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS OF SHEETS			REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
			SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
RAJESH PITHADIA

CHECKED BY
KENNETH RICE

APPROVED BY
MICHAEL FRYE

DRAWING APPROVAL DATE
93-10-22

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
DAYTON, OHIO 43216

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 10000 GATE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-92305**

SHEET 1 OF 34

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

```
    5962          -          92305     01          M           X          X
      |           |                     |          |           |          |
      |           |                     |          |           |          |
  ____|____   ____|____            _____|_____  ___|_____   ___|____   ___|___
   Federal       RHA                 Device      Device       Case       Lead
 stock class  designator              type        class      outline    finish
 designator   (See 1.2.1)         (See 1.2.2)  designator  (See 1.2.4) (See 1.2.5)
\__________________ __________________/        (See 1.2.3)
                   \/
             Drawing number
```

1.2.1 Radiation hardness assurance (RHA) designator. Device classes M RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	4010-10	10000 gate programmable array	10 ns
02	4010-6	10000 gate programmable array	6 ns
03	4010-5	10000 gate programmable array	4.5 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outlines shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA10-PN	191 1/	Pin grid array package
Y	see figure 1	196	Unformed-lead chip carrier
Z	CQCC1-F196	196	Unformed-lead chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ 191 = actual number of pins used, not maximum listed in MIL-STD-1835.

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to V_{CC} +5.0 V dc
Voltage applied to three-state output(V_{IS})	-0.5 V dc to V_{CC} +5.0 V dc
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines X, Y, and Z	See MIL-STD-1835
Junction temperature (T_J)	+150° C 3/
Lead temperature (soldering, 10 seconds)	+260° C
Storage temperature range	-65° C to +150° C

1.4 Recommended operating conditions. 4/

Supply voltage relative to ground(V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Case operating temperature Range(T_C)	-65° C to +125° C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	5/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

4/ All voltage values in this drawing are with respect to GND.

5/ When a QML source exists, a value shall be provided.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17	- A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88	- Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.2.4 Logic block diagram. The logic block diagram shall be as specified in figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Serialization for device class V. Class V shall be serialized in accordance with MIL-PRF-38535.

3.12 Operational notes. Additional information shall be provided by the device manufacturer (see 6.7 herein).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Static burn-in for device class M, Q, and V (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 5.0 V + 0.5 - 0.0 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} + 0.5 - 0.0 V. R1 = 220Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 5.0 V + 0.5 V - 0.0 V minimum

(c) Ambient temperature (T_A) shall be +125°C minimum.

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\text{ V} \le V_{CC} \le 5.5\text{ V}$ $-55^\circ\text{C} \le T_C \le +125^\circ\text{C}$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8V, V_{IH} = 2.0 V	1,2,3	All	2.4		V
Low level output voltage 1/	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 4.0 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All		0.4	V
Dynamic power consumption 2/ 3/		V_{CC} = 5.5 V	1,2,3	All		2/	mW/MHz
Quiescent LCA supply current 4/	I_{CCO}	V_{CC} = V_{IN} = 5.5 V	1,2,3	All		50	mA
Input leakage current	I_{IL}	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V	1,2,3	All	-10	+10	uA
Output leakage current	I_{OL}	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V with no load	1,2,3	All	-1.0	+1.0	uA
Pad pull-up current (when selected)	I_{RIN}	V_{IN} = 0 V	1,2,3	All		0.5	mA
Horizontal long line pull-up current (when selected)	I_{RLL}	At logic low	1,2,3	All		5.0	mA
Input capacitance	C_{IN}	See 4.4.1e	4	All		16	pF
Output capacitance	C_{OUT}	See 4.4.1e	4	All		16	pF
Functional test	FT	See 4.4.1c	7,8A,8B	All			
Interconnect + t_{PID} + t_{OPS} + t_{ILO}	t_{B1}		9,10,11	01		271.5	ns
				02		168.5	
				03		128.2	
Interconnect + t_{PID} + t_{HHO} + t_{OPS}	t_{B2}		9,10,11	01		235.7	ns
				02		190.6	
				03		140.3	
Interconnect + t_{PID} + t_{OPS} + t_{IHO}	t_{B3}		9,10,11	01		351.5	ns
				02		208.5	
				03		178.2	
Interconnect + t_{PID} + t_{OPS} + tRIO	t_{B4}		9,10,11	01		375.6	ns
				02		230.6	
				03		200.3	
Interconnect + t_{CKO} + t_{ICK} + t_{CKI}	t_{B5}		9,10,11	01		22.6	ns
				02		12.6	
				03		8.8	
Interconnect + t_{CKO} + t_{HHCK} + t_{CKHH}	t_{B6}		9,10,11	01		20.7	ns
				02		13.6	
				03		9.3	
Interconnect + t_{CKO} + t_{IHCK} + tCKIH	t_{B7}		9,10,11	01		26.6	ns
				02		14.6	
				03		10.3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Interconnect + t_{CKO} + t_{DICK} + t_{CKDI}	t_{B8}		9,10,11	01		18.7	ns
				02		10.6	
				03		7.3	
Interconnect + t_{CKO} + t_{ECCK} + t_{CKEC}	t_{B9}		9,10,11	01		23.6	ns
				02		13.6	
				03		8.3	
Interconnect + t_{PID} + t_{OPS} + t_{OPCY} + t_{SUM} - t_{BYP}	t_{B10}		9,10,11	01		398.3	ns
				02		297.4	
				03		230.2	
Interconnect + t_{PID} + t_{OPS} + t_{ASCY} + t_{SUM} - t_{BYP}	t_{B11}		9,10,11	01		456.8	ns
				02		318.1	
				03		318.1	
Interconnect + t_{PID} + t_{OPS} + t_{INCY} + t_{SUM}	t_{B12}		9,10,11	01		230.1	ns
				02		175.9	
				03		128.5	
Interconnect + t_{PID} + t_{OPS} + t_{INCY} + t_{SUM} + tBYP	t_{B13}		9,10,11	01		96.9	ns
				02		70.6	
				03		52.9	
WIDE DECODER SWITCHING CHARACTERISTIC							
Full length, both pull-ups inputs from IOB I-pins	T_{WAF}	See figures 4 and 5 as applicable. 5/	3/	01,02		13	ns
				03		12	
Full length, both pull-ups inputs from internal logic	T_{WAFL}		3/	01,02		16	ns
				03		15	
Half length, one pull-up inputs from IOB i-pins	T_{WAO}		3/	01,02		13	ns
				03		12	
Half length, one pull-up inputs from internal logic	T_{WAOL}		3/	01,02		16	ns
				03		15	
CLB SWITCHING CHARACTERISTICS							
Combinatorial delay F/G inputs to X/Y outputs	T_{ILO}	See figures 4 and 5 as applicable.	6/	01		10	ns
				02		6	
				03		4.5	
Combinatorial delay F/G inputs via H' to X/Y outputs	T_{IHO}		6/	01		14	ns
				02		8	
				03		7	
Combinatorial delay C inputs via H' to X/Y outputs	T_{HHO}		6/	01		8	ns
				02		7	
				03		5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
CLB fast carry logic operand inputs (F1,F2,G1, G4) to C_{OUT}	T_{OPCY}	See figures 4 and 5, as applicable	7/	01		8	ns
				02		7	
				03		5.5	
CLB fast carry logic add/ subtract input (F3) to C_{OUT}	T_{ASCY}		7/	01		11	ns
				02		8	
				03		6	
CLB fast carry logic initialization inputs (F1,F3) to C_{OUT}	T_{INCY}		7/	01,02		6	ns
				03		4	
CLB fast carry logic C_{IN} through function generators to X/Y outputs	T_{SUM}		7/	01		12	ns
				02		8	
				03		6	
CLB fast carry logic C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		7/	01		3	ns
				02		2	
				03		1.5	
Sequential delays clock K to outputs Q	T_{CKO}		6/	01		9	ns
				02		5	
				03		3	
Set-up time before clock K, F/G inputs	T_{ICK}		6/	01	11		ns
				02	6		
				03	4.5		
Set-up time before clock K, F/G inputs via H'	T_{IHCK}		6/	01	15		ns
				02	8		
				03	6		
Set-up time before clock K, C inputs via H1	T_{HHCK}		6/	01	9		ns
				02	7		
				03	5		
Set-up time before clock K, C inputs via DIN	T_{DICK}		6/	01	7		ns
				02	4		
				03	3		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Set-up time before clock K, C inputs via EC	T_{ECCK}	See figures 4 and 5 as applicable.	6/	01	12		ns
				02	7		
				03	4		
Set-up time before clock K, C inputs via S/R, going low (inactive)	T_{RCK}		3/	01	10		ns
				02	6		
				03	4.5		
Set-up time before clock K, C_{IN} input via F'/G'	T_{CCK}		3/	01,02	8		ns
				03	6		
Set-up time before clock K C_{IN} input via F'/G' and H'	T_{CHCK}		3/	01,02	10		ns
				03	7.5		
Hold time after clock K, F/G inputs	T_{CKI}		6/	All	0		ns
Hold time after clock K, F/G inputs via H'	T_{CKIH}		6/	All	0		ns
Hold time after clock K, C inputs via H1	T_{CKHH}		6/	All	0		ns
Hold time after clock K, C inputs via DIN	T_{CKDI}		6/	All	0		ns
Hold time after clock K, C inputs via EC	T_{CKEC}		6/	All	0		ns
Hold time after clock K, C inputs via S/R, going low (inactive)	T_{CKR}		3/	All	0		ns
Clock high time	T_{CH}		3/	01	5.5		ns
				02	5		
				03	4.5		
Clock low time	T_{CL}		3/	01	5.5		ns
				02	5		
				03	4.5		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
CLB SWITCHING CHARACTERISTICS - continued.							
Set/Reset direct width (high)	T_{RPW}	See figures 4 and 5 as applicable.	3/	01	6		ns
				02	5		
				03	4		
Set/Reset direct delay from C to Q	T_{RIO}		6/	01		15	ns
				02		9	
				03		8	
Master set/reset width (high or low)	T_{MRW}		3/	01	55		ns
				02	50		
				03	45		
Master set/reset delay from global set/reset net to Q	T_{MRQ}		3/	01		78	ns
				02		74	
				03		70	
CLB SWITCHING CHARACTERISTIC (RAM OPTION)							
Read operation address read cycle time (16 X 2)	T_{RC}	See figures 4 and 5 as applicable. 8/	9/	01	12		ns
				02	7		
				03	5.5		
Read operation address read cycle time (32 X 1)	T_{RCT}		9/	01	15		ns
				02	10		
				03	7.5		
Read operation data valid after address change (no write enable) (16 X 2)	T_{ILO}		9/	01		10	ns
				02		6	
				03		4.5	
Read operation data valid after address change (no write enable) (32 X 1)	T_{IHO}		9/	01		14	ns
				02		8	
				03		7	
Read during write, clocking data into flipflop address setup time before clock (32 x 1)	T_{ICK}		9/	01	11		ns
				02	6		
				03	4.5		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Read during write, clocking data into flip flop address setup time before clock K (32 X 1)	T_{IHCK}		9/	01	15		ns
				02	8		
				03	6		
Read during write data valid after WE going active (16 X 2)	T_{WO}		9/	01		15	ns
				02		12	
				03		10	
Read during write DIN stable before WE (32 X 1)	T_{WOT}		9/	01		27	ns
				02		15	
				03		12	
Read during write data valid after DIN (16 X 2)	T_{DO}		9/	01		19	ns
				02		11	
				03		9	
Read during write (DIN change during WE) (32 X 1)	T_{DOT}		9/	01		22	ns
				02		14	
				03		11	
Read during write, clocking data into flip flop, WE setup time before clock K (16 X 2)	T_{WCK}		9/	01	15		ns
				02	12		
				03	10		
Read during write, clocking data into flip flop WE setup time before clock K (32 X 1)	T_{WCKT}		9/	01	27		ns
				02	15		
				03	12		
Read during write, clocking data into flip flop data setup time before clock K (16 X 2)	T_{DCK}		9/	01	19		ns
				02	11		
				03	9		
Read during write, clocking data into flip flop data setup time before clock K (32 X 1)	T_{DCKT}		9/	01	22		ns
				02	14		
				03	11		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Write operation address write cycle time (16 X 2)	T_{WC}	See figures 4 and 5 as applicable. 8/	9/	01	16		ns
				02	9		
				03	8		
Write operation address write cycle time (32 X 1)	T_{WCT}		9/	01	16		ns
				02	9		
				03	8		
Write operation write enable pulse width (high) (16 X 2)	T_{WP}		9/	01	12		ns
				02	5		
				03	4		
Write operation write enable pulse width (high) (32 X 1)	T_{WPT}		9/	01	12		ns
				02	5		
				03	4		
Write operation address setup time before beginning of WE (16 X 2)	T_{AS}		9/	All	2		ns
Write operation address setup time before beginning of WE (32 X 1)	T_{AST}		9/	All	2		ns
Write operation, address hold time after end of WE (16 X 2)	T_{AH}		9/	All		2	ns
Write operation, address hold time after end of WE (32 X 1)	T_{AHT}		9/	All		2	ns
Write operation DIN setup time before end of WE (16 X 2)	T_{DS}		9/	All	4		ns
Write operation DIN setup time before end of WE (32 X 1)	T_{DST}		9/	All	5		ns
Write operation DIN hold time after end of WE	T_{DHT}		9/	All		2	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
IOB SWITCHING CHARACTERISTIC							
Input propagation delay pad to I1, I2	T_{PID}	See figures 4 and 5 as applicable. 10/ 11/	6/	01,02		4	ns
				03		3	
Input propagation delay pad to I1, I2, via transparent latch (fast)	T_{PLI}		3/	01		13	ns
				02		8	
				03		7	
Input propagation delay pad to I1, I2, via transparent latch (with delay)	T_{PDLI}		3/	01		30	ns
				02		26	
				03		24	
Input propagation delay clock (IK) to I1, I2, (flip-flop)	T_{IKRI}		3/	01		8.5	ns
				02		8	
				03		7	
Input propagation delay clock (IK) to I1, I2, (latch enable)	T_{IKLI}		3/	01		9	ns
				02		8	
				03		7	
Setup time, pad to clock (IK), fast	T_{PICK}	See figures 4 and 5 as applicable. 10/ 11/ 12/	3/	01	9		ns
				02	7		
				03	6		
Setup time pad to clock (IK), with delay	T_{PICKD}		3/	01	35		ns
				02	25		
				03	24		
Hold time pad to clock (IK), fast	T_{IKPI}		3/	All		1	ns
Hold time pad to clock (IK), with delay	T_{IKPID}		3/	All		negative	ns
Output propagation delay clock (OK) to pad (fast)	T_{OKPOF}	See figures 4 and 5 as applicable. 10/ 11/	3/	01		11	ns
				02		7.5	
				03		7	
Output propagation delay clock (OK) to pad (slew-rate limited)	T_{OKPOS}		3/	01		16	ns
				02		11.5	
				03		10	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \le V_{CC} \le 5.5\text{ V}$ $-55^\circ\text{C} \le T_C \le +125^\circ\text{C}$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Output propagation delay output (O) to pad (fast)	T_{OPF}	See figures 4 and 5 as applicable. 10/ 11/	3/	01		10	ns
				02		9	
				03		7	
Output propagation delay output (O) to pad (slew rate limited)	T_{OPS}		6/	01		15	ns
				02		13	
				03		10	
Output propagation delay 3-state to pad begin hi-z (fast)	T_{TSHZF}		3/	01		10	ns
				02		9	
				03		7	
Output propagation delay 3-state to pad active and valid (fast)	T_{TSONF}		3/	01		15	ns
				02		13	
				03		10	
Output propagation delay 3-state to pad active and valid (slew rate limited)	T_{TSONS}		3/	01		20	ns
				02		17	
				03		13	
Setup time, output (O) to clock (OK)	T_{OOK}		3/	01	13		ns
				02	8		
				03	6		
Hold time, output (O) to clock (OK)	T_{OKO}		3/	All		0	ns
Clock high or low time	T_{CH}/ T_{CL}		3/	01	6		ns
				02	5		
				03	4.5		
Global set/reset delay from GSR net through Q to I1, I2	T_{RRI}		3/	01		20	ns
				02		14.5	
				03		13.5	
Global set/reset delay from GSR net to pad	T_{RPO}		3/	01		23	ns
				02		18	
				03		17	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \le V_{CC} \le 5.5\text{ V}$ $-55^\circ\text{C} \le T_C \le +125^\circ\text{C}$ unless otherwise specified	Group A Subgroups	Device type	Limits Min	Limits Max	Unit
Global set/reset GSR width	T_{MRW}	See figures 4 and 5 as applicable. 10/ 11/	5/	01,02	21		ns
				03	18		

1/ With 50 percent of the outputs or 64 pins maximum for any device simultaneously sinking 4 mA.

2/ 1 CLB driving 3 local interconnects ---------------- 0.30 mW/MHz max. at 50 MHz max.
1 device output with a 50 pF load ------------------ 1.20 mW/MHz max. at 50 MHz max.
1 global clock buffer and line --------------------- 5.10 mW/MHz max. at 50 MHz max.
1 half longline without driver --------------------- 0.24 mW/MHz max. at 50 MHz max.

3/ Parameter is not tested but is guaranteed by characterization data which is taken at initial device introduction, prior to the introduction of significant changes, and at least twice yearly.

4/ With no output current loads, no active input or long line pull-resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits "tie" option.

5/ These delays are specified from the decoder input to the decoder output. For pad-to-pad delays, add the input delay (T_{PID}) and output delay (TOPF or TOPS).

6/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark patterns (t_{B1} - t_{B13}) are then used to determine the compliance of this parameter. Characterization data is taken at initial device introduction, prior to the introduction of significant changes, and at least twice yearly to monitor correlation between benchmark patterns and this parameter.

7/ Benchmark patterns (t_{B1} - t_{B13}) are used to determine compliance of this parameter.

8/ Timing for the 16 X 1 RAM option is identical to 16 X 2 RAM timing.

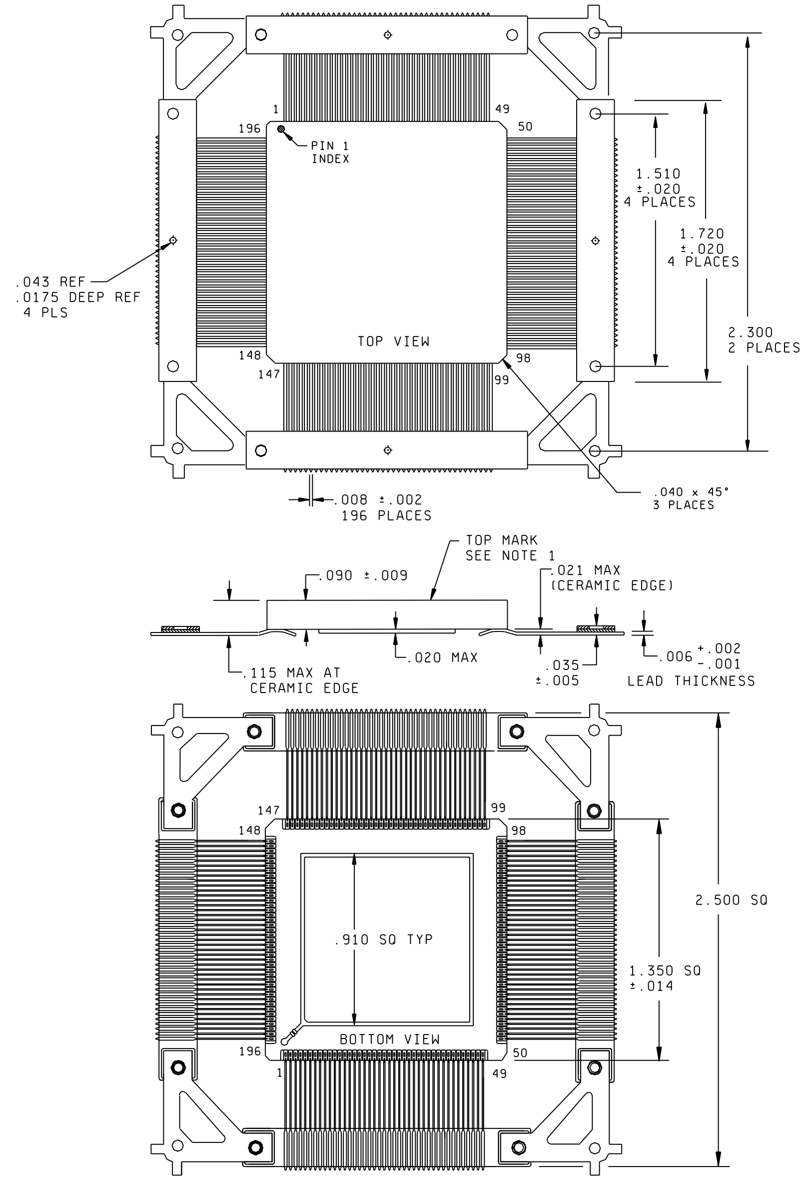
9/ Values indicated are guaranteed by characterization data if application note, provided by manufacturer, is followed. If application note is not followed, indicated values are typical only.

10/ Timing is measured at pin threshold, with 50 pF external capacitive loads including test fixture. Slew rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs this total is two times larger. Exceeding this maximum capacitive load can result in ground bounce of greater than 1.5 V amplitude, less than 5 ns duration, which might cause problems when the LCA drives clocks and other asynchronous signals.

11/ Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor or alternatively configured as a driven output or be driven from an external source.

12/ Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero. "Negative" hold time means that the delay in the input data is adequate for the external system hold time to be zero, provided the input clock uses the global signal distribution from pad to IK.

Case Y



NOTE:

1. Package has top marking on non-lid side, therefore, pin out goes clockwise when device is mounted with lid in down position. The Z package is just like this package except the top marking is on the traditional lid side and when mounted with the lid up, the pin out goes counter clockwise.

FIGURE 1. Case outline.

Case Y

Inches	mm	Inches	mm
.001	0.02	.043	1.09
.002	0.05	.090	2.29
.005	0.13	.115	2.92
.006	0.15	.910	23.11
.008	0.20	1.350	34.29
.009	0.23	1.510	38.35
.014	0.36	1.720	43.69
.0175	0.44	2.300	58.42
.020	0.51	2.500	63.50
.021	0.53		
.035	0.89		
.040	1.02		

NOTE: The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline - Continued.

Case outline X

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A2	I/O (TD1)		C2	I/O (A14)		F16	I/O
A3	I/O		C3	PGCK1 (A16, I/O)		F17	I/O
A4	I/O		C4	I/O (A17)		F18	I/O
A5	I/O		C5	I/O		G1	I/O (A10)
A6	I/O		C6	I/O		G2	I/O (A11)
A7	I/O		C7	GND		G3	GND
A8	I/O		C8	I/O		G16	GND
A9	I/O		C9	I/O		G17	I/O
A10	I/O		C10	I/O		G18	I/O
A11	I/O		C11	I/O		H1	I/O
A12	I/O		C12	GND		H2	I/O
A13	I/O		C13	I/O		H3	I/O
A14	I/O		C14	I/O		H16	I/O
A15	I/O		C15	M1		H17	I/O
A16	I/O		C16	M2		H18	I/O
A17	I/O		C17	I/O		J1	I/O
A18	MO		C18	I/O		J2	I/O (A9)
B1	I/O		D1	I/O		J3	I/O (A8)
B2	SGCK1 (A15, I/O)		D2	I/O (A13)		J4	V_{CC}
B3	I/O		D3	V_{CC}		J15	V_{CC}
B4	I/O (TCK)		D4	GND		J16	I/O ($\overline{ERR}$, $\overline{INIT}$)
B5	I/O		D9	GND		J17	I/O
B6	I/O		D10	V_{CC}		J18	I/O
B7	I/O (TMS)		D15	GND		K1	I/O
B8	I/O		D16	V_{CC}		K2	I/O (A6)
B9	I/O		D17	I/O		K3	I/O (A7)
B10	I/O		D18	I/O		K4	GND
B11	I/O		E1	I/O		K15	GND
B12	I/O		E2	I/O		K16	I/O
B13	I/O		E3	I/O		K17	I/O
B14	I/O		E16	I/O (HDC)		K18	I/O
B15	I/O		E17	I/O (LDC)		L1	I/O
B16	SGCK2 (I/O)		E18	I/O		L2	I/O
B17	PGCK2 (I/O)		F1	I/O		L3	I/O
B18	I/O		F2	I/O		L16	I/O
C1	I/O		F3	I/O (A12)		L17	I/O

NC = NO CONNECT

FIGURE 2. Terminal connections.

Case outline X - Continued.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
L18	I/O		R17	I/O		U8	I/O
M1	I/O (A5)		R18	I/O		U9	I/O ($\overline{RS}$)
M2	I/O (A4)		T1	I/O		U10	I/O (D4)
M3	GND		T2	I/O ($\overline{CS1}$, A2)		U11	I/O
M16	GND		T3	I/O (A0, $\overline{WS}$)		U12	I/O (D5)
M17	I/O		T4	SGCK4 (I/O)-DOUT		U13	I/O
M18	I/O		T5	I/O		U14	I/O
N1	I/O		T6	I/O		U15	I/O
N2	I/O		T7	GND		U16	PGCK3 (I/O)
N3	I/O (A3)		T8	I/O		U17	DONE
N16	I/O		T9	I/O (D3)		U18	I/O
N17	I/O		T10	I/O		V1	CCLK
N18	I/O		T11	I/O		V2	I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)
P1	I/O		T12	GND		V3	I/O (D1)
P2	I/O		T13	I/O		V4	I/O
P3	I/O		T14	I/O		V5	I/O
P16	I/O		T15	I/O (D7)		V6	I/O
P17	I/O		T16	SGCK3 (I/O)		V7	I/O (D2)
P18	I/O		T17	I/O		V8	I/O
R1	I/O		T18	I/O		V9	I/O
R2	I/O		U1	PGCK4 (I/O, A1)		V10	I/O
R3	GND		U2	TD0		V11	I/O
R4	V_{CC}		U3	I/O (D0, DIN)		V12	I/O ($\overline{CS0}$)
R9	GND		U4	I/O		V13	I/O
R10	V_{CC}		U5	I/O		V14	I/O
R15	V_{CC}		U6	I/O		V15	I/O
R16	GND		U7	I/O		V16	I/O
						V17	I/O (D6)
						V18	$\overline{PROG}$

NC = NO CONNECT

FIGURE 2. Terminal connections - Continued.

Case outline Y and Z

Device type	All	Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	37	I/O	73	I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)
2	PGCK1 (A16, I/O)	38	I/O	74	V_{CC}
3	I/O (A17)	39	I/O	75	GND
4	I/O	40	I/O	76	I/O
5	NC	41	I/O	77	I/O
6	I/O	42	I/O	78	I/O
7	I/O (TDI)	43	I/O	79	I/O
8	I/O (TCK)	44	I/O	80	I/O
9	I/O	45	I/O	81	I/O
10	I/O	46	SGCK2 (I/O)	82	I/O
11	I/O	47	M1	83	I/O
12	I/O	48	GND	84	I/O
13	GND	49	M0	85	I/O
14	I/O	50	V_{CC}	86	GND
15	I/O	51	M2	87	I/O
16	I/O (TMS)	52	PGCK2 (I/O)	88	I/O
17	I/O	53	I/O (HDC)	89	I/O
18	I/O	54	NC	90	I/O
19	I/O	55	I/O	91	I/O
20	I/O	56	I/O	92	I/O
21	I/O	57	I/O	93	I/O
22	I/O	58	I/O (LDC)	94	I/O
23	I/O	59	I/O	95	I/O
24	GND	60	I/O	96	SGCK3 (I/O)
25	V_{CC}	61	I/O	97	GND
26	I/O	62	I/O	98	DONE
27	I/O	63	GND	99	V_{CC}
28	I/O	64	I/O	100	$\overline{\text{PROG}}$
29	I/O	65	I/O	101	I/O (D7)
30	I/O	66	I/O	102	PGCK3 (I/O)
31	I/O	67	I/O	103	NC
32	I/O	68	I/O	104	I/O
33	I/O	69	I/O	105	I/O
34	I/O	70	I/O	106	I/O (D6)
35	I/O	71	I/O	107	I/O
36	GND	72	I/O	108	I/O

NC = NO CONNECT

FIGURE 2. Terminal connections - Continued.

Case outlines Y and Z - Continued.

Device type	All	Device type	All	Device type	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
109	I/O	140	I/O (D1)	171	I/O (A7)
110	I/O	141	I/O ($\overline{\text{RCLK}}$-$\overline{\text{BUSY}}$/RDY)	172	GND
111	I/O	142	I/O	173	V_{CC}
112	GND	143	I/O	174	I/O (A8)
113	I/O	144	I/O (D0, DIN)	175	I/O (A9)
114	I/O	145	SGCK4 (I/O)-DOUT	176	I/O
115	I/O (D5)	146	CCLK	177	I/O
116	I/O ($\overline{\text{CS0}}$)	147	V_{CC}	178	I/O
117	I/O	148	TD0	179	I/O
118	I/O	149	GND	180	I/O (A10)
119	I/O	150	I/O (A0, $\overline{\text{WS}}$)	181	I/O (A11)
120	I/O	151	PGCK4 (I/O, A1)	182	I/O
121	I/O (D4)	152	NC	183	I/O
122	I/O	153	I/O	184	GND
123	V_{CC}	154	I/O	185	I/O
124	GND	155	I/O ($\overline{\text{CS1}}$, A2)	186	I/O
125	I/O (D3)	156	I/O (A3)	187	I/O
126	I/O ($\overline{\text{RS}}$)	157	I/O	188	I/O
127	I/O	158	I/O	189	I/O (A12)
128	I/O	159	I/O	190	I/O (A13)
129	I/O	160	I/O	191	I/O
130	I/O	161	GND	192	NC
131	I/O (D2)	162	I/O	193	I/O
132	I/O	163	I/O	194	I/O (A14)
133	I/O	164	I/O (A4)	195	SGCK1 (A15, I/O)
134	I/O	165	I/O (A5)	196	V_{CC}
135	GND	166	I/O		
136	I/O	167	I/O		
137	I/O	168	I/O		
138	I/O	169	I/O		
139	I/O	170	I/O (A6)		

NC = NO CONNECT

FIGURE 2. Terminal connections - Continued.

I/O BLOCK

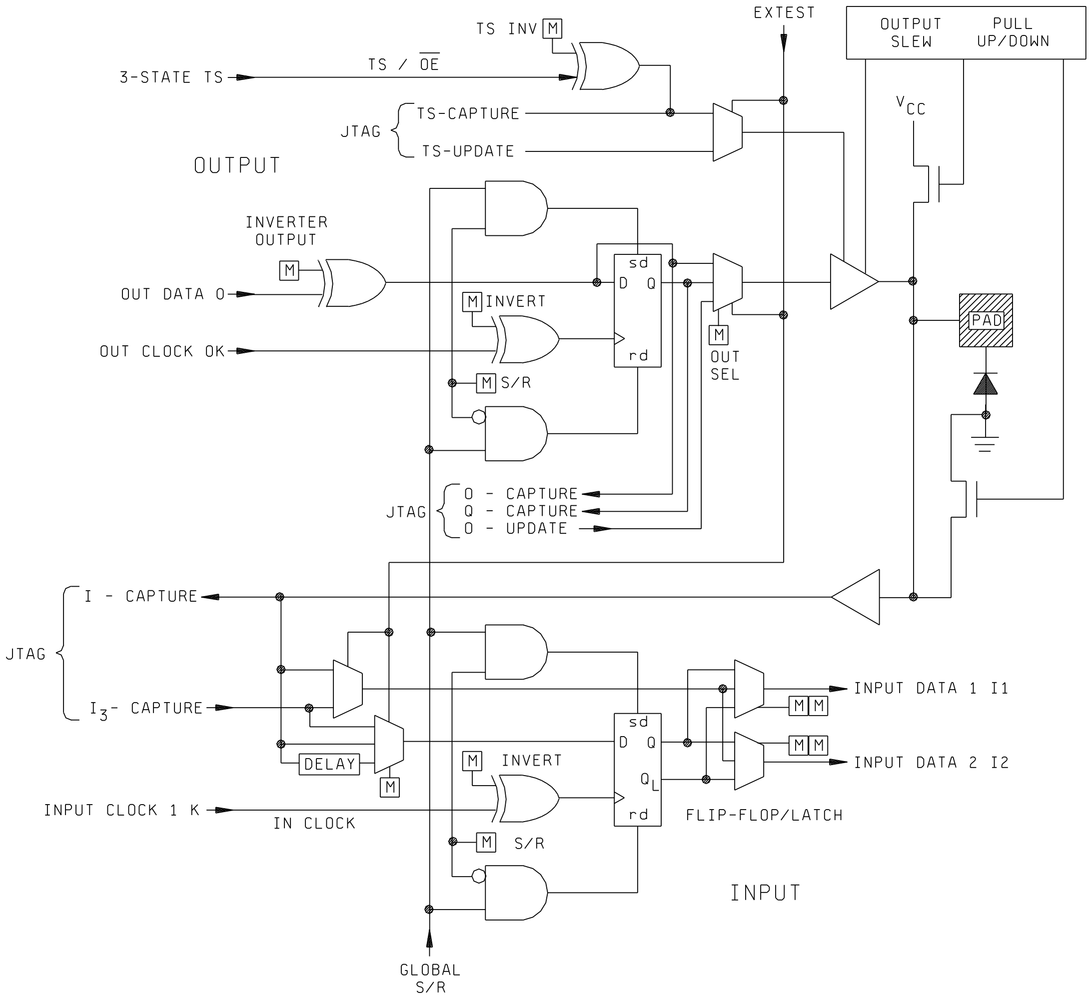


FIGURE 3. Logic block diagram.

CONFIGURABLE LOGIC BLOCK (CLB)

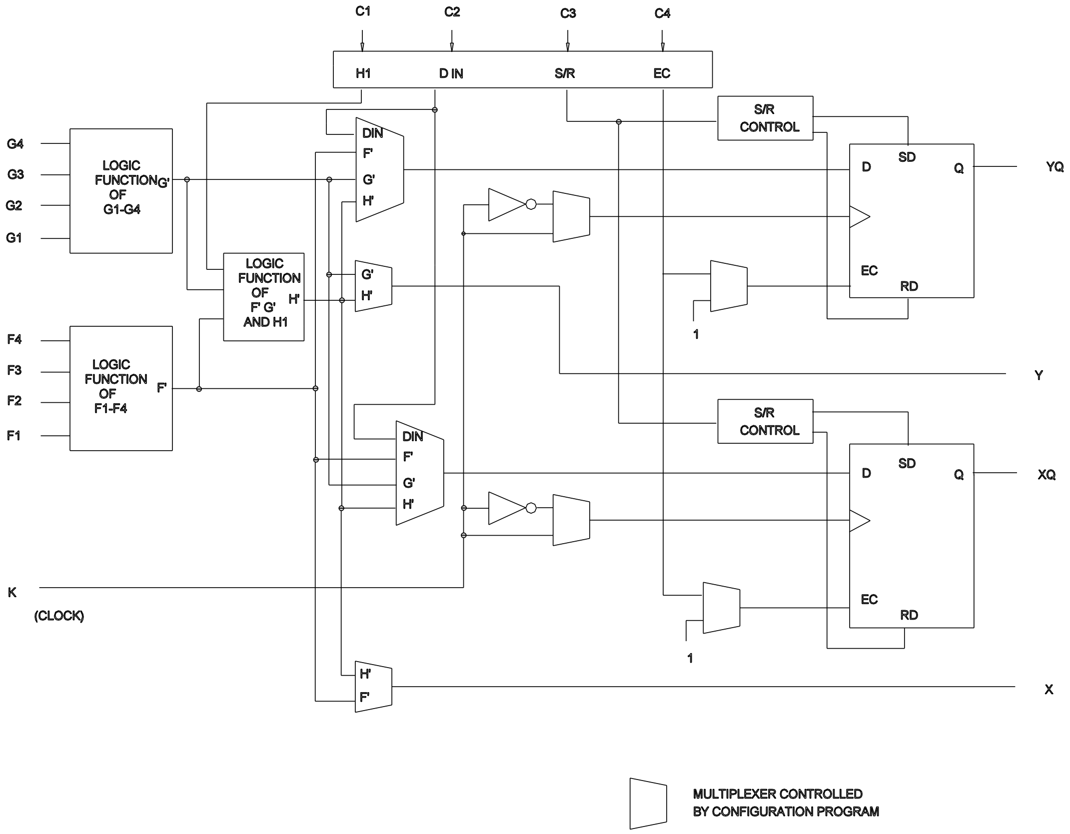
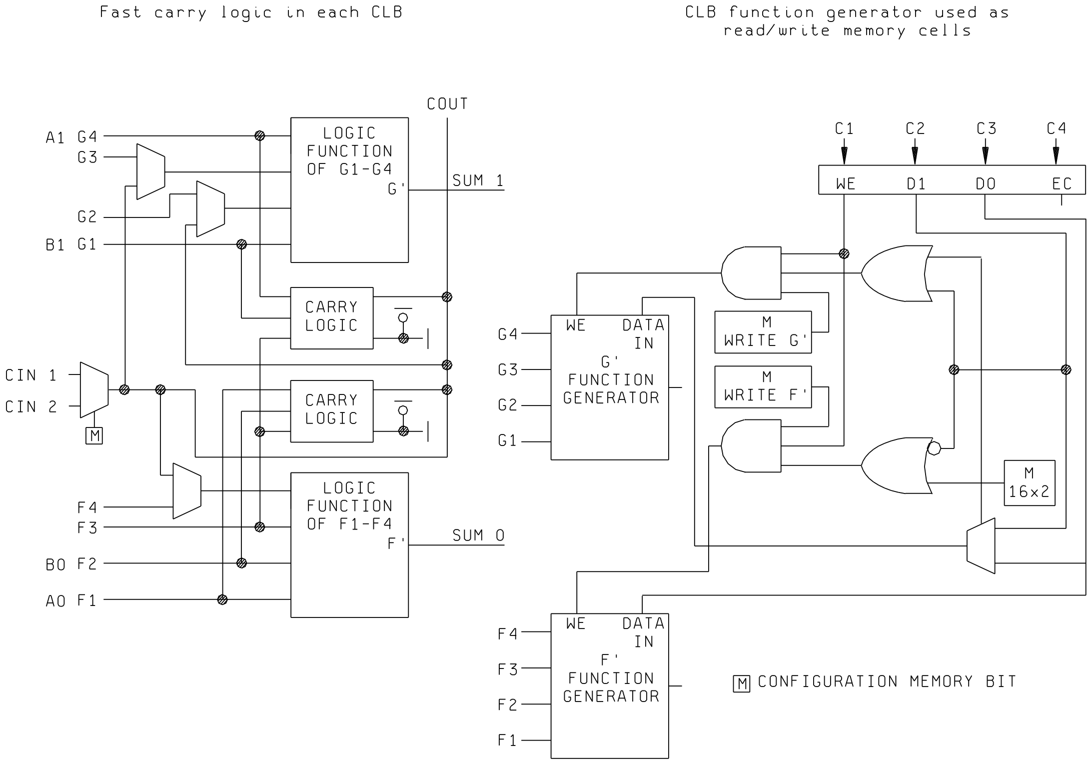


FIGURE 3. Logic block diagram - Continued.



Fast carry logic in each CLB

CLB function generator used as read/write memory cells

FIGURE 3. Logic block diagram - Continued.

BOUNDARY SCAN LOGIC

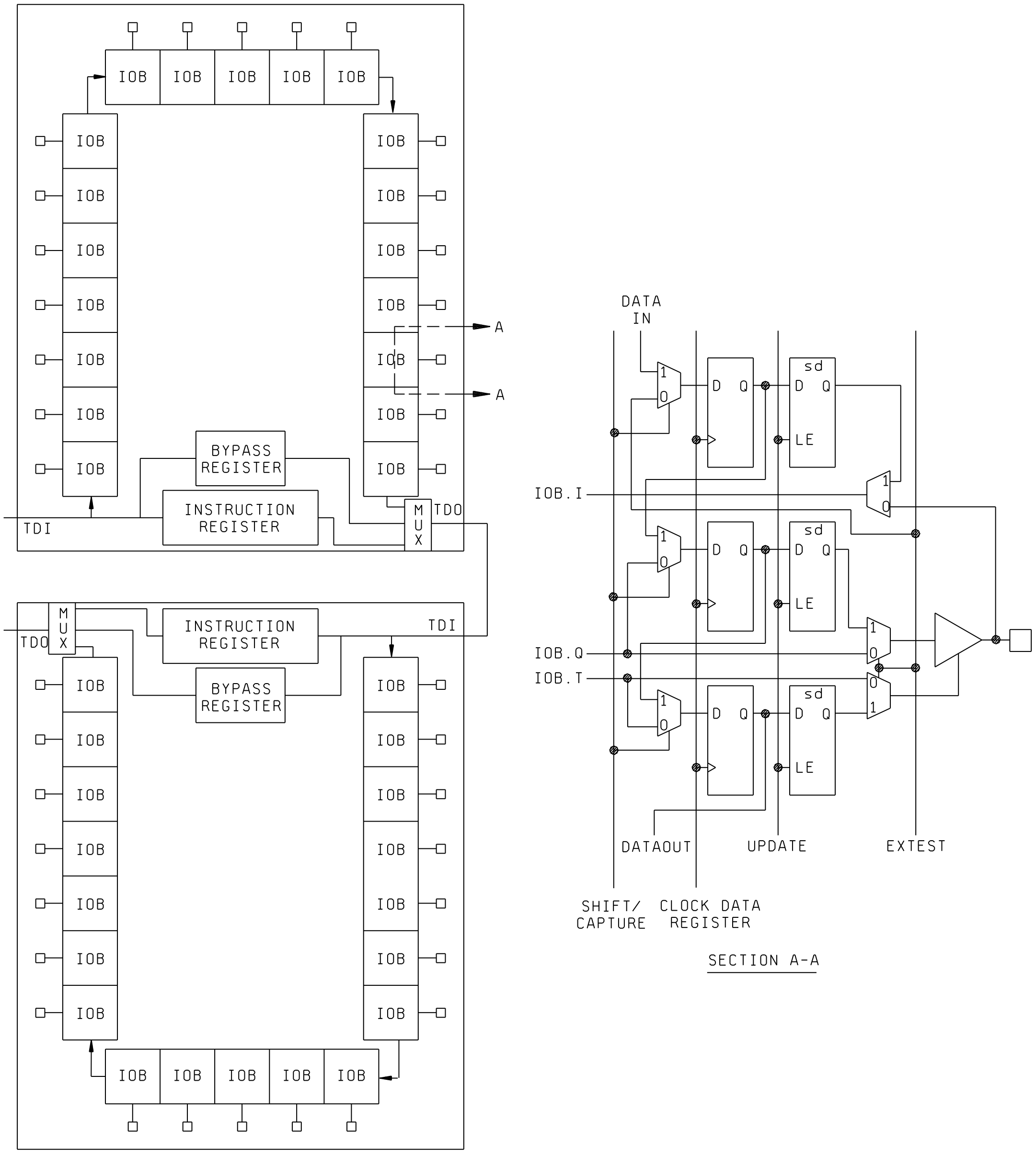


FIGURE 3. Logic block diagram - Continued.

GENERAL LOGIC CELL ARRAY (LCA) SWITCHING CHARACTERISTICS

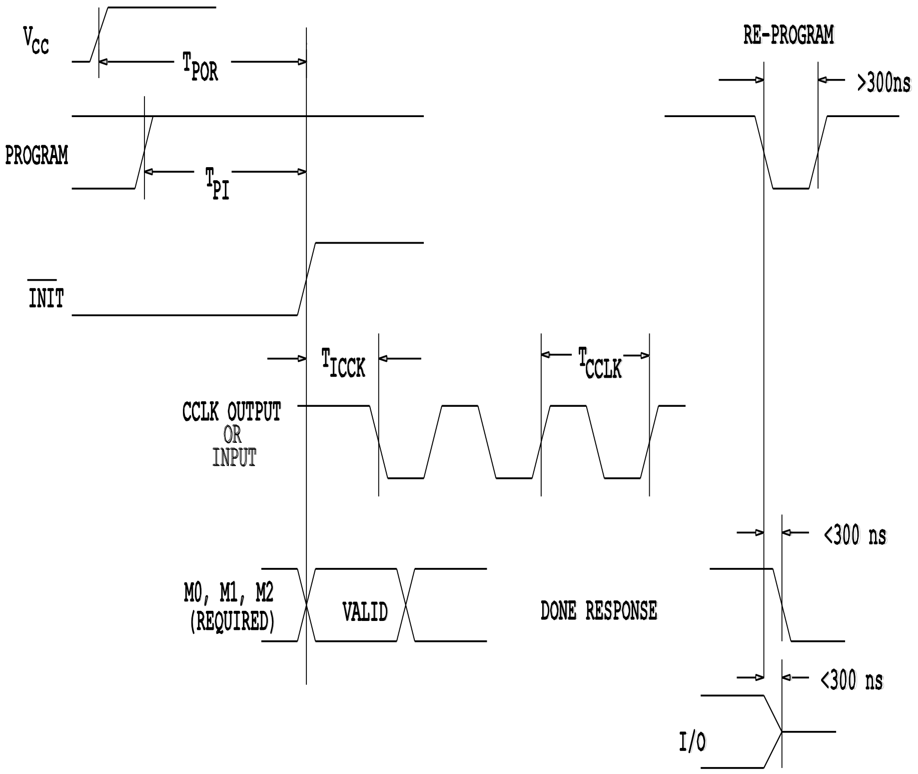


FIGURE 4. Timing diagrams and switching characteristics.

CONFIGURABLE LOGIC BLOCK (CLB) SWITCHING CHARACTERISTICS

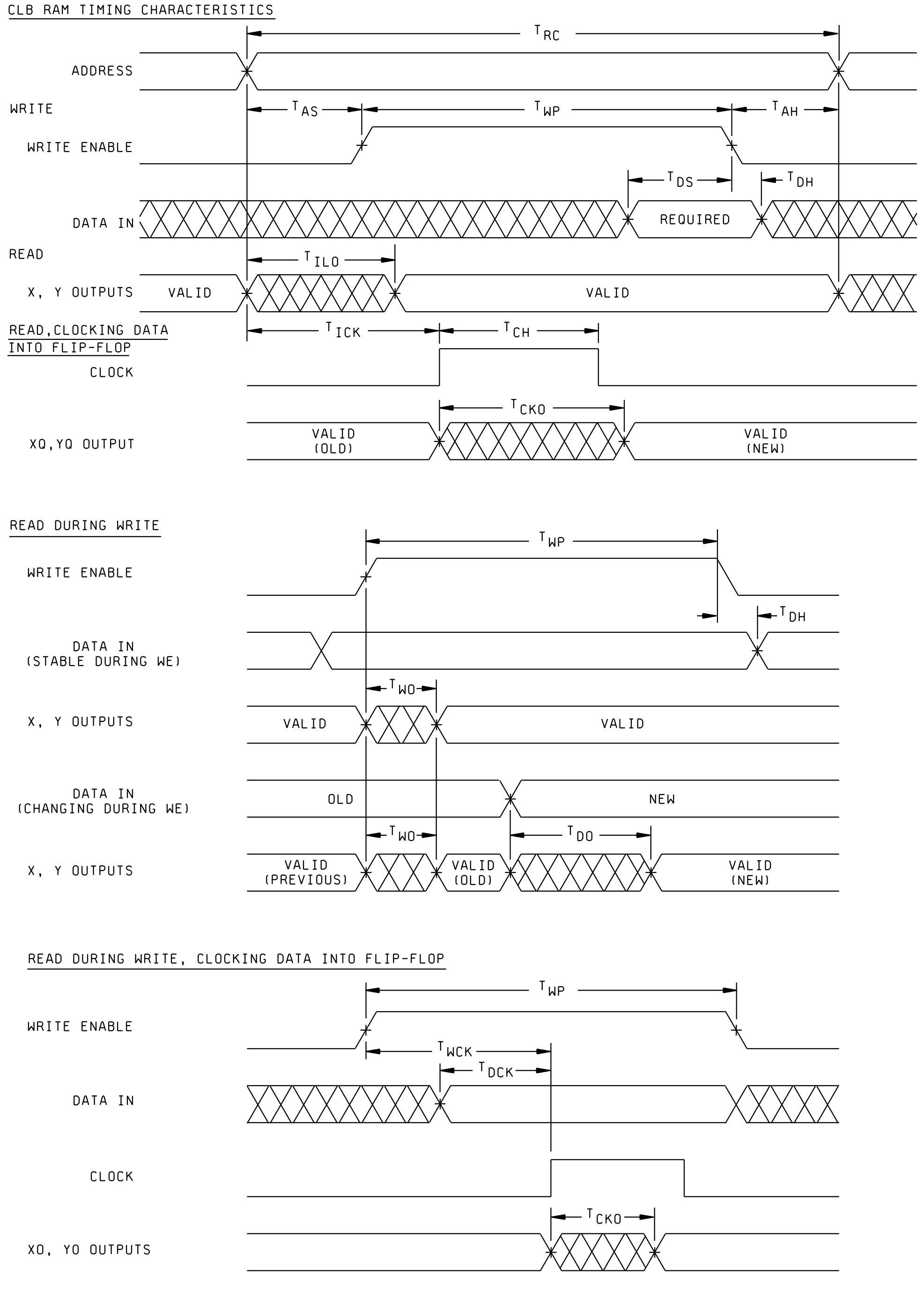
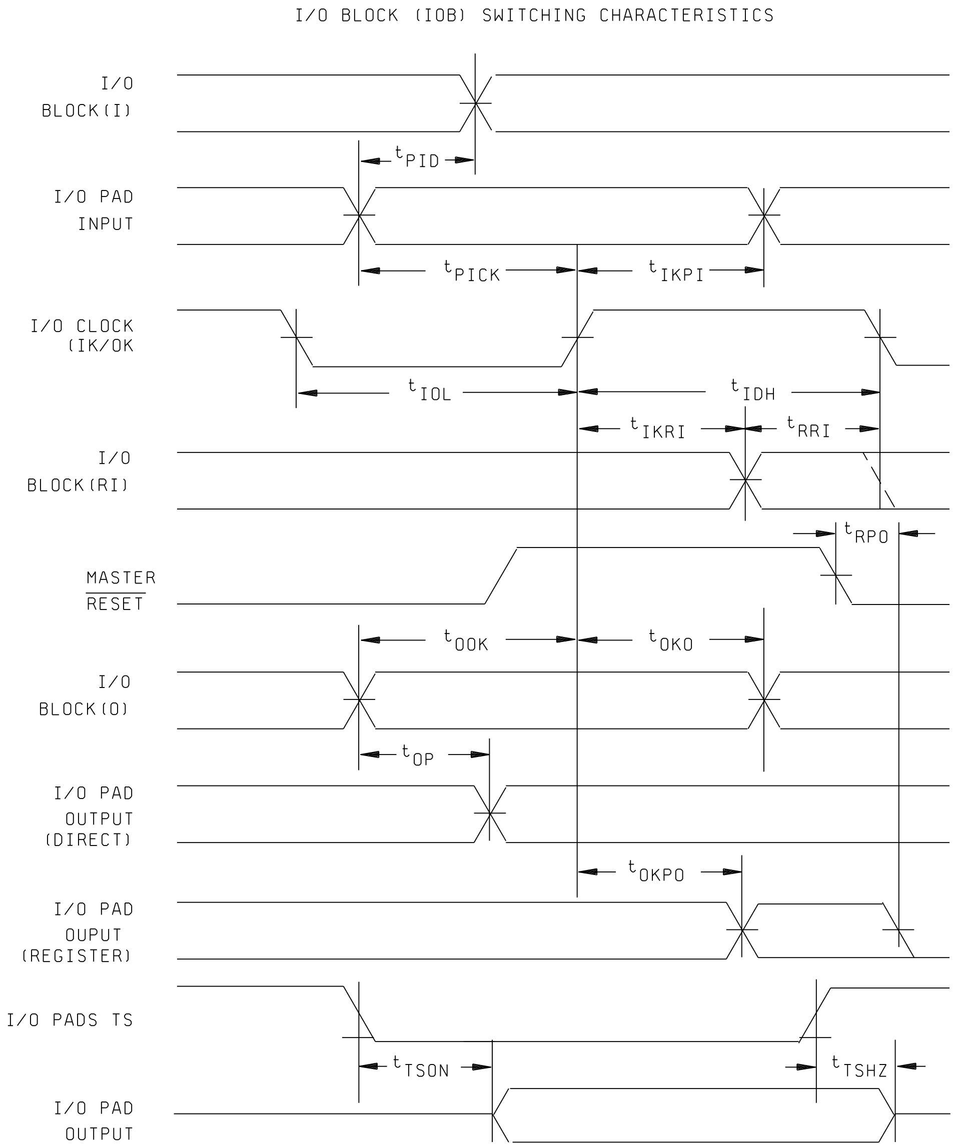
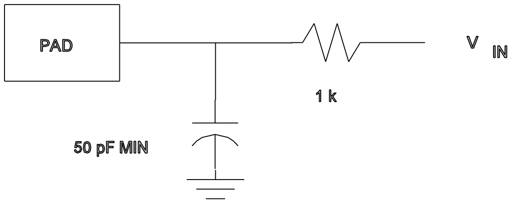


FIGURE 4. Timing diagram and switching characteristics - Continued.

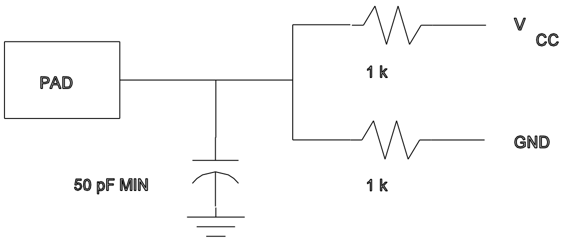


NOTE: t_{TSHZ} is determined when the output shifts 10 percent (of the output voltage swing) from V_{OL} level or V_{OH} level. See figure 5, circuit A herein for circuit used. t_{TSON} is measured at 0.5 V_{CC} level with V_{IN} = 0.0 V for three-state to active high, and V_{IN} = V_{CC} for three-state to active low. See figure 5, circuit B herein for circuit used.

FIGURE 4. Timing diagram and switching characteristics - Continued.



Circuit A



Circuit B

FIGURE 5. Load circuit.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5 and 6 (C_{IN} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device classes M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Required	Required	Required
3	Same as line 1			1* Δ
4	Dynamic burn-in (method 1015)	Not required	Not required	Not required
5	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
6	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A,8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1,2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
9	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q, and V shall be M, D, L, R, F, G and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CCO} standby	±1 mA of specified limit in table I.
I_{IL}	±1 µA of specified limit in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

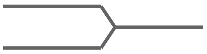
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535, MIL-STD-1331, and as follows:

V_{CC}	+5.0 V SUPPLY VOLTAGE
GND	GROUND
CCLK	CONFIGURATION CLOCK
DONE	DONE
PROGRAM	PROGRAM
RCLK	READ CLOCK
M0	MODE 0
M1	MODE 1
M2	MODE 2
TDO	TEST DATA OUTPUT
TDI	TEST DATA IN
TCK	TEST CLOCK
TMS	TEST MODE SELECT
HDC	HIGH DURING CONFIGURATION
LDC	LOW DURING CONFIGURATION
INIT	INIT
PGCK1-PGCK4	PRIMARY GLOBAL INPUTS
RDY/BUSY	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written into it. After configuration is complete, this pin becomes a user programmed I/O pin.
CSO	CHIP SELECT, WRITE
CS1	CHIP SELECT, WRITE
WS	WRITE STROBE
RS	READ STROBE
A0-A17	ADDRESS
D0-D7	DATA
DIN	DATA INPUT
DOUT	DATA OUTPUT
I/O	INPUT/OUTPUT

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique part numbers. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique part number. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

BUFFER SWITCHING CHARACTERISTICS

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TBUF driving a horizontal Longline (L.L.) I to L.L. while T is low (buffer active)	T_{IO1}	See note.	N/A	All		13	ns
TBUF driving a horizontal Longline (L.L.) I going low to L.L. going from resistive pull up high to active low, (TBUF configured as open drain)	T_{IO2}		N/A	All		13.5	ns
T going low to L.L active and valid	T_{ON}		N/A	All		15.1	ns
T to L.L. inactive	T_{OFF}		N/A	All		3	ns
T going high to L.L. (inactive) with single pull-up resistor	T_{PUS}		N/A	All		36	ns
T going high to L.L. (inactive) with pair of pull-up resistors	T_{PUF}		N/A	All		17	ns

NOTE: These values are typical. They are not tested, characterized, or guaranteed but are derived from benchmark timing patterns.

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-09-26

Approved sources of supply for SMD 5962-92305 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9230501MXX	68994	XC4010-10PG191B
5962-9230501MYX	68994	XC4010-10CB196B
5962-9230501MZX	68994	XC4010-10CB196B
5962-9230502MXX	68994	XC4010-6PG191B
5962-9230502MYX	68994	XC4010-6CB196B
5962-9230502MZX	68994	XC4010-6CB196B
5962-9230503MXX	68994	XC4010-5PG191B
5962-9230503MYX	68994	XC4010-5CB196B
5962-9230503MZX	68994	XC4010-5CB196B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124