REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Removed vendor 65786, added vendor 0WGG6. Changed number of devices tested in O/V (latch-up) test from 5 to 3. Changed Table I, ICC from 10 mA to 20 mA. Added footnote Table I, for Dynamic power. ksr	97-10-31	Raymond Monnin
B	Added case Y to cover pin grid array package. Editorial changes. ksr	99-06-16	Raymond Monnin

REV																				
SHEET																				
REV	B	B	B																	
SHEET	15	16	17																	

REV STATUS OF SHEETS																
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
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Michael A. Frye

DRAWING APPROVAL DATE
96-06-06

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY 4000 GATES, MONOLITHIC SILICON

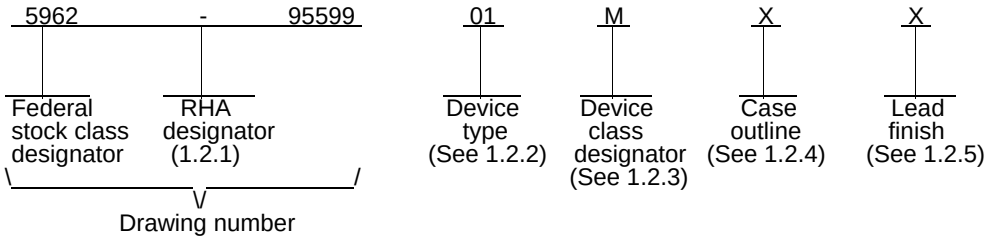
SIZE	CAGE CODE	
A	**67268**	**5962-95599**

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Delay Factor (K) Min	Max
01	7C386A-X	4000 Gate CMOS FPGA	0.39	3.00
02	QL16X24B-0	4000 Gate CMOS FPGA	0.39	1.82
03	QL16X24B-1	4000 Gate CMOS FPGA	0.39	1.56

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	160	Quad flat package
Y	CMGA7-P144	144	Pin Grid Array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-2.0 V dc to +7.0 V dc
Programming supply voltage range (V_{PP})	-2.0 V dc to +13.5 V dc 2/
DC input voltage range	-2.0 V dc to +7.0 V dc 2/
Maximum power dissipation	2.5 W 3/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	5.3° C/W
Case outline Y	See MIL-STD-1835
Junction temperature (T_J)	+175°C 4/
Storage temperature range	-65°C to +150°C
Data retention	10 years (minimum)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Minimum dc input voltage is -0.5 V, which may overshoot to -2.0 V for periods less than 20 ns. Maximum dc voltage on output pins is V_{CC} + 0.5 V, which may overshoot to +7.0 V for periods less than 20 ns under load conditions.
3/ Must withstand the added P_D due to short circuit test (e.g., IOS).
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

1.4 Recommended operating conditions. 5/

Case operating temperature Range(T_C)	-55°C to +125°C
Supply voltage relative to ground(V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	6/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

5/ All voltage values in this drawing are with respect to V_{SS}.
6/ Values will be added when they become available.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.12 Data Retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with the test data.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 5 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. Test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015. Use of built-in test circuitry testing the entire lot to verify programmability and AC performance without programming the user array is an option the manufacturer may use.

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7, 8A and 8B tests shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available upon request. For device classes Q and V subgroups 7, 8A and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 3 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is three devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8V I_{OH} = -8.0 mA, V_{IH} = 2.0 V	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All		0.4	V
High level input voltage	V_{IH}		1,2,3	All	2.0		V
Low level input voltage	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1,2,3	All	-10	+10	μA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{IN} = output disabled and 5.5 V	1,2,3	All	-10	+10	μA
Output short circuit current 1/ 2/ 3/	I_{OS}	VCC = 5.5 V, $V_{OUT} = V_{SS}$	1,2,3	All	-10	-80	mA
		VCC = 5.5 V, $V_{OUT} = V_{CC}$			30	140	
Dynamic Power supply current 4/	I_{CCD}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 V and 5.5 V	1,2,3	All		5/	mA
Standby Power supply current 4/	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 V and 5.5 V	1,2,3	All		20	mA
Input capacitance 2/	C_{IN}	See 4.4.1e	4	All		10	pF
Output capacitance 2/	C_{OUT}	See 4.4.1e	4	All		10	pF
Functional test		See 4.4.1c	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Propagation Delays with Fanout of 3/					Unit
Logic cells					1	2	3	4	8	
Combinatorial Delay 5/	t_{PD}	See figure 4	9,10,11	All	1.7	2.2	2.6	3.2	5.3	ns
Set-up time 5/	t_{SU}				2.1	2.1	2.1	2.1	2.1	
Hold time	t_H				0.0	0.0	0.0	0.0	0.0	
Clock to Q delay	t_{CLK}				1.0	1.5	1.9	2.6	4.7	
Clock HIGH time	t_{CWHI}				2.0	2.0	2.0	2.0	2.0	
Clock LOW time	t_{CWLO}				2.0	2.0	2.0	2.0	2.0	
Set delay	t_{SET}				1.7	2.2	2.6	3.2	5.3	
Reset delay	t_{RESET}				1.5	1.9	2.2	2.7	4.4	
Set width	t_{SW}				1.9	1.9	1.9	1.9	1.9	
Reset width	t_{RW}				1.8	1.8	1.8	1.8	1.8	

See footnotes at end of table.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Propagation Delays with Fanout of 3/						Unit
Input cells					1	2	3	4	8	12	
Input delay (HIGH DRIVE)	t_{IN}	See figure 4	9, 10, 11	All	2.8	2.9	3.0	3.1	4.0	5.3	ns
Input Inverting delay (HIGH DRIVE)	t_{INI}				3.0	3.1	3.2	3.3	4.1	5.7	
Input Delay (Bidirectional Pad)	t_{IO}				1.4	1.9	2.2	2.9	4.7	6.5	
Clock Buffer delay 6/	t_{GCK}				2.7	2.8	2.9	3.0	3.1	3.3	
Clock Buffer minimum HIGH 6/	t_{GCKHI}				2.0	2.0	2.0	2.0	2.0	2.0	
Clock Buffer minimum LOW 6/	t_{GCKLO}				2.0	2.0	2.0	2.0	2.0	2.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Propagation Delays with Output load capacitance (pF) of 3/					Unit
					30	50	75	100	150	
Output cells										
Output delay LOW TO HIGH	t_{OUTLH}	See figure 4	9,10,11	All	2.7	3.4	4.2	5.0	6.7	ns
Output delay HIGH to LOW	t_{OUTHL}				2.8	3.7	4.7	5.6	7.6	
Output delay three-state to HIGH	t_{PZH}				4.0	4.9	6.1	7.3	9.7	
Output delay three-state to LOW	t_{PZL}				3.6	4.2	5.0	5.8	7.3	
Output delay HIGH to three-state (figure 3)	t_{PHZ}				2.9					
Output delay LOW to three-state (figure 3)	t_{PLZ}				3.3					

See footnotes at end of table.

High Drive Buffer:

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	# High Drives Wired together	Propagation Delays with Fanout of 3/					Unit
						12	24	48	72	96	
High drive Input delay	t_{IN}	See figure 4	9,10,11	All	1	5.3	6.7				ns
					2		4.5	6.6			
					3			5.3	6.2	7.2	
					4				5.4	6.2	
High drive Input, Inverting delay	t_{INI}				1	5.7	7.2				
					2		4.6	6.8			
					3			5.5	6.4	7.4	
					4				5.6	6.4	

1/ Only one output at a time. Duration should not exceed 30 seconds.
2/ C_I = 45 pF max on I(SI) and I(P).

TABLE I. Electrical performance characteristics - Continued.

3/ Worst case propagation delay times over process variation at V_{CC} = 5.0 V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst case parameters over the full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3 ns linear transition time between 0 and 3 volts.

4/

1 CLB driving a 15 pF load	0.38 mW/MHz
1 clock buffer	0.36 mW/MHz
1 clock col buffer	0.08 mW/MHz
1 clock load	0.02 mW/MHz
1 macro cell driving a fanout of 4	0.44 mW/MHz

5/ These limits are derived from worst case values for a representaive selection of the slowest paths through the device logic cell including net delays. Guaranteed delay values for specific programmed part should be determined from simulation results.

6/ Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

Case X

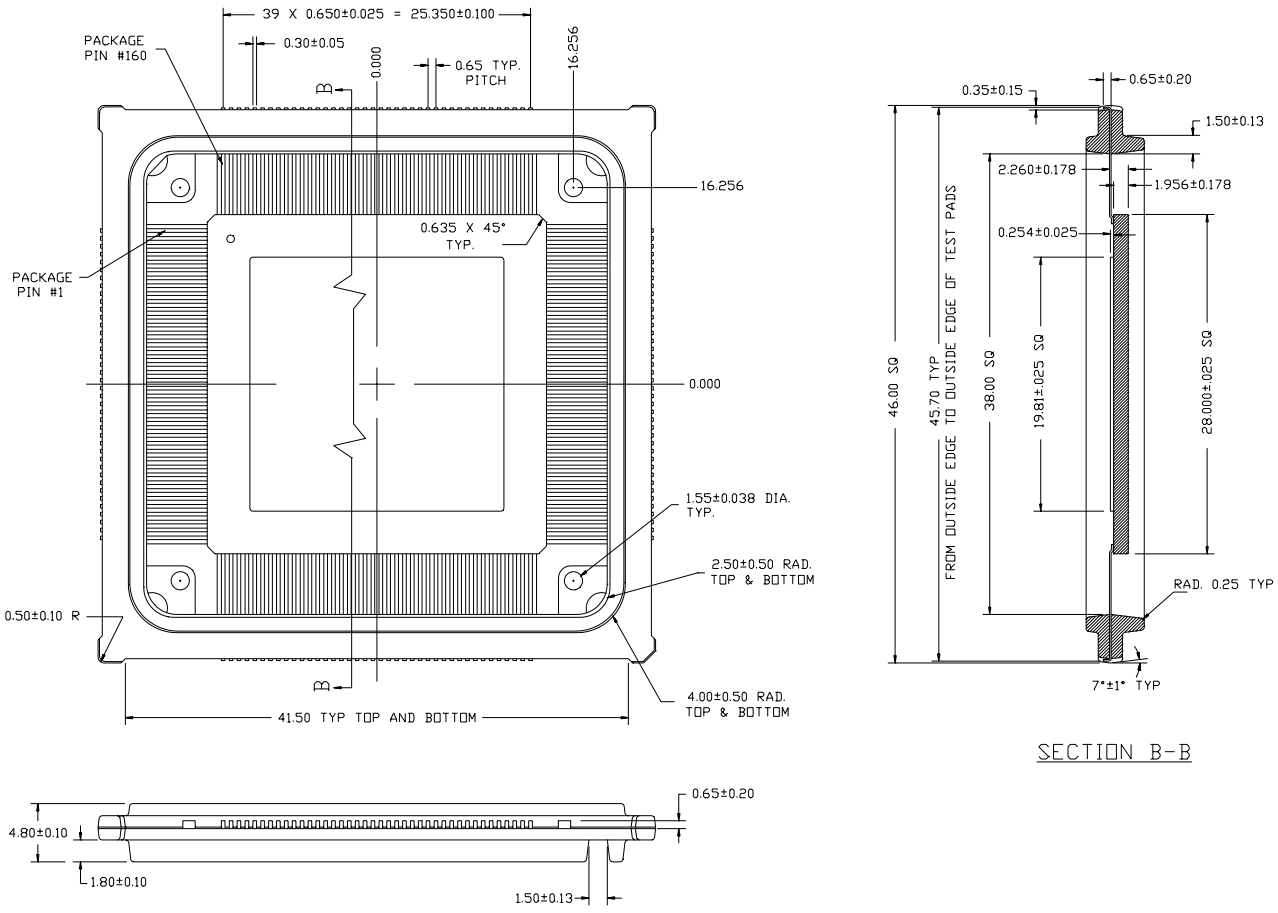


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE **A**		**5962-95599**
		REVISION LEVEL B	SHEET **11**

Case outline X

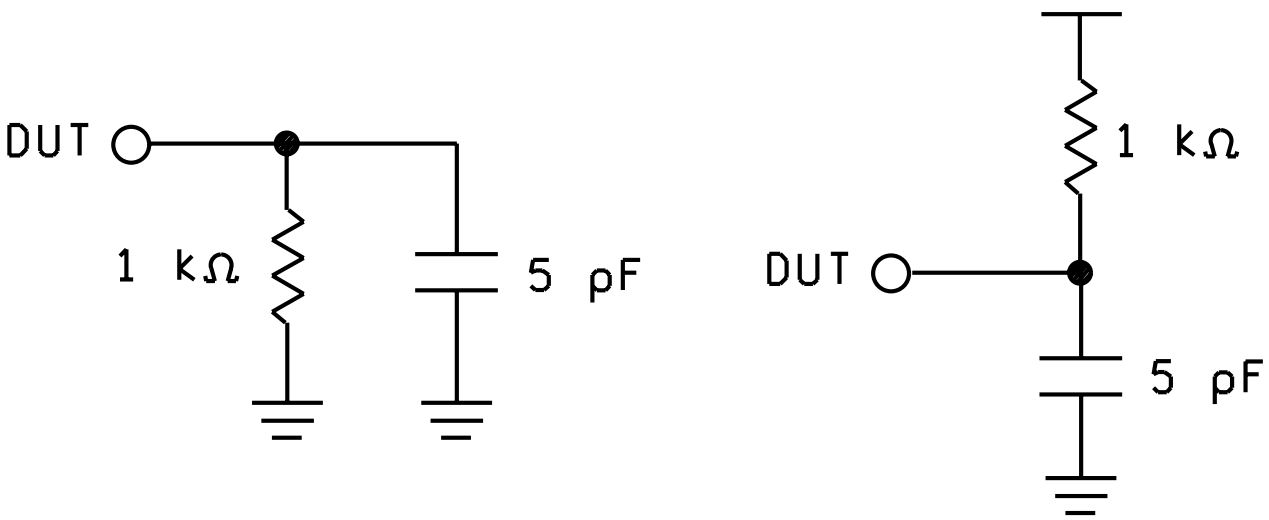
Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	I/O		55	NC		108	I/O
2	I/O		56	VSS		109	I/O
3	I/O		57	I/O		110	I/O
4	I/O		58	I/O		111	I/O
5	I/O		59	I/O		112	I/O
6	NC		60	V_{SS}		113	V_{SS}
7	I/O		61	I/O		114	I/O
8	VCC		62	I/O		115	NC
9	I/O		63	I/O		116	I/O
10	I/O		64	V_{CC}		117	I/O
11	I/O		65	I/O		118	I/O
12	I/O		66	NC		119	I/O
13	I/O		67	I/O		120	I/O
14	I/O		68	I/O		121	I/O
15	NC		69	I/O		122	I/O
16	I/O		70	I/O		123	I/O
17	VSS		71	I/O		124	I/O
18	I/O		72	I/O		125	I/O
19	I/SCLK		73	V_{SS}		126	NC
20	I/CLK(SM)		74	I/O		127	V_{CC}
21	VCC		75	NC		128	I/O
22	I(P)		76	I/O		129	I/O
23	I		77	I/O		130	I/O
24	VCC		78	I/O		131	I/O
25	I/O		79	I/O		132	I/O
26	NC		80	NC		133	I/O
27	I/O		81	I/O		134	I/O
28	I/O		82	I/O		135	NC
29	I/O		83	I/O		136	V_{SS}
30	I/O		84	I/O		137	I/O
31	I/O		85	I/O		138	I/O
32	I/O		86	NC		139	I/O
33	V_{SS}		87	I/O		140	V_{SS}
34	I/O		88	V_{CC}		141	I/O
35	NC		89	I/O		142	I/O
36	I/O		90	I/O		143	I/O
37	I/O		91	I/O		144	V_{CC}
38	I/O		92	I/O		145	I/O
39	I/O		93	I/O		146	NC
40	I/O		94	I/O		147	I/O
41	I/O		95	NC		148	I/O
42	I/O		96	I/O		149	I/O
43	I/O		97	V_{SS}		150	I/O
44	I/O		98	I/O		151	I/O
45	I/O		99	I(SI)		152	I/O
46	NC		100	I/CLK		153	V_{SS}
47	VCC		101	V_{CC}		154	I/O
48	I/O		102	I		155	NC
49	I/O		103	I(SO)		156	I/O
50	I/O		104	V_{CC}		157	I/O
51	I/O		105	I/O		158	I/O
52	I/O		106	NC		159	I/O
53	I/O		107	I/O		160	NC
54	I/O						

FIGURE 2. Terminal connections.

Case outline Y

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A1	I/O		E1	I/O		N1	I/O
A2	I/O		E2	I/O		N2	I/O
A3	I/O		E3	GND		N3	VSS
A4	I/O		E13	VCC		N4	I/O
A5	I/O		E14	I/O		N5	I/O
A6	I/O		E15	I/O		N6	I/O
A7	I/O		F1	I/O		N7	VSS
A8	I/O		F2	I/O		N8	I/CLK
A9	I(P)		F3	I/O		N9	VCC
A10	I/O		F13	I/O		N10	I/O
A11	I/O		F14	I/O		N11	VSS
A12	I/O		F15	I/O		N12	I/O
A13	I/O		G1	I/O		N13	VCC
A14	I/O		G2	I/O		N14	I/O
A15	I/O		G3	VCC		N15	I/O
B1	I/O		G13	VSS		P1	I/O
B2	NC		G14	I/O		P2	I/O
B3	I/O		G15	I/O		P3	I/O
B4	I/O		H1	I/O		P4	I/O
B5	I/O		H2	I/O		P5	I/O
B6	I/O		H3	I/O		P6	I/O
B7	I/O		H13	I/O		P7	I(SO)
B8	I/SCLK		H14	I/O		P8	I(SI)
B9	I		H15	I/O		P9	I/O
B10	I/O		J1	I/O		P10	I/O
B11	I/O		J2	I/O		P11	I/O
B12	I/O		J3	VSS		P12	I/O
B13	I/O		J13	VCC		P13	I/O
B14	I/O		J14	I/O		P14	NC
B15	I/O		J15	I/O		P15	I/O
C1	I/O		K1	I/O		R1	I/O
C2	I/O		K2	I/O		R2	I/O
C3	VCC		K3	I/O		R3	I/O
C4	I/O		K13	I/O		R4	I/O
C5	VSS		K14	I/O		R5	I/O
C6	I/O		K15	I/O		R6	I/O
C7	VCC		L1	I/O		R7	I
C8	I/CLK(SM)		L2	I/O		R8	I/O
C9	VSS		L3	VCC		R9	I/O
C10	I/O		L13	VSS		R10	I/O
C11	VCC		L14	I/O		R11	I/O
C12	I/O		L15	I/O		R12	I/O
C13	VSS		M1	I/O		R13	I/O
C14	I/O		M2	I/O		R14	I/O
C15	I/O		M3	I/O		R15	I/O
D1	I/O		M13	I/O			
D2	I/O		M14	I/O			
D3	I/O		M15	I/O			
D13	I/O						
D14	I/O						
D15	I/O						

FIGURE 2. Terminal connections - continued.



t_{PHZ} t_{PLZ}

FIGURE 3. Output load circuits and test conditions.

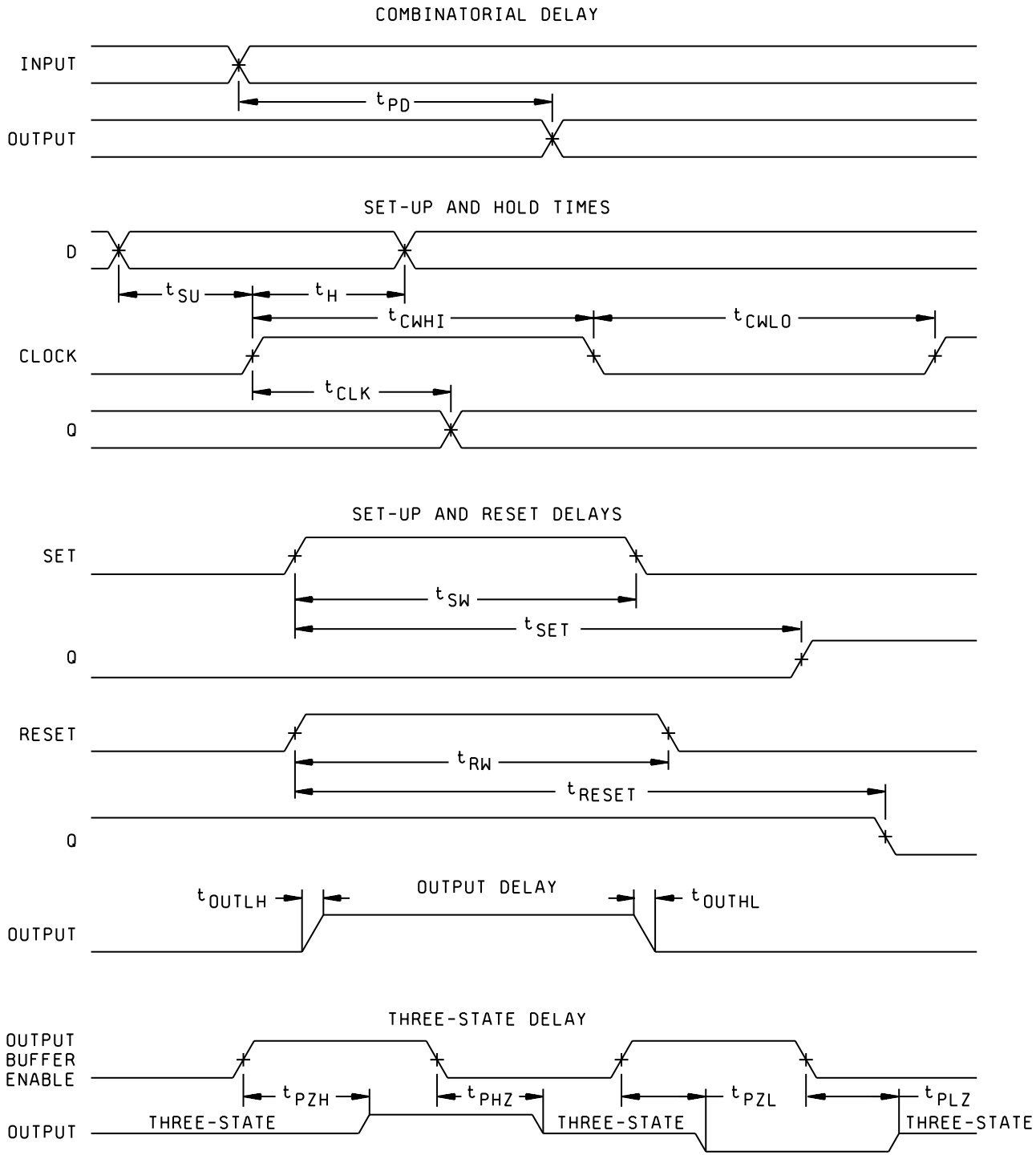


FIGURE 4. Switching waveforms.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9 or 2,8A,10
2	Static burn-in (method 1015)	Not Required	Not Required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
6	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
8	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
9	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{OZ}	±10% of the specified value in table I
I_{IX}	±10% of the specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 16 JUNE 1999

Approved sources of supply for SMD 5962-95599 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-9559901QXC	2/	CY7C386A-XUMB
5962-9559902MXC	0WGG6	QL16X24B-0CF160M/883C
5962-9559903MXC	0WGG6	QL16X24B-1CF160M/883C
5962-9559902MYC	0WGG6	QL16X24B-0CG144M/883C
5962-9559903MYC	0WGG6	QL16X24B-1CG144M/883C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Not available from an approved source.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0WGG6	QuickLogic Corporation 1277 Orleans Drive Sunnyvale, CA 94089-1138

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.