

EVALUATION
OF THE
CHIP EXPRESS
QYH580 (LPGA)

Test Date: February, 1997, March, 1997, May, 1997

Test Location: Brookhaven National Laboratory (Heavy Ion)
NASA/GSFC (Total Dose)
NASA/GSFC (DPA)

Test Device: Chip Express QYH580

Prepared By: NASA/GSFC (R. Katz)

INTRODUCTION

The QYH580 is a member of the Chip Express QYH500 family. This family is a 0.8 μm bulk CMOS technology. The QYH500 gate array can be configured to yield up to 60,000 usable "gate array gates". This technology utilizes two types of cells: I/O cells and 2 input NAND gates. The I/O cells may be programmed into a variety of configurations; however, there is no storage available in these cells. The two input NAND gates can be configured to provide buffers, logic functions, or flip-flops. The I/O structure is flexible and the devices may have the pins configured per user specifications. For this evaluation, the QYH580 was configured to be pin compatible with an Actel A1280A in a CPGA176 package for both a proof of concept and compatibility with existing test infrastructure. Chip Express is foundryless; the QYH500 series of devices is fabricated by Yamaha.

The QYH500 series is a channeled gate array architecture. Metal routing segments are "pre-placed" in the channels and all possible connections are made during integrated circuit fabrication. The chip is "programmed" by selectively opening connections leaving the interconnect in a state which implements the design netlist. This is opposite of antifuse-based Field Programmable Gate Array (FPGA) technology where connections are made during programming by making an antifuse into a conductor. Note that only a small fraction of possible connections are needed in a gate array; thus in an FPGA a small number of connections must be programmed and in the QYH500 the majority of connections must be made into open circuits.

The QYH500 series, for the purposes of this evaluation, can be programmed using two different techniques for the identical base arrays. The first technique utilizes a laser to remove the unwanted connections and takes on the order of 1 hour at the factory. Turn around for these *Laser Programmable Gate Arrays* (LPGA) is on the order of days. A *one mask* technology can remove metal connections from the base array on two levels of metal using a single masking step. In both cases, unused routing segments are left floating. For quick prototypes (as were our test devices) the LPGA is used and the device is not passivated. The 883-qualified devices are processed using one mask technology and are passivated following processing. The devices are qualified for both $V_{CC} = 3.3$ and 5.0 volts.

This evaluation is considered preliminary: 3 devices were used for heavy ion testing, 1 for total ionizing dose (TID) testing, and several unprogrammed devices were used for a quick, coarse, destructive physical analysis. The sample device utilized approximately 35,000 gate array gates, roughly 4 times that of our A1280A 1.0 μm samples. It was observed even with the higher gate counts, the dynamic power of the QYH500 was less than the A1280A; static power was essentially 0 μA (our system, as configured, had a measurement resolution of 10 μA).

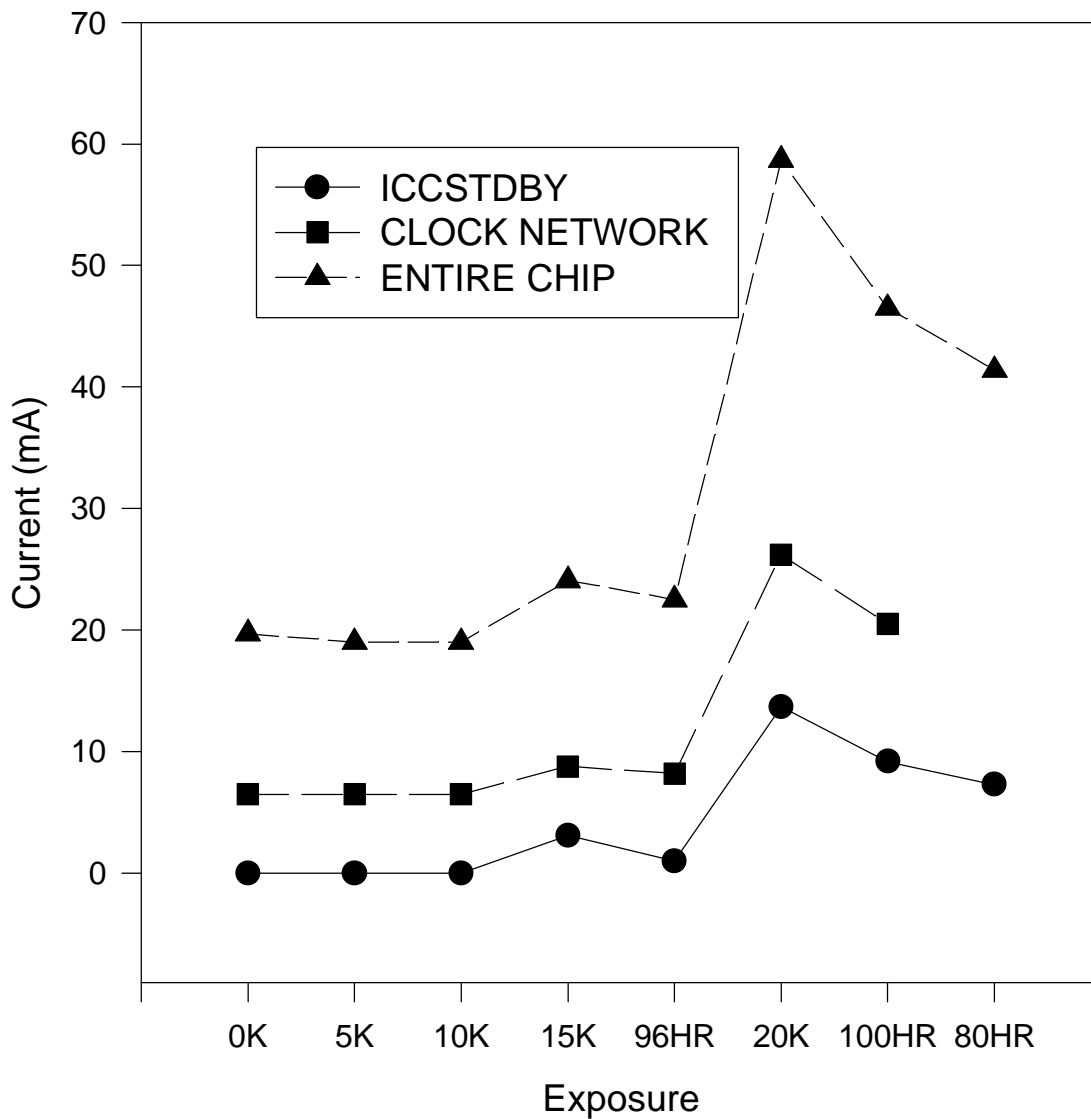
The CX2000 series of devices is a 0.6 μm epi-layer technology fabricated by Tower Semiconductor. This part will be evaluated in future tests (July, 1997).

TOTAL IONIZING DOSE TEST

TID testing was performed at NASA/GSFC using a Co-60 source. The device was statically biased at $V_{CC} = 5.0$ VDC with all inputs terminated to ground. The dose rate was 5 krad (Si) / day or 0.058 rads (Si) per second. Functional tests were run at each radiation step of 5 krad (Si) and three device current parameters were measured: standby (the entire chip static), clock on (measuring the clock distribution network), and dynamic, with all elements toggling at approximately 500 kHz.

No functional failures were detected and a plot of I_{CC} vs. radiation and annealing is given below. Testing proceeded to 20 krad (Si). All annealing was biased at $V_{CC} = 5.0$ VDC and was at room temperature.

QYH500 LPGA1 TID TEST



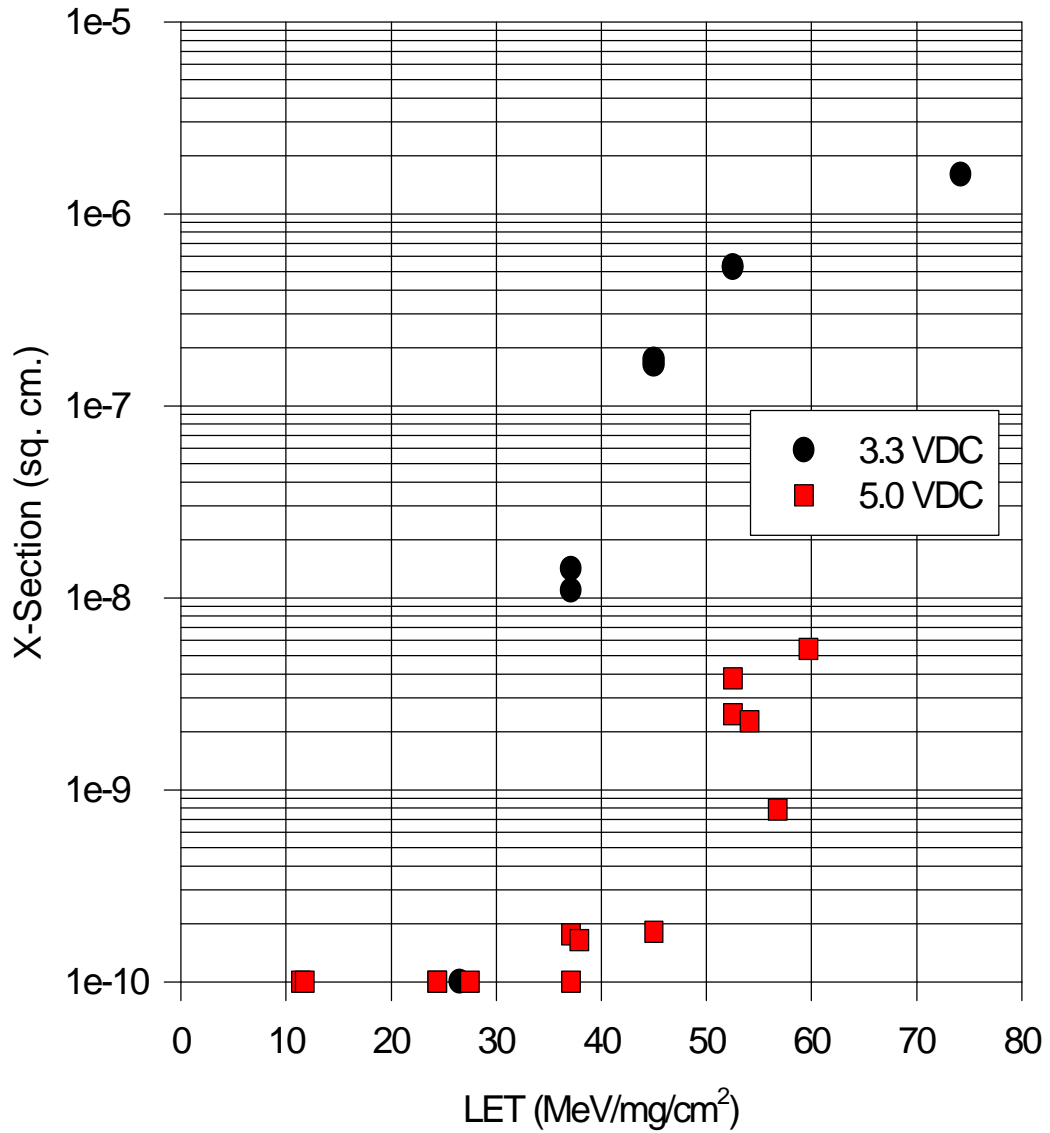
HEAVY ION TESTING

Heavy ion Single Events Effects (SEE) testing was performed at Brookhaven National Laboratory. The device was monitored for single event upset (SEU), single event latchup (SEL) and device functionality. Strip charts were made of I_{CC} vs. time. Nominal fluence for each run was either 0.5×10^7 or 1×10^7 ions/cm². Runs were performed with V_{CC} either in the standard 5.0 VDC \pm 10% range or in the 3.3 VDC \pm 10% range.

No functional failures were observed during testing. Latchup was detected at relatively high LETs with V_{CC} in the 5.0 VDC \pm 10% range; no latchup was observed in the lower voltage range up to an LET of 74 MeV-cm²/mg. Latchup data is summarized in the chart below. SEU performance was very good with upsets first detected near LET = 40 MeV-mg/cm² with a very small cross-section; the SEU performance is also summarized in a chart below. SEU performance has been measured for both 5.0 and 3.3 volt bias levels. The good SEU performance is believed to come from the relatively high capacitance of the "pre-laid" metal routing segments. Note that this performance is similar to that observed for Actel C-Module flip-flops in one of its two storage states which uses a similar routing segment scheme.

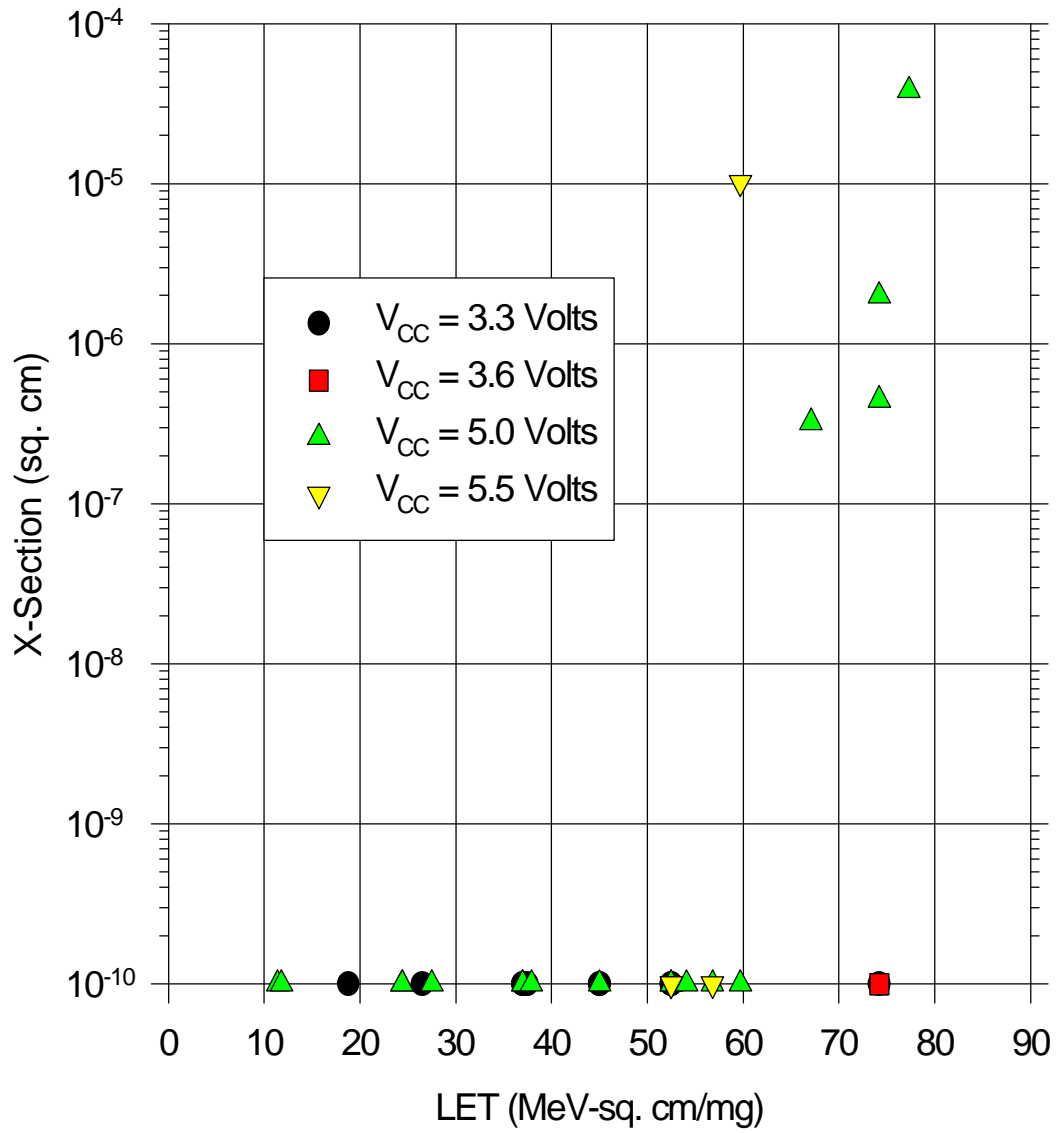
Points at the graphs on the 1×10^{-10} line indicate that no SEE was detected for that run.

QYH580 SEU Data (S/Ns 1, 3, 4)



NASA/GSFC (rk/af)
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QYH580 Latchup Data (S/Ns 1, 3, 4)

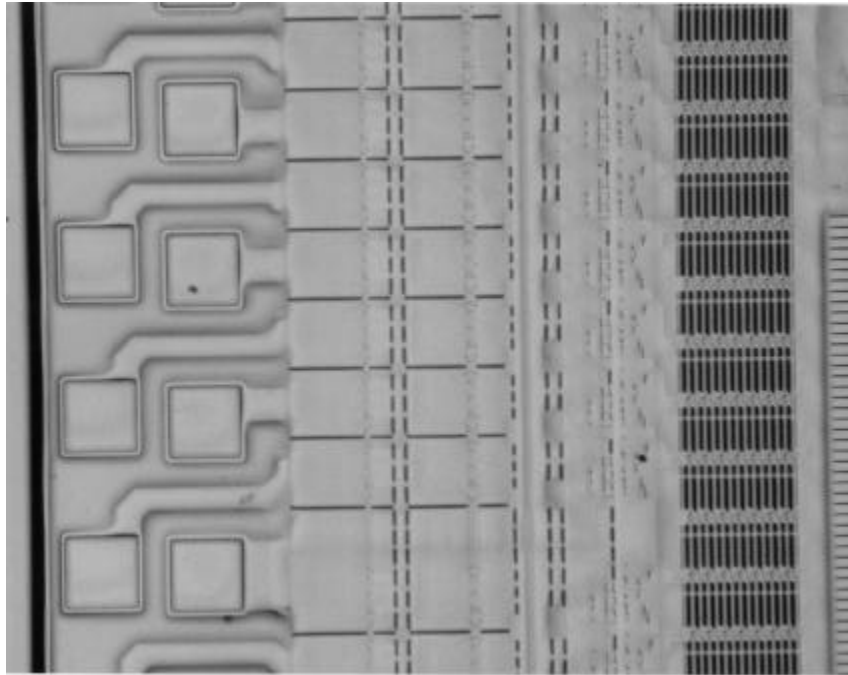


NASA/GSFC (rk/af)

DESTRUCTIVE PHYSICAL ANALYSIS

Unprogrammed devices from the QYH500 and CX2000 series were subject to a quick, rough, destructive physical analysis. No obvious defects were noted and the preliminary evaluation showed processing consistent with 883 standards. Fully processed samples are expected for a more thorough analysis in the near future.

The CX2000 series has a very high I/O pin count. Note, in the photograph below, that many of the I/O pads are staggered. This can have implications for package selection and chip on board (COB) or multi-chip modules (MCMs).



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Software and Design Flow

Chip Express has two families for low volume applications using it's LPGA and OneMask technologies; the QYH500 is 0.8 micron, two level metal and the CX2000 family is 0.6 micron, three level metal. The "golden" simulator for both parts is Cadence Verilog XL. Also supported for signoff are Synopsys VSS and Model Tech's V-System with the VHDL flow utilizing Vital-95. Synthesis for these devices is provided by Synopsys' Design Compiler and Exemplar Leonardo. Scan insertion is accomplished using either Synopsys' Test Compiler or Syntest's Picasso. Motive is used for static timing analysis.

For the QYH500 family only, Viewlogic schematic capture and simulation (ViewDraw and ViewSim) are supported.