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INTEROFFICE MEMO

97-SYD-029

FROM: Tom Page (Mail Stop 120 / 023) Ext. 7-1870

SUBJECT: Qualification Total-Dose Test Results for the Actel **RH1020** Field-Programmable Gate Array (FPGA) Microcircuit, Lockheed Martin Federal Systems (LMFS) Part No. *197A805*

DATE: 10 October 1997

Purpose: The purpose of this radiation test was to characterize and to qualify the RH1020 Field-Programmable Gate Array (FPGA) microcircuit to total-ionizing-dose radiation. To do this, a sample size of five (5) programmed parts was exposed to gamma radiation from a cobalt-60 (^{60}Co) radiation source at 1X the specified radiation level (*i.e.*, 300 krads{Si}) and then at 2X the specified radiation level, with all parts passing.

Background: The part type tested is fully identified as a radiation-hardened monolithic silicon complementary-metal-oxide-semiconductor (CMOS) 2000-gate field-programmable gate array microcircuit. This part type is fabricated using the LMFS "RHCMOS-4EF" process merged with the Actel oxide-nitride-oxide (ONO) anti-fuse process, with L_{EFF} = 0.8 µm, V_{DD} = +5.0V, and ONO T_{EFF} = 96 Å. The electrical performance characteristics are provided in LMFS top-level drawing (TLD) #197A805.

Exposures: The RH1020 FPGA devices, five (5) programmed samples of device type 197A805, were tested for their responses to total-ionizing-dose (TID) radiation. The five samples were exposed to radiation doses of 200 krads(Si), 300 krads(Si), and 600 krads(Si) using the LMFS in-house J.L. Shepherd Model 109-68 Laboratory Irradiator (gamma source). The TID testing was performed per the guidelines of MIL-STD-883E, Method 1019.4.

Results: All five test samples were fully functional before and after the TID testing including the subsequent 168-hour high-temperature anneal. Each test sample met the specified performance and parametric limits listed in TLD #197A805; key parameters are shown graphically as a function of TID in Attachment 1. As a result of this test, the RH1020 Field-Programmable Gate Array IC (#197A805) has satisfied the radiation-test criteria for qualification as a radiation-hardened "300-krad(Si)" part.

Discussion:

Test Samples. The 197A805 RH1020 FPGA test samples were from TCI lot T7012E.1, which came from manufacturing lots # 96509A.1 and # 96509B.1. The exposed test samples consisted of modules #1413, #1414, #1415, #1419, and #1535, with module #1417 as the "control" sample. All parts were packaged in 84-pin leaded flat packs (lidded).

Test Configuration. Each part was programmed by LMFS (Manassas) with an *ALPHA-11* pattern and employing a "Binning Circuit." This "Binning Circuit" consists of one input buffer, sixteen combinatorial logic modules, and one output buffer. The logic modules are configured as non-inverting buffers, and are connected through programmed antifuses with typical capacitive loading.

Test Conditions. During the total-dose exposures, each sample was biased at $\mathbf{V}_{DD}$ = +5.0V dc. Each part was exposed at a case temperature of ~+28°C (ambient). Parametric and performance measurements, pre- and post-exposure, were made at a controlled temperature of +25.0°C.

Test Equipment. The *ADVANTEST* T3340 General-Purpose VLSI Test System was used to measure each part. Measurements were made at pre-exposure, after each radiation level, and after the anneal. Actel repeated final parametric measurements on the tested parts, especially $\mathbf{V}_{IH}$, to verify final passing values.

Summary. The particulars of this test are summarized below:

- **Part Type:** RH1020 Field-Programmable Gate Array (FPGA), Si, CMOS, monolithic, device type # 197A805, 2000 gates.
- **Part Process:** RHCMOS-4EF ($\mathbf{L}_{EFF}$ = 0.8 µm; $\mathbf{V}_{DD}$ = +5.0V; 96 Å ONO).
- **Samples Tested:** Five (5) plus one (1) "control."
- **Test Lot:** T7012E.1; Manufacturing Lots #96509A.1 & #96509B.1.
- **Test Samples:** *A.1*: #1413, #1414, #1415, #1417, #1419; *B.1*: #1535.
- **Package Type:** 84-lead Flat Pack (lidded).
- **Test Facility:** Lockheed Martin Federal Systems - Manassas (LMFS-M) J.L. Shepherd Model 109-68 (S*I*N 3028) gamma source.
- **Dose Levels:** 200 krads(Si), 300 krads(Si), and 600 krads(Si).
- **Dose Rate:** 125.3 rads(Si)/s.
- **Test Date:** 17 September 1997.
- **Bias Conditions:** +5.0V dc (exposures); +4.50V, +4.75V, +5.00V, +5.25V, and +5.50V (measurements); and +5.5V (anneal).
- **Test Pattern:** *ALPHA-11* with "Binning Circuit"
- **Temperatures:** ~+28°C (exposures); +25°C measurements; +125°C (168-hour anneal).
- **Test Method:** Radiation-tested per MIL-STD-883E, Method 1019.4. The **D**evice **U**nder **T**est (DUT) was exposed while powered, & measured on the *ADVANTEST* logic tester. DUT's parameters and functionality measured before radiation, after each exposure, and again after 168 hours of a high-temperature (+125°C) anneal while on bias. *[Note: The anneal was conducted at +125°C instead of +100°C, and +5.5V instead of +5.0V, to accommodate concurrent testing in the Burn-In Lab ovens. This constitutes a worse-case condition, so passing results are valid with additional margin.]*
- **Test Personnel:** C. Kaufman (Logic Test), C. Gibson (Logic Test); T. Page, R. Brown (Radiation Assurance Engineers), and J. Vasquez (Radiation Assurance Technician).

Any questions concerning these data or the test report should be directed to the author at (703) 367-1870.

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Attachment 1

Data Plots & Tables

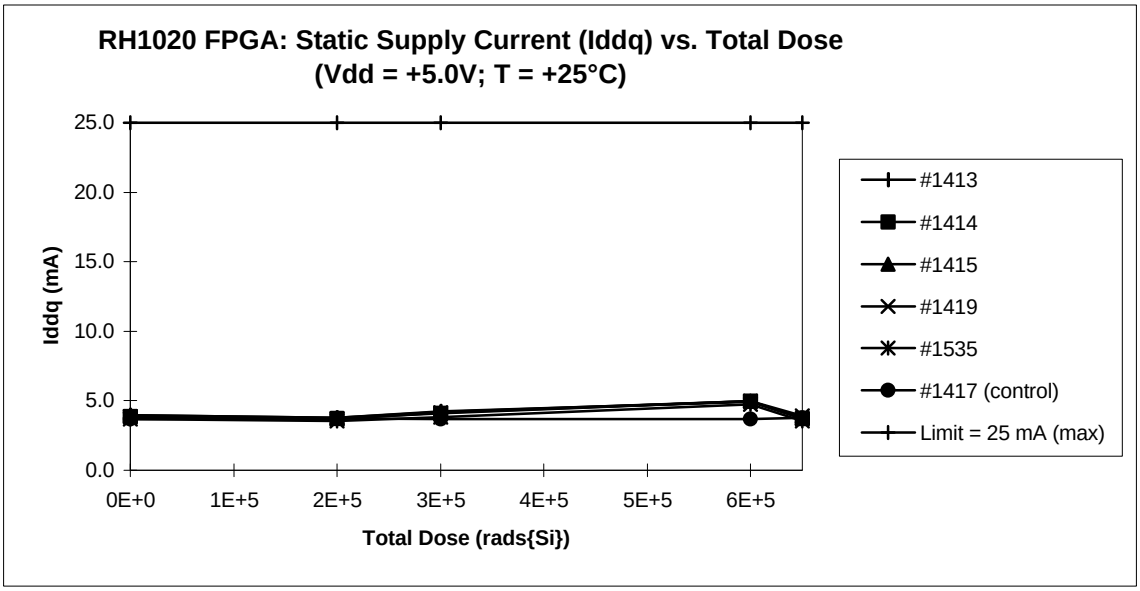

Figure 1a. Static Supply Current (I_{DDQ}) vs. Total Dose — Full View

(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}

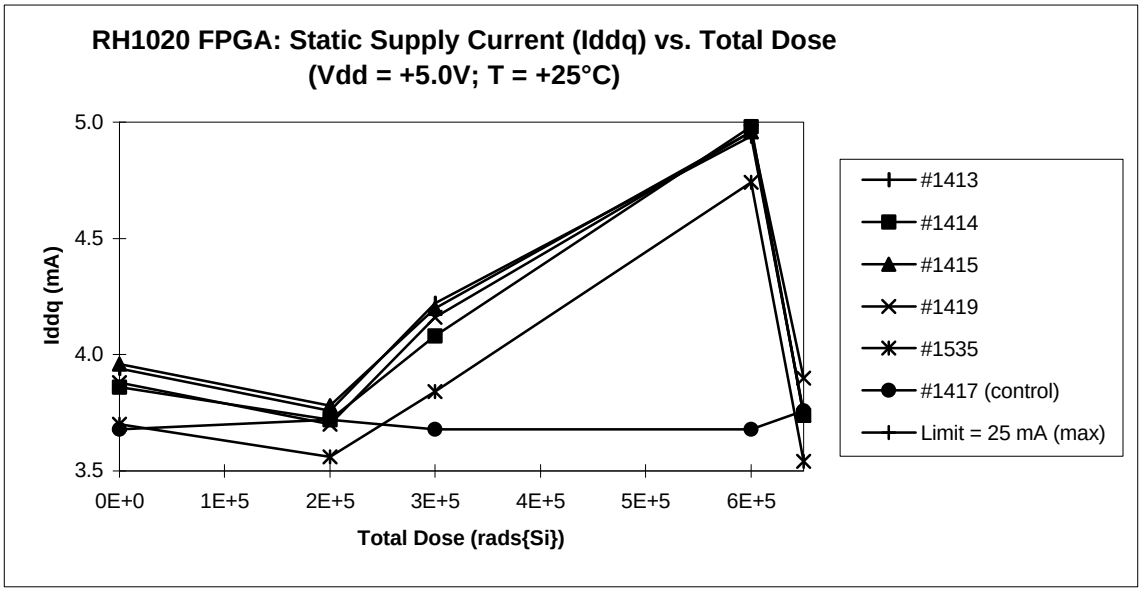

Figure 1a. Static Supply Current (I_{DDQ}) vs. Total Dose — Close-Up View

(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}

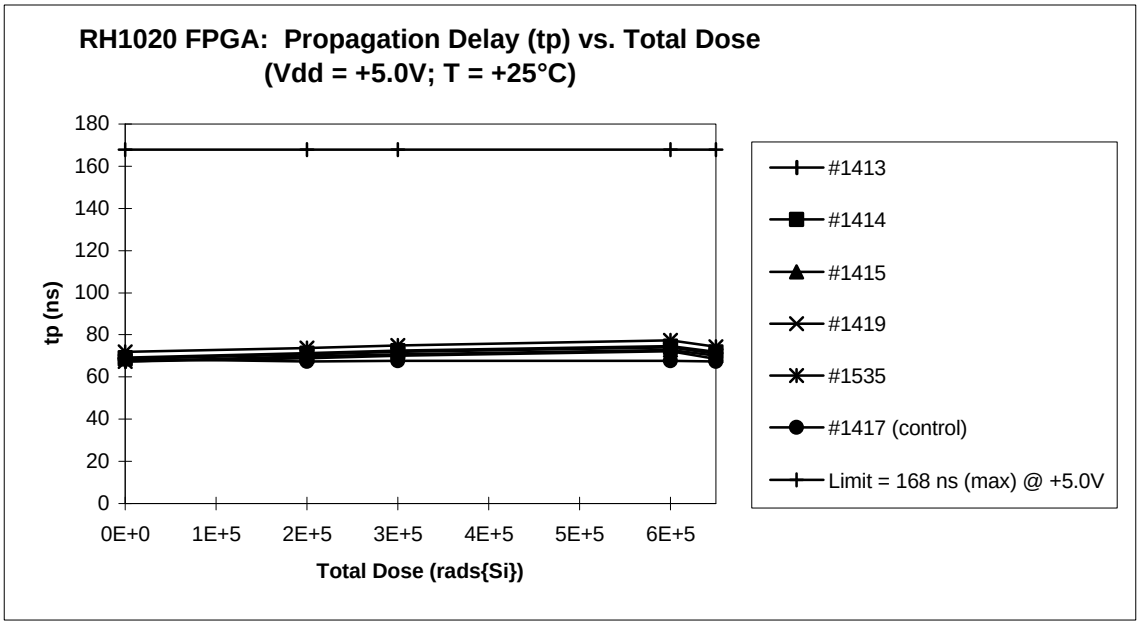

Figure 2a. Propagation Delay (t_P) vs. Total Dose — Full View
(Binning-Circuit)
(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}

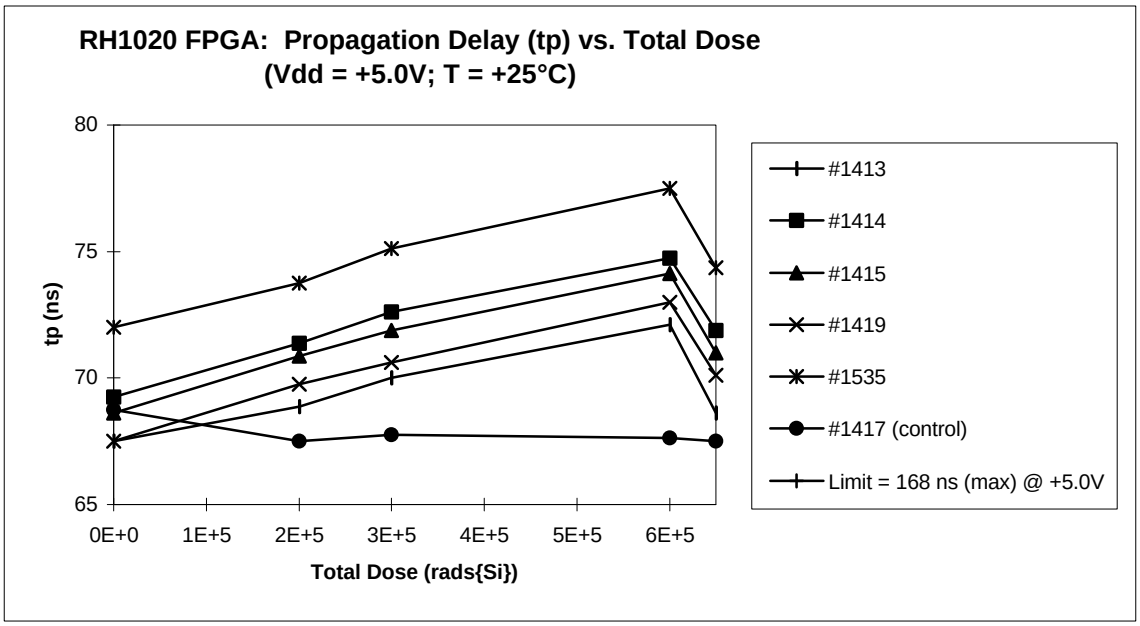

Figure 2b. Propagation Delay (t_P) vs. Total Dose — Close-Up View
(Binning-Circuit)
(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}

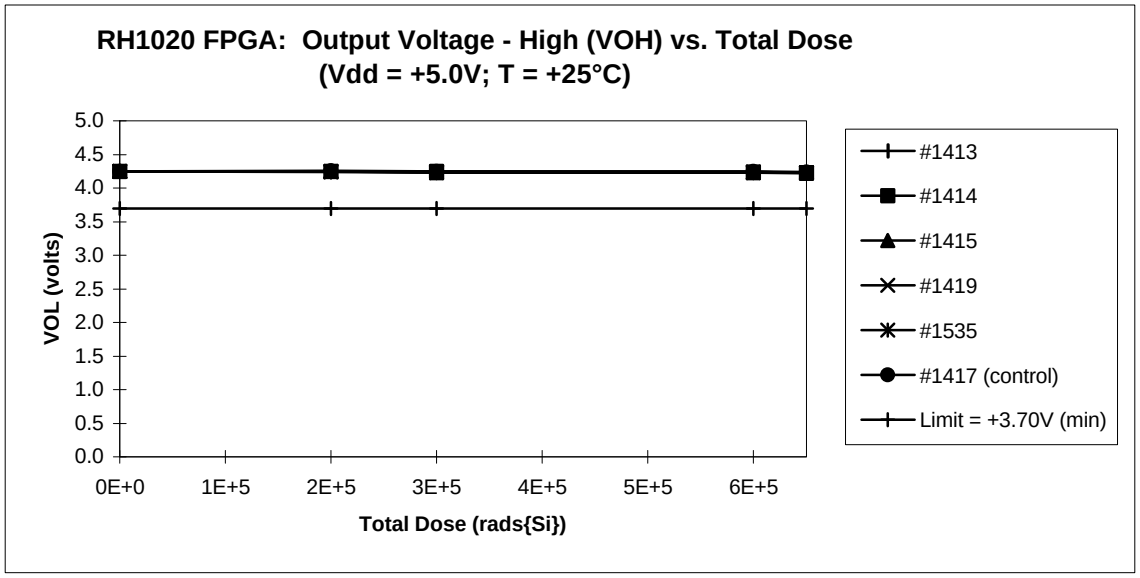

Figure 3a. Output Voltage - High (V_{OH}) vs. Total Dose — Full View

(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}

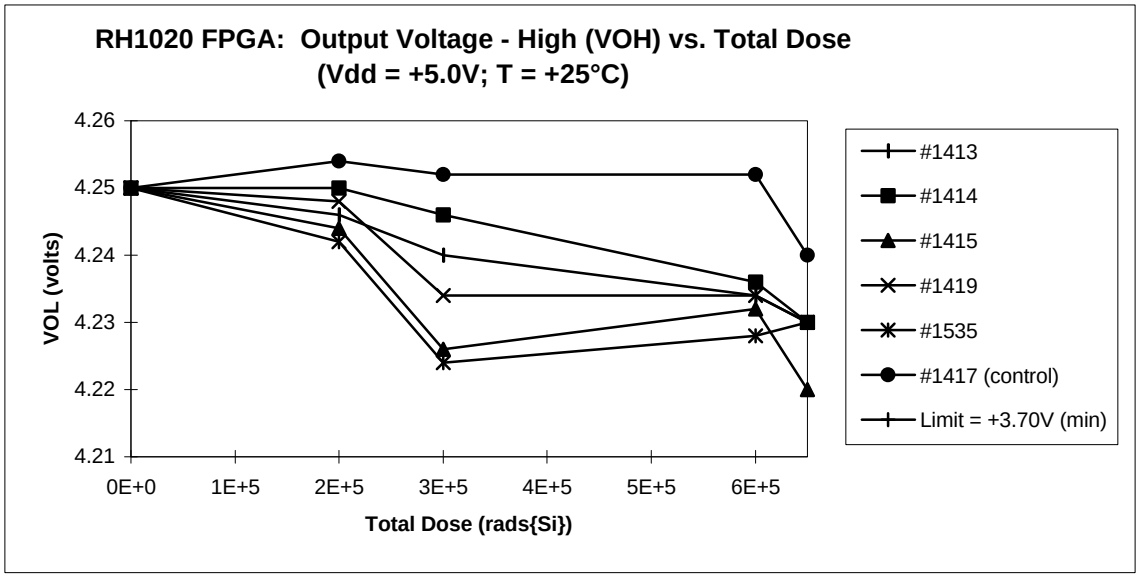

Figure 3b. Output Voltage - High (V_{OH}) vs. Total Dose — Close-Up View

(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}

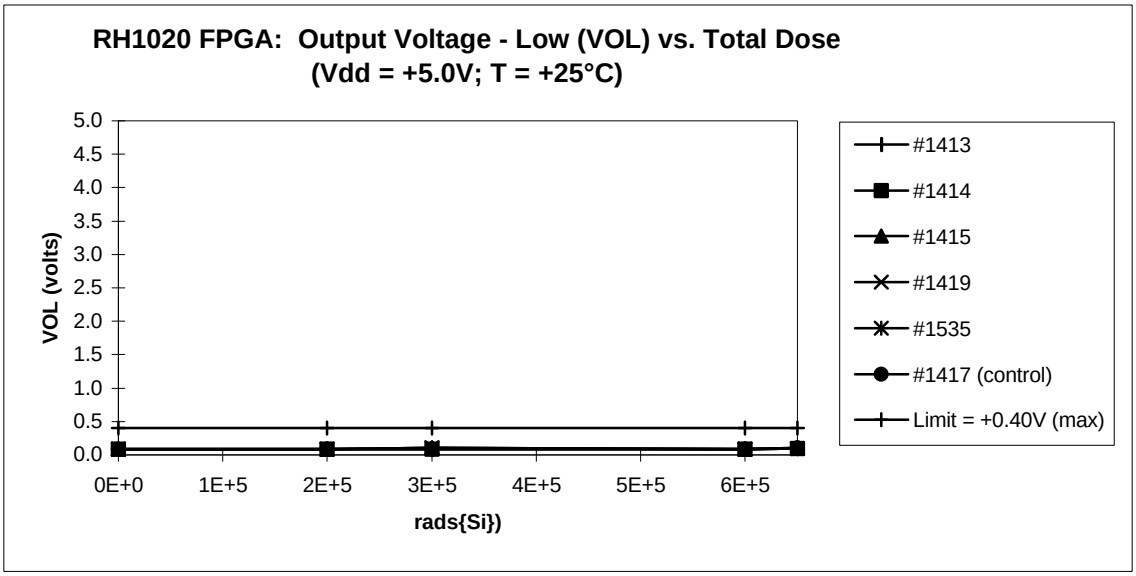

Figure 4a. Output Voltage - Low (V_{OL}) vs. Total Dose — Full View

(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}

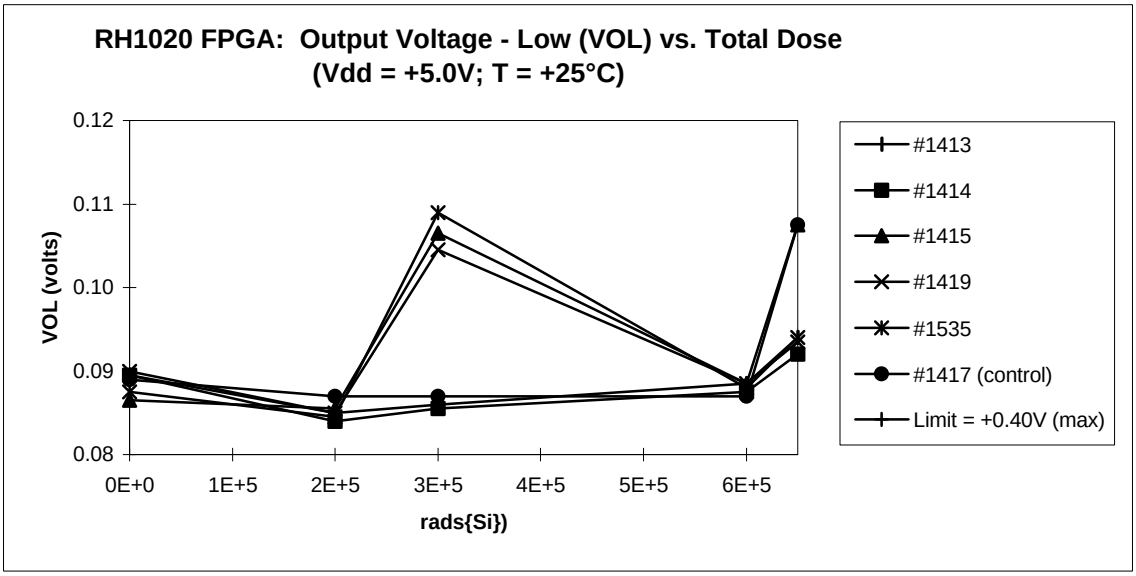

Figure 4b. Output Voltage - Low (V_{OL}) vs. Total Dose — Close-Up View

(final data points are after the 168-hour high-temperature anneal)

{$\mathbf{V}_{DD}$ = +5.0V dc and **T** = +25°C}