

# Programmable Logic Application Notes

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarters column will include some design application notes and some recent radiation test results of interest.

## NEW WWW SITE FOR PROGRAMMABLE LOGIC AND DEVICES

A new WWW site dedicated to the design and use of programmable and quick-turn technologies for space flight applications (<http://rk.gsfc.nasa.gov>). This site is intended to complement this column. As such, the EEE Links columns will be shorter with more information (with a higher level of detail) available on-line. The site is still a bit new and more information is constantly being added with older reports and papers being put on line and new results rapidly being posted.

The site will cover several categories of programmable devices such as FPGAs, PALs, memories such as EEPROMs, and programmable substrates. For each topic area, there are three sub-areas: design application notes, radiation test results, and links to manufacturers sites for access to commercially available information. Two pages are dedicated to technical papers and presentations concerning programmables - typically radiation or reliability information. Other pages include useful information such as links to socket manufacturers, sites with radiation information, general design information, and industry links. Comments and submissions are always welcome.

## CHIP EXPRESS UPDATE

Two rounds of heavy ion tests have been completed on our CX2041 LPGA prototypes. The first round was conducted at  $V_{CC} = 5.0$  volts and these epi-based devices readily latched.

Further testing was performed at  $V_{CC} = 3.3$  volts and the samples latched quickly with Bromine ( $LET = 37 \text{ MeV-cm}^2/\text{mg}$ ). The CX2041 model has embedded SRAM. The CX2030, which does not have SRAM, is planned for testing in February 1998.

As discussed in the last edition, we were building an in-flight radiation experiment. This has been delivered (see notes below) and included QYH530 and CX2041 packaged both in MQFP208's and on a Pico Systems antifuse programmable substrate/MCM.

## RADECS '97 PAPER

"Antifuse FPGA for Space Applications" has been accepted for RADECS '97. *Abstract:* This paper presents total dose and SEE testing data of recent antifuse products. It includes ONO-antifuse FPGAs: A1020B, A1020S, RH1020, A1280XL, A1460A, A14100A, A32140DX and A32200DX. Also included are preliminary results of pre-production metal to metal (M/M) antifuse FPGAs, the I100 and the RHI100. Finally, SEU rate calculations of Actel FPGAs are discussed.

[http://rk.gsfc.nasa.gov/richcontent/fpga\\_content/ad97\\_v3.pdf](http://rk.gsfc.nasa.gov/richcontent/fpga_content/ad97_v3.pdf)

## Recent Test Results on PALs: Cypress BiCMOS 22V10C devices

Here's a summary of some recent heavy ion and proton tests of PALs.

www link:

<http://rk.gsfc.nasa.gov/richcontent/pals/Cypress22v10Sep-97.PDF>

Test mode: Dynamic, 1 MHz, shift register of alternating 1's and 0's

*Protons at UCD (6/97)*

Mfr: Elmo (Cypress die)

Part #: JT22V10-10 ETUFP (Jackson and Tull part number)

Results: Upsets in flip-flops with 63 MeV protons.

Cross-section is  $2E-11$  per flip-flop  
No upsets in combinational logic gates

**Heavy ion tests at BNL (7/97)**

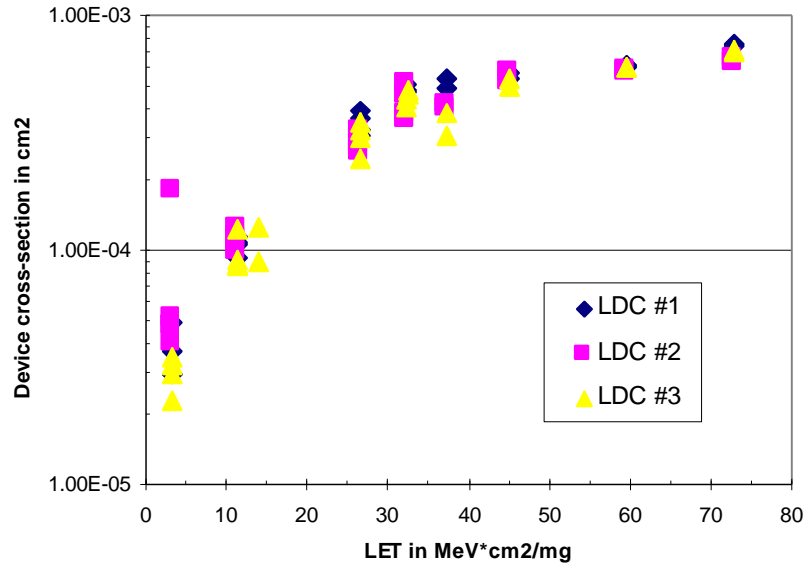
Results for 3 LDCs are graphed below.

LDC #1 002611202

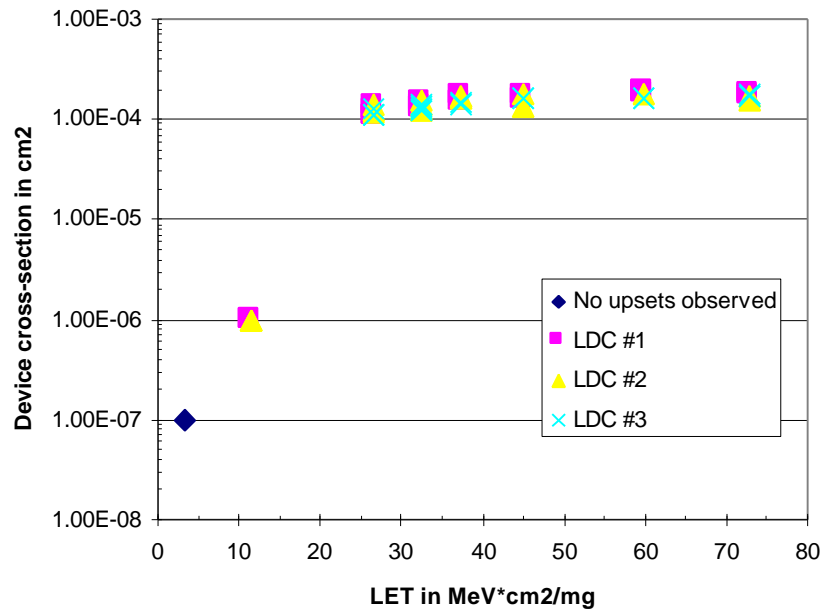
LDC #2 XC34950484

LDC #3 XC349608493

**22V10C PALs - flip-flop cross-section (divide by 8 to get per flip-flop)**



**22V10C PALs - combinational logic cross-sections per device**



## Detecting Asynchronous Loops with Designer

**Abstract:** Current versions of Designer timing analysis software do not automatically notify the analyst of asynchronous feedback loops in their design. These warning were the default for earlier versions such as ALS 2.3.2. This checking can be done as described below.

To make DTAnalyze issue a warning if it senses an asynchronous loop perform the following operation. Under the Options menu, use the Set command to set the variable "showbreakloop" to "1" (without the quotation marks). The Set command setting can be verified by using the Get command, also under

the Options menu, which will print the "showbreakloop" variable's value in the main status window. Now, when a timing analysis is performed, a warning should appear in the main status window indicating any asynchronous loops and which pins were put into a break set

Here's sample output from a simple design using cross-coupled NAND gates to make an RS flip-flop.

```
Variable showbreakloop = 1;  
Pins 'G2:A' has been put into  
STOP set to break loop.
```

## Using Synopsis to Design Flip-Flops for the Radiation Environment

**Abstract:** This application note shows how to use Synopsis automation scripts to control synthesis such that SEU soft flip-flops (S-Module flip-flops) are excluded from the synthesized output. The synthesis can be controlled to either use radiation-tolerant flip-flops (C-Module or C-C flip-flops) or triple-modular redundant (TMR) structures. For the full application note, see [http://rk.gsfc.nasa.gov/richcontent/fpga\\_content/synopsis\\_actel.pdf](http://rk.gsfc.nasa.gov/richcontent/fpga_content/synopsis_actel.pdf).

### Act 3 Technology at 125 MHz

**Abstract:** Simulations were run on a simple circuit to determine the feasibility of running Actel Act 3 devices at 125 MHz (8 nSec cycle time) with two levels of logic between flip-flops and high-slew output buffers were used. The

simulations determined chip-to-chip timing as well as internal timing and were run over a variety of models, speed grades, and environmental conditions.

## Evaluation of 125 MHz Circuits in Act 3 FPGAs

Simulations were run on a simple circuit to determine the feasibility of running Actel Act 3 devices at 125 MHz (8 nSec cycle time) with two levels of logic between flip-flops and high-slew output buffers were used. The simulations determined chip-to-chip timing as well as internal timing and were run over a variety of models, speed grades, and environmental conditions.

Here are the results:

Device	Speed	Cond	t <sub>SU</sub>	t <sub>H</sub>	REG REG	CLK PAD
A1425A	-1	MIL	2.9	-1.0	10.4	10.4
A1425A	-2	MIL	2.9	-1.4	9.1	8.7
A1425A	-2	COM	2.6	-1.2	7.9	7.5
A1425A	-3	MIL	1.8	-0.3	8.2	8.7
A1425A	-3	COM	1.5	-0.3	7.1	7.5
A1460A	-1	MIL	3.3	0.4	10.9	11.7
A1460B	-1	MIL	2.5	1.6	10.1	11.7
A1460BP	-1	MIL	2.5	1.6	10.1	11.7

An attempt was made to place and route the A1425A-2, with military derating, using timing-driven place and route with a constraint of an 8 nSec clock period. The attempt failed with a negative slack of -1.2 nSec.

## CONCLUSIONS AND NOTES

1. There are timing differences between the A1425A and the A1460A, with the A1425A being faster in several categories, with about a 5% improvement in register-to-register performance.
2. 125 MHz operation does not appear feasible in this configuration with two logic levels between flip-flops.
3. The 'B' series devices have a very significant positive hold time.
4. Getting data on-chip at high speeds seems feasible. Note, however, that the SEU-soft I/O-Module flip-flops must be used.
5. Getting the data off-chip is also a critical path and will limit system performance.

## PGA to QFP Work-a-round for Designer

A problem was encountered with Designer 3.1.1 when repackaging an A14100A PGA257 design to a CQFP256 design. Actel has stated that this will be fixed in the next revision of software and has quickly provided the following work-a-round. This bug did not show up in Designer 3.0 and it appears to be limited to versions 3.1 through 3.1.1U1.

The bug is that the software doesn't save any "compatible" die or package changes in the database. If you changed to a package or die that forced you to re-layout the design, then the information gets saved properly. The problem only occurs if you change to a package or die that doesn't require a re-layout, a compatible die change. This feature is used, for example, if a prototype is done in a PGA package and a flight QFP device needs to be programmed - obviously, no die changes eliminates the need to rerun the timing analysis and possibly modify the design or place and route.. This is a general software bug, not related to the type of device being used.

The procedure is to manually set the "package" variable, then re-generate the AFM file. To do this:

1. First, verify which package is currently selected. In Designer, go to the top level Options menu and select Get. Under "Variable:", type in "package" (without the quotes), then select OK. In the status window below, you will see either  
  
Variable package = pga257 (if the 257 pin CPGA package was selected) or Variable package = qfp256 (if the 256 pin CQFP package was selected)
2. To set the package type manually, in the Options menu, select Set. Under "Variable:", type in "package" (without the quotes). Under "Value:" type in either pga257 or qfp256, depending upon which one you want, then select OK.
3. After changing the package, nothing will happen. The display at the bottom of the screen will still show the old package, but if you use the Get command as in step 1) above, the value of the variable "package" should show the new value. Always verify

that the variable "package" was set properly, as we don't check the variable values very carefully when they are entered manually.

4. Re-generate the AFM file by clicking on the Fuse button. You can verify that none of the fuses changed by "diffing" the old and new AFM files. Only one line should be different and that is the line that contains the package type. If you are VERY, VERY careful, you can edit the AFM file directly to change the package type, but I am reluctant to recommend this, as it is so easy to make mistakes when manually editing files.

## Metastable States

### Introduction

Normally a flip-flop is one of two states; either storing a logical '1' or a '0'. These states are stable as flip-flop elements employ positive feedback. In properly designed and functioning systems, all flip-flop parameters are met and the device operates normally. The key parameters are setup time, hold time, and pulse width (for clocks, presets, clears, jam loads, etc.). If these parameters are violated, as when an asynchronous input is fed into a flip-flop without meeting the setup and hold times, or when a runt pulse is input into the clock or asynchronous preset/clears, the flip-flop may go "metastable."

Device behavior in the metastable state may manifest itself as increased CLK -> Q delay, device output being a non-logic level, or an output switching and then returning to it's original state. Theoretically, the amount of time a device stays in the metastable state may be infinite; in practical circuits, there is sufficient noise to move the device output of the metastable state and into one of the two legal ones - however, this time may be large with respect to the available timing slack in the circuit resulting in a system failure. Factors that affect a flip-flop's metastable "performance" include the circuit design and the process the device is fabricated on. It turns out that by allowing sufficient settling time the MTBF for a well-designed system with asynchronous inputs can be made extremely low. This is possible since resolution time is not linear with increased circuit time and the MTBF is an exponential function of the available slack time. This can be seen in the following equation:

$$MTBF = e^{(K2*t)} / (K1 \times F_{clock} \times F_{data})$$

where  $t$  is the slack time available for settling,  $K1$  and  $K2$  are constants that are characteristic of the flip-flop, and  $F_{clock}$  and  $F_{data}$  are the frequency of the synchronizing clock and asynchronous data. By this equation, it is clear that an increase of ' $t$ ' has an exponential effect on the MTBF. The two constants account for the two key characteristics of a flip-flops metastable behavior: the size of the window (usually sub-nanosecond and the time to get out of a metastable state that is a function of the gain-bandwidth product of the device).

### Example

Here are some calculations we did using the Chip Express CX2001 technology, based on their flip-flop parameters and example in the CX Technology Design Manual, as a look at how this technology performs. The CX2001 series uses a channeled module architecture (gate array) with each module consisting of three 2:1 muxes and an AND gate (a bit differently set up than Act 1 but not all that dissimilar). There are no hardwired flip-flops in the architecture; these are available in all Actel families except for Act 1, in Xilinx, Lucent, etc., devices. This sample calculation uses a 50 MHz clock, a 10 MHz average incoming data rate, and the available extra settling time is the independent parameter.

extra delay (nsec)	MTBF (sec)	MTBF (years)
1	448.2e-6	14.2e-12
2	180.8e-3	5.7e-9
3	72.9e+0	2.3e-6
4	29.4e+3	933.2e-6
5	11.8e+6	376.5e-3
6	4.7e+9	151.9e+0
7	1.9e+12	61.2e+3
8	779.6e+12	24.7e+6
9	314.5e+15	9.9e+9
10	126.8e+18	4.0e+12
11	51.1e+21	1.6e+15
12	20.6e+24	654.8e+15
13	8.3e+27	264.1e+18
14	3.3e+30	106.5e+21

### DISCUSSION

With the 20 nSec period, let's say we allocate 10 nSec of additional delay for the first synchronizing flip-flop to recover; this leaves 10 nSec for  $clk \rightarrow q$ , routing delays,  $t_{su}$ , and any unfavorable  $t_{skew}$ . Since the flip-flops in a

synchronizer will be physically close, this is probably very conservative. As can be seen from the chart, 10 nSec of slack will give a pretty reliable circuit.

This information and references on this topic is available at:

<http://rk.gsfc.nasa.gov/richcontent/General%20Application%20Notes/mestablestates/MetastableStates.htm>. Later, we'll be adding parameters for many manufacturers and a specialized calculator, for predicting MTBF for a particular design configuration.

### Upcoming Tests

We're planning our next series of radiation tests and plan to include some new programmables. Included will be the Dyna Chip DL5000, the 0.35  $\mu m$  QuickLogic pASIC 3 amorphous silicon antifuse FPGA, a standard evaluation circuit for the QYH500 series, including the digital phase lock loop (DPLL), and the UTMC amorphous silicon antifuse PAL. We also hope to include the Xilinx XC400XL devices and the Actel 42MX09. It's interesting to see the newer devices making the move to 3.3-volt systems.

### Recent TID Test Results

Below are some charts from recent total dose tests. It is noted that radiation-tolerant performance is seen in the A14100A/MEC device (5 krads(Si)/Day) and lower than typical performance is seen from the A1280A/MEC device (1 and 2 krads(Si)/Day).

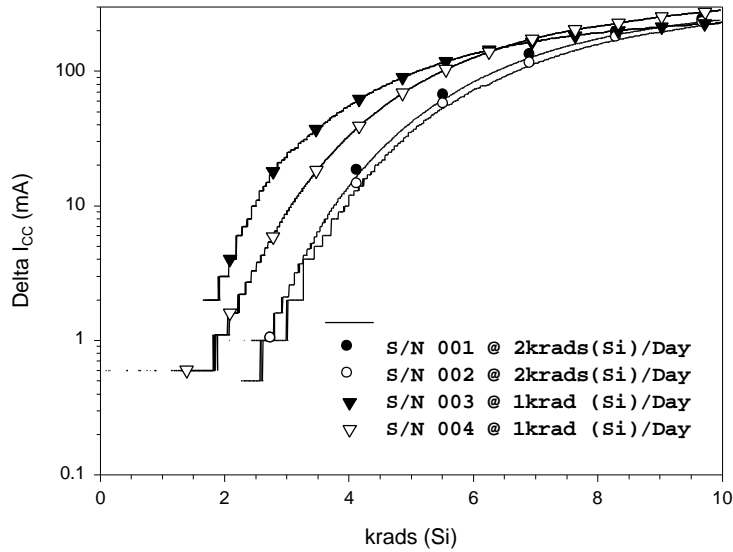
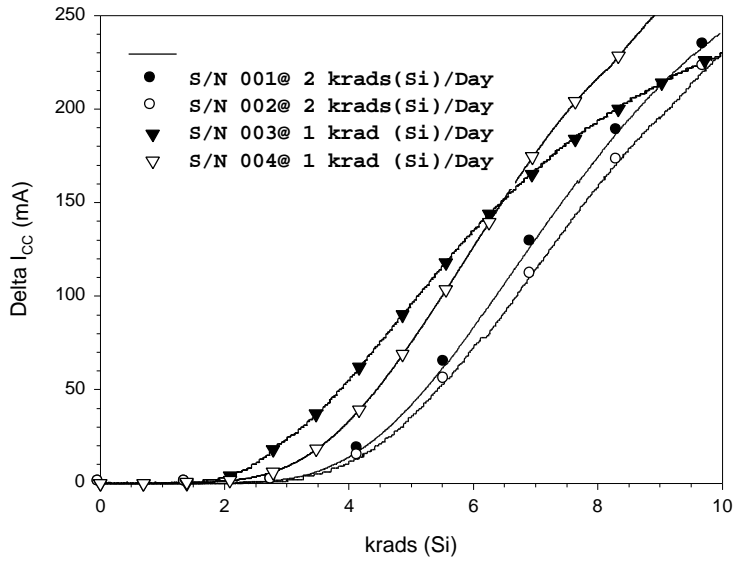
### In-Flight Experiment

We have completed and shipped our second in a series of in-flight radiation experiments. A photograph of our flight spare unit is at the bottom of this report. This experiment includes the MKJ911 metal-to-metal antifuse FPGA technology development vehicle, the Chip Express QYH530 and the CX2041 (One-Mask) quick-turn ASICs, the amorphous silicon antifuse UTMC UT22VP10 PAL, and the Pico Systems amorphous silicon programmable substrate in an MCM with Chip Express ASICs and Harris CD4050B die.

### References and Acknowledgements:

Ken LaBel NASA/GSFC <http://flick.gsfc.nasa.gov>  
Anita Jeong - Actel Corp.

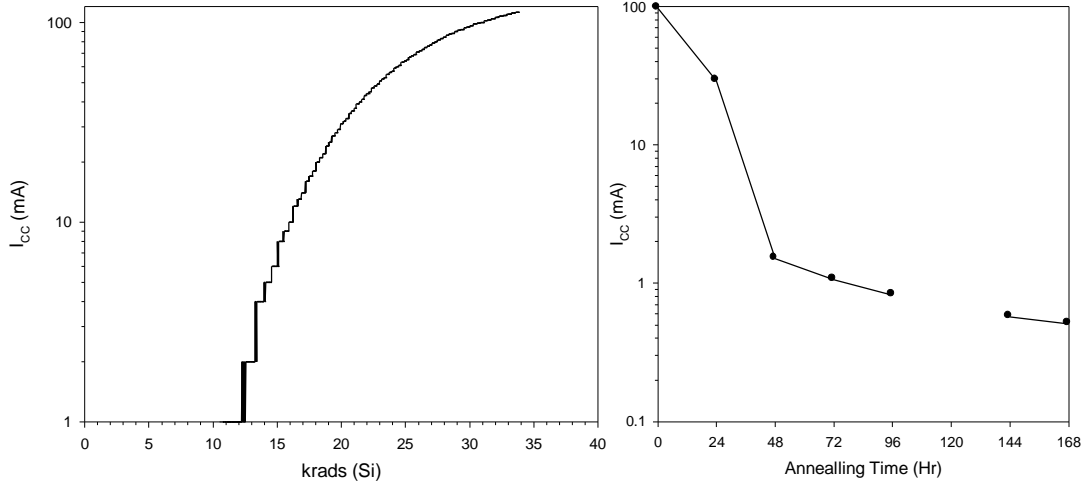
MAP A1280A TID TEST  
 NASA/GSFC  
 Dec. 29, 1997  
 2 krads(Si)/Day for S/N 001, 002  
 1 krad(Si)/Day for S/N 003  
 D/C 9729  
 L/C U1H428



Note: After some unbiased annealing (facility accessibility) S/N 001 was functional and had an I<sub>cc</sub> of ~ 25 mA. Under a powered, room temperature anneal, S/N 001 was tested continuously for several days and I<sub>cc</sub> dropped to ~18 mA.

EO-1 A14100A/MEC TID Test  
 D/C 9712  
 UCL046  
 January 5, 1997  
 NASA/GSFC  
 5 krad(Si)/Day

100C Annealing Data  
 January 12, 1998  
 NASA/GSFC



NOTE: The logic threshold had a slight increase of approximately 100 mV after irradiation - it decreased approximately 50 mV after the 168 hour, 100C anneal. Values ranged from 1.19V to 1.29V.

## DITS-2 S/N 001 (Flight Spare)

