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ADVANCED MICROCIRCUIT EMULATION (AME) PROGRAM – DEVELOPING NEXT GENERATION EMULATION TECHNOLOGY

Harvey M. Hanson, Space and Naval Warfare Systems Center, San Diego, CA; Donald F. O'Brien, Alex Melnikow, Defense Logistics Agency, Ft. Belvoir, VA; James S. Crabbe, Les R. Avery, Sarnoff Corporation, Princeton, NJ

Abstract: This paper presents the Advanced Microcircuit Emulation (AME) Program, a Defense Logistics Agency (DLA) managed tri-service effort that is developing the next generation of form, fit, and function (FFF) microcircuit emulation capability. This program is operated independently from the Defense Supply Center's (DSCC) Generalized Emulation of Microcircuits (GEM) Production Program. AME's technology scope includes advanced digital devices, microprocessors/microcontrollers, memory, analog, hybrids, and assemblies employing AME technologies. The paper begins with a brief review of the program's background and drivers. It continues by detailing AME's program structure, current status, and concludes with future plans.

Background: Accelerating microcircuit technology implementation results in microcircuit family lifecycles as short as eighteen months in the commercial sector. The transition of dominant microcircuit market forces from the historic DoD consumption to a computer/telecom focus also contributes to ever shrinking technology lifetimes. The net result of rapid product terminations and altered market forces is a reduction in the availability of microcircuits traditionally used to support DoD requirements. The Defense Logistics Agency is responsible for microcircuits through its field activity DSCC, the DoD's microcircuit inventory control point (ICP). Each non-fillable purchase request (PR) lowers the support level to the services and weapon systems. Non-filled PRs ultimately incur additional expense to the customer and lower our nation's defense readiness. More than a decade ago, DLA and DSCC recognized these impacts and initiated the GEM Program to develop technology to mitigate the impact of microcircuit Diminishing Manufacturing Sources And Material Shortages (DMSMS) to DoD. GEM is now a fielded Production Program providing required parts throughout DoD, weapon system contractors, and the general defense community. There continues to be interest from the defense community in obtaining non-procurable microcircuits beyond GEM's technology.

Initiation and Structure: Microcircuit problems encountered in both weapon system production and support environments were accumulated in visits to DoD organic installations, the ICP, and weapon system contractors over the past several years. The problems were classified into the broad categories cited previously in the abstract. It was determined that the optimum method to address these new troublesome requirements would be an advanced development program independent of the current GEM program and its contract vehicle. The objective of the AME Program is to adapt modern microcircuit manufacturing and design processes to provide an ongoing rapid, economical, high quality microcircuit emulation capability to support the non-procurable requirements of the ICP, Original Equipment Manufacturers, and weapons systems. The AME Program was procured through full and open competition by the DSCC. The Request for Proposals, issued in late 1996, was structured in a Broad Agency Announcement (BAA) format with an optional BAA Proposal Abstract process. The results of the Government's Proposal Abstract review were not binding and proposers receiving an unfavorable abstract review could submit a full AME proposal if they desired. Multiple Abstracts and full Proposals were received in response to the BAA. An award was made to Sarnoff Corporation in June 1997 for a five year AME effort. AME is managed by the DLA, with the Contracting Officer/Agency being at the DSCC. The Contracting Officer's Technical Representative (COTR) is located at Space and Naval Warfare Systems Center, San Diego. AME is not contractually tied to the GEM Program in any manner; GEM is directly managed and contracted by DSCC. The AME Program is not a production program; it is developing and demonstrating advanced emulation capability.

Implementation: The AME implementation model is to demonstrate capability in successive releases of increasing complexity and capability. Each technology release will be integrated into a suitable military quality program to ensure the capability meets the requirements of the target market, ICP, and weapon systems. Technology developments will be verified through the design and fabrication of demonstration devices. These microcircuits will be tested at the part level both in-house at the Sarnoff facility and at certified independent microcircuit test facilities. AME has a range of arrays that initially include smaller elements for each technology release, with larger arrays following shortly. This technique allows more rapid verification of both design and fabrication technologies at any given design feature size.

Challenges: The principal challenges faced by AME are adapting design techniques to emulate larger microcircuits, progressing to a smaller geometry emulation process, efficiently testing large scale devices, and adapting to the limited technical data environment associated with the typical Application Specific Integrated Circuits (ASICs) in DoD systems. These challenges will be partially met through increased use of Hardware Description Languages in design and test environments, e.g. VHSIC (Very High Speed Integrated Circuit) Hardware Description Language (VHDL) and Verilog. These technologies reduce the cost and time required per gate to perform emulation. Closely integrating the design and test environments will also reduce the cost and increase the speed of a given emulation.

Technology: As mentioned above in the abstract, AME has a broad microcircuit scope. In addition, its scope includes Application Specific Integrated Circuits (ASIC), Digital to Analog Convertors, Analog to Digital Convertors, and engineering services related to replacement of electronic assemblies or elements thereof with emulated FFF devices developed in AME. AME is implemented with both Bipolar and Complementary Metal Oxide Semiconductor (CMOS) technologies. The current efforts in AME involve both a 1.2 micron and hybrid 0.8/1.0 micron. These smaller geometries enable emulation of parts with faster transition times and higher gate counts. The hybrid 0.8/1.0 micron has

0.8 micron gate length with 1.0 micron features elsewhere. The 0.8 micron effort was initiated far ahead of original program schedule due to the success of the 1.2 micron technology. A high voltage process is also under development as a part of AME. This process has standard voltage logic with 100-Volt outputs. This capability is useful in for driver circuitry that is employed throughout DoD systems.

Current Status: A number of gate arrays are either designed or are currently being designed in AME. Currently, an 100,000-gate gate array is being designed. This array will be useful for emulation of both custom and larger "standard" digital microcircuits. An integral part of the AME has been successful implementation of a triple level metalization process for interconnect on AME microcircuits. This three level capability was prerequisite to implementing advanced emulation. Another portion of the current effort is devoted to developing accurate design models for incorporation into the design library/system. These models are critical for accurate FFF emulation of the final microcircuit. Inadequate models would result in unnecessary emulation cycles to meet the original parts performance. Sample small circuits have been implemented in the 1.2 micron technology. These circuits are proven designs that have been previously implemented in another process. These devices will offer a first look at the 1.2 micron performance in a finished package.

Facilities and Capitalization: Sarnoff Corporation was originally the RCA Corporate Laboratory. When GE bought RCA they donated Sarnoff to SRI International. Sarnoff Corporation has been a wholly owned subsidiary of SRI International since 1987. Due to its corporate heritage, Sarnoff has both extensive modern microcircuit design tools and an in-house fabrication facility. The fabrication facility is flexible, supporting a number of programs outside of emulation. Sarnoff has made a substantial corporate commitment to maintain and enhance the facilities. Sarnoff is in the process of enlarging their IC Center and has been acquiring and installing multiple major pieces of processing equipment every year. AME benefits from these enhancements, enabling the program to move forward to ever more advanced processes.

Plans: AME's roadmap includes progressing to pure 0.8 micron process technology, smaller than 0.8 micron effective gate technology, larger emulation arrays, linear, and mixed mode emulation. These technologies will be implemented based on the same successful model as earlier emulation technologies.

Conclusion: AME technology is a complementary tool to all other options available to address DMSMS, e.g. Aftermarket, redesign, scavenging, remanufacture, system retirement, COTS, etc. No single solution is capable of alleviating the entire DMSMS problem. AME technology should be considered as one more tool in a successful balanced approach to DMSMS. AME has the well known advantages of rapid schedule, high quality devices, no documentation changes, and cost effectiveness. The AME Program Management and COTR are very much interested in learning your DMSMS challenges and are always willing to discuss your requirements. All challenges are used in our future planning for AME.