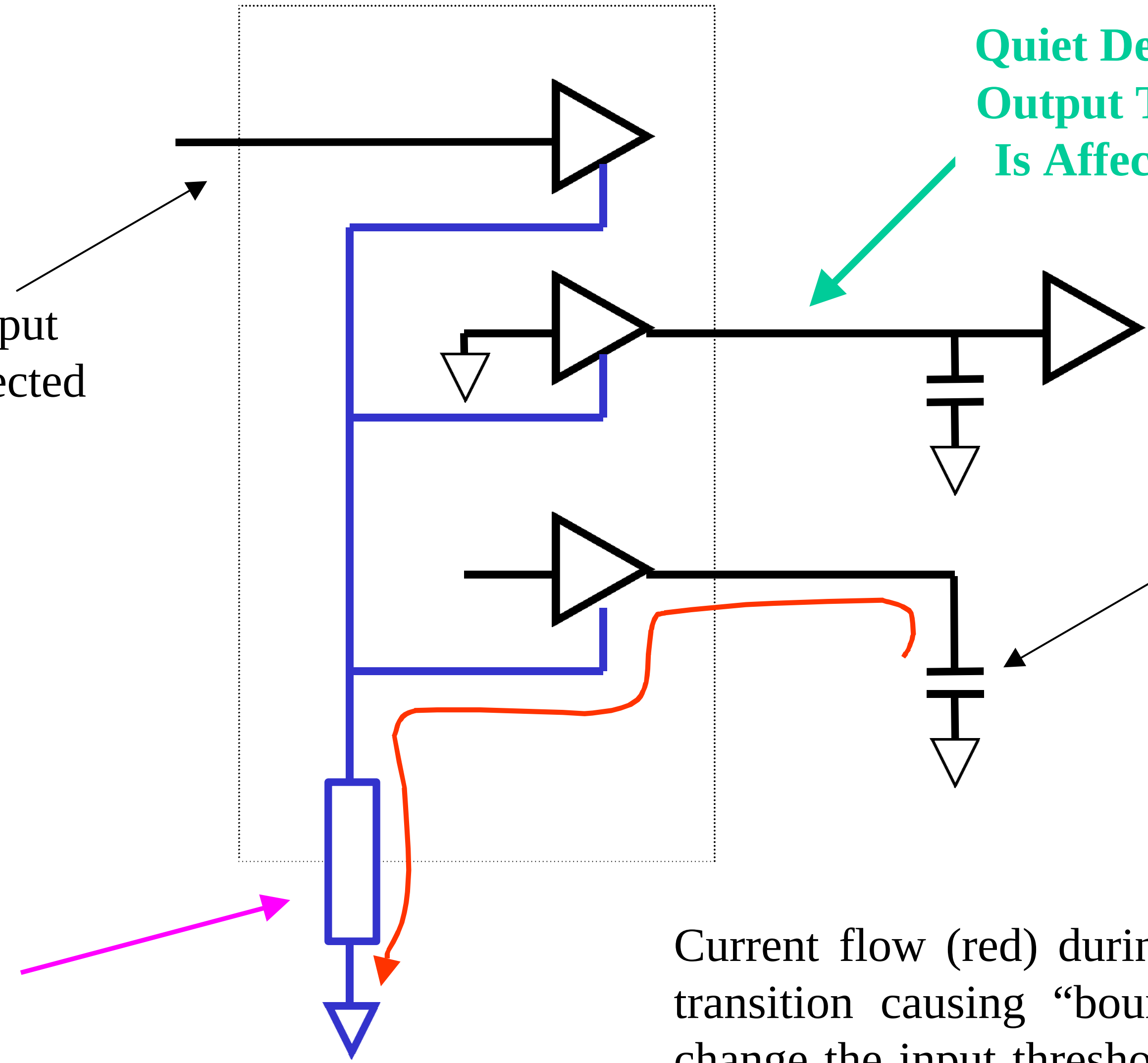
Ground Bounce

(and it’s dual, V_{DD} Bounce)

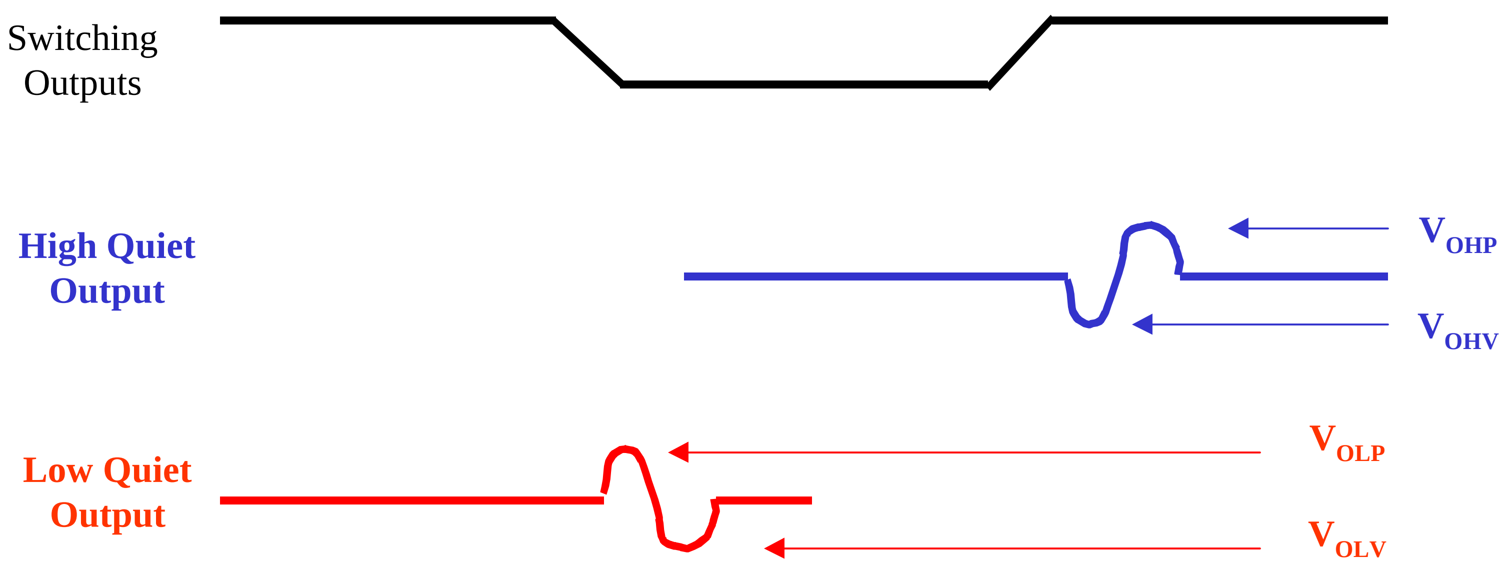
Concept of Ground Bounce



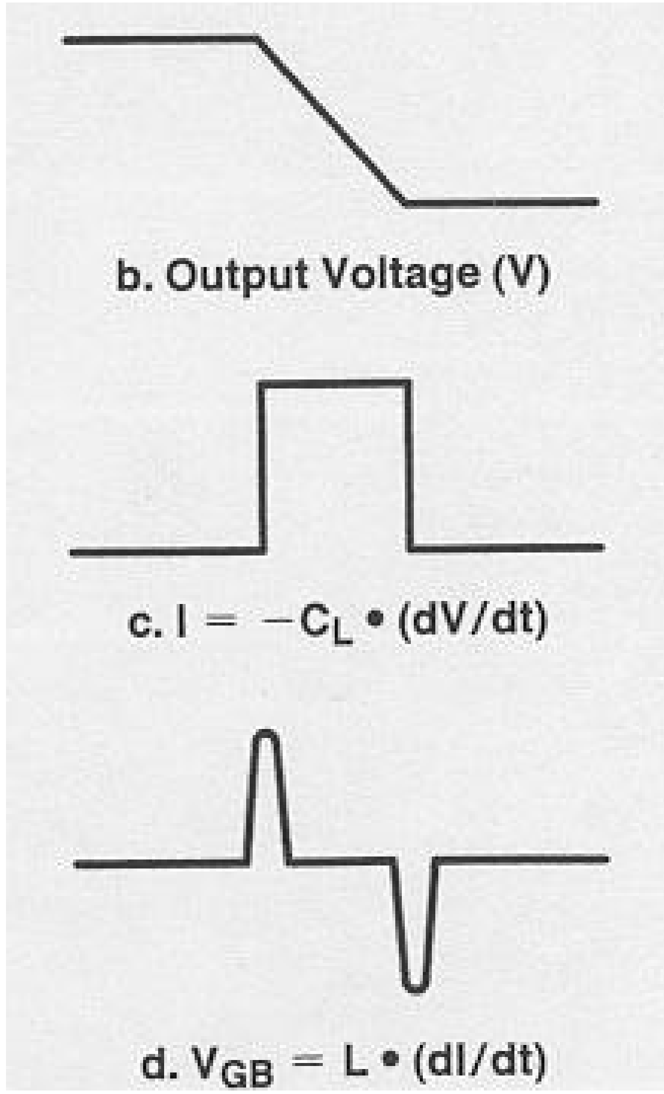
Current flow (red) during a high to low transition causing “bounce.” This can change the input thresholds to the device as well as result in output pulses being transmitted to a receiver.

Ground Bounce - Definition

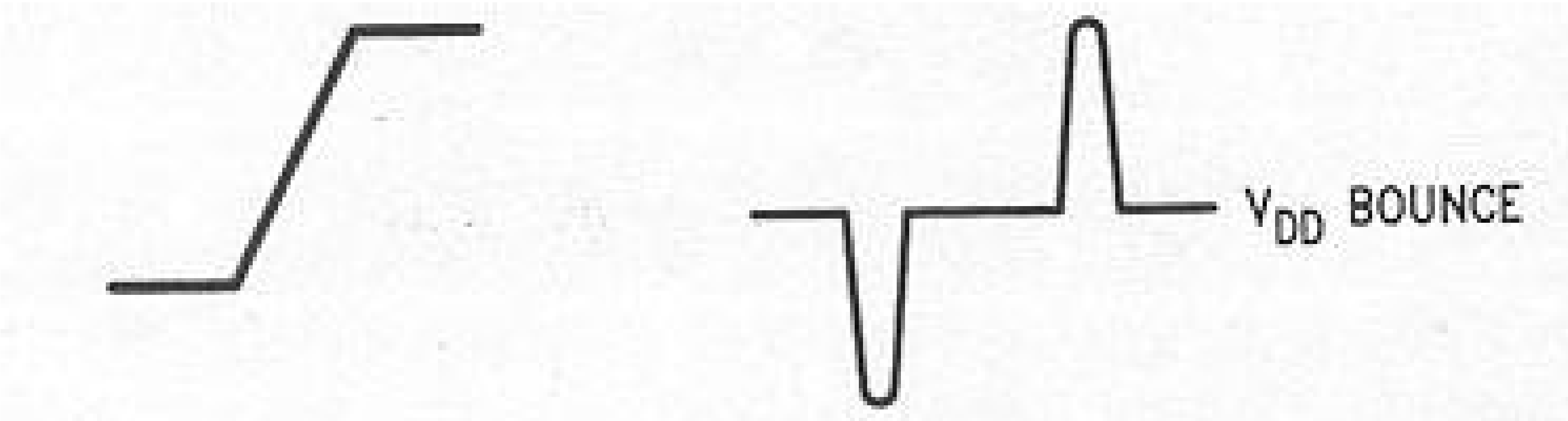
- Noise on a ‘quiet’ output.
- Voltage with respect to ground.



Ground Bounce - A Closer Look

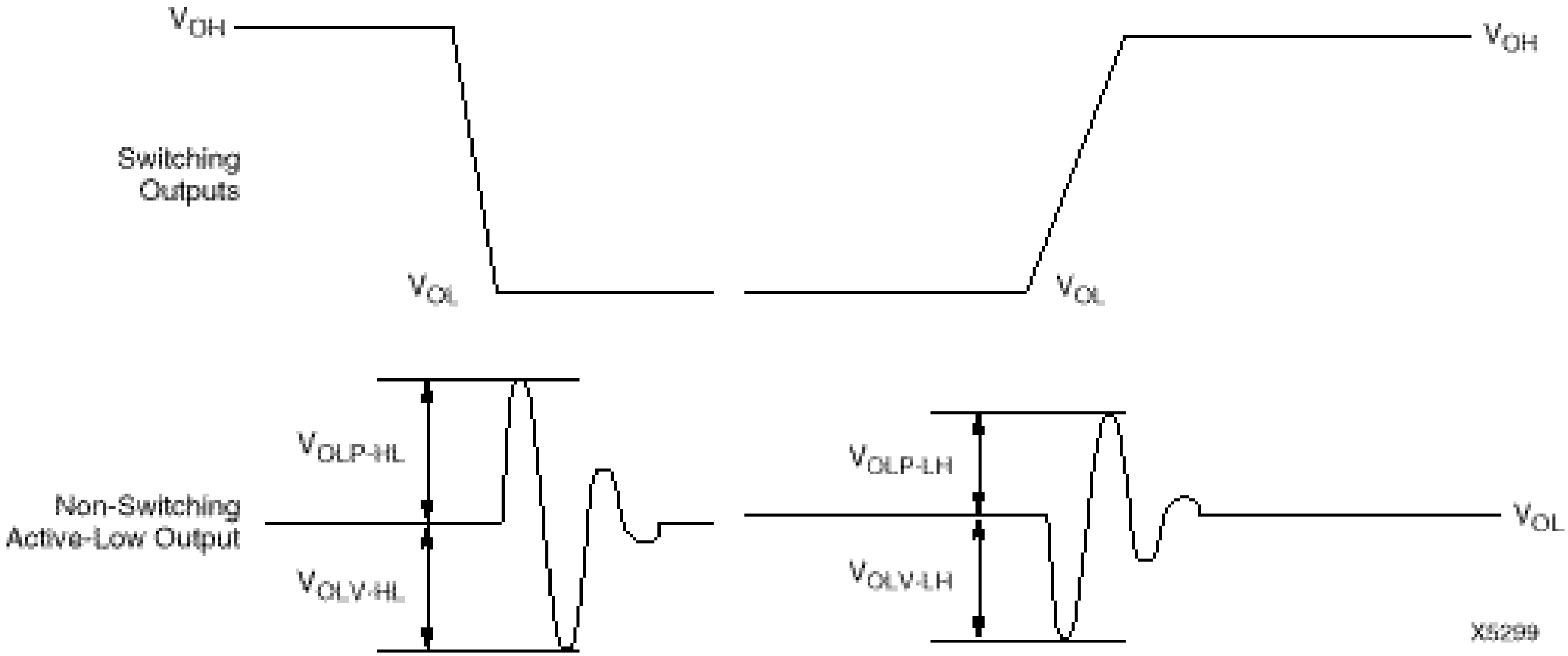


V_{DD} Bounce



Ground Bounce - Definition

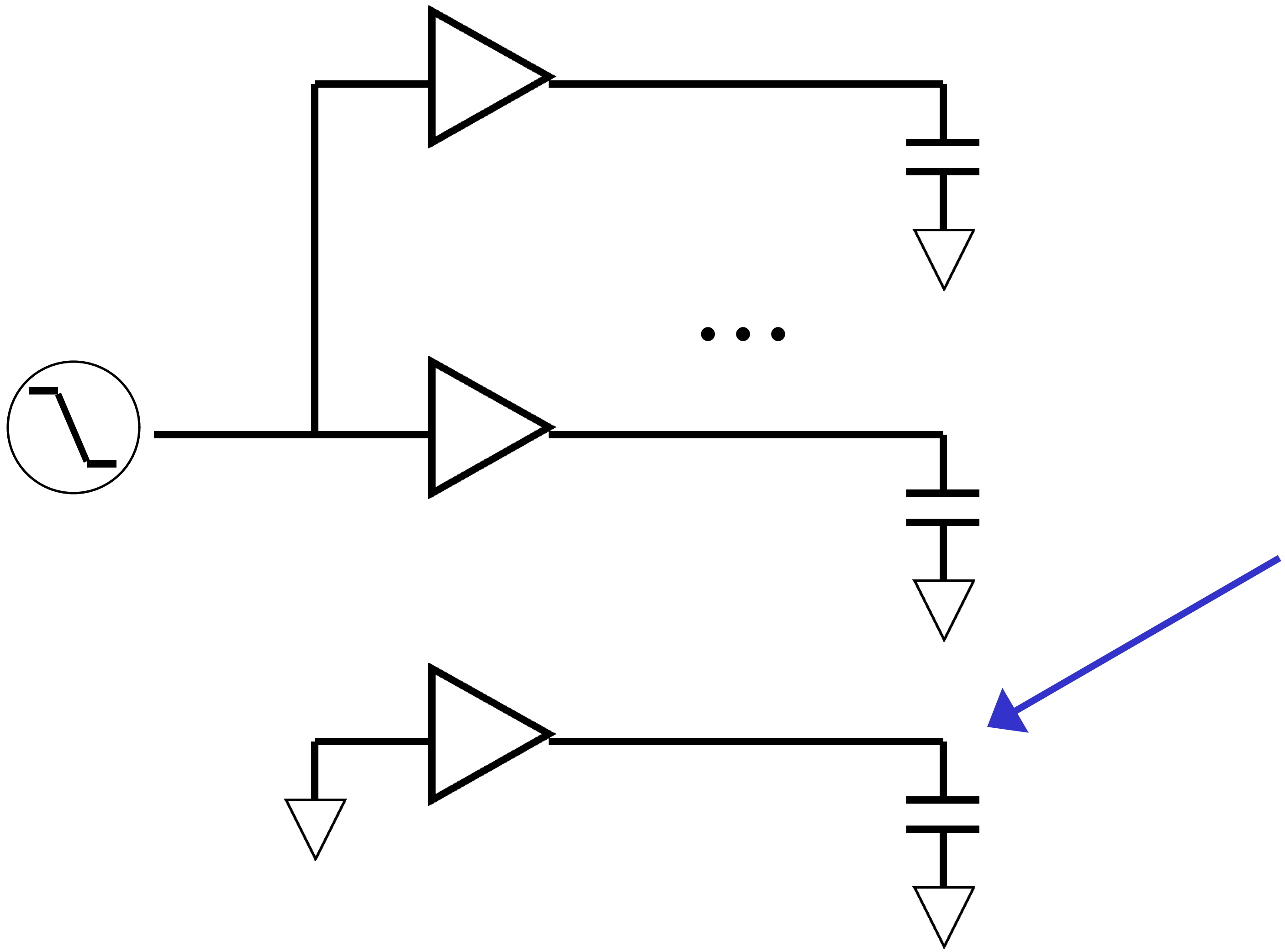
Xilinx Terminology



Ground Bounce - Measuring

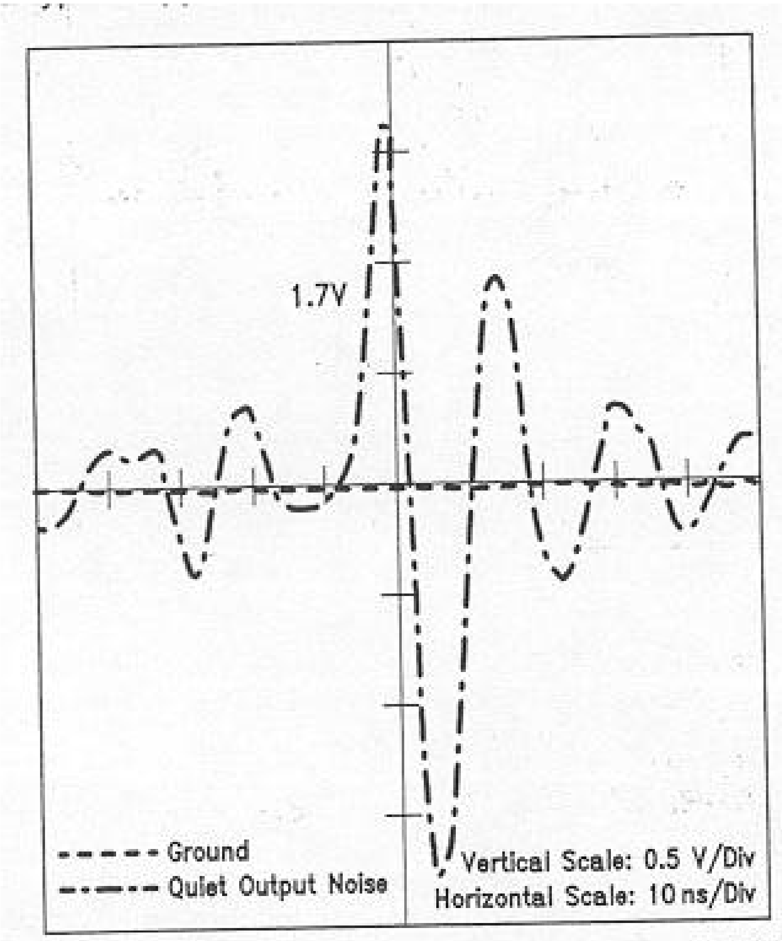
- Measured on pin with greatest noise.
- Worst-case pin usually furthest from ground.
- V_{OLP} and V_{OLV} are measured on a quiet line that is a ‘0’; switching outputs transition from high to low for ground bounce.
- V_{OHP} and V_{OHV} are measured on a quiet line that is a ‘1’; switching outputs transition from low to high for supply droop.

Ground Bounce - Measuring

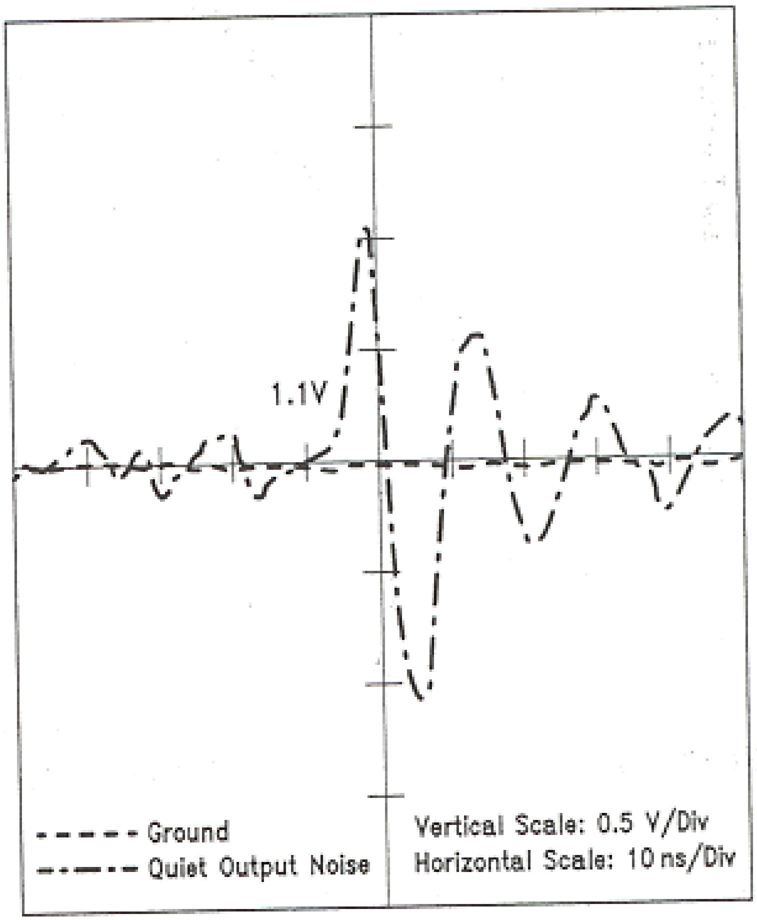


Ground Bounce - Measuring

Worst-Case vs. Best-Case Pin



Worst-case



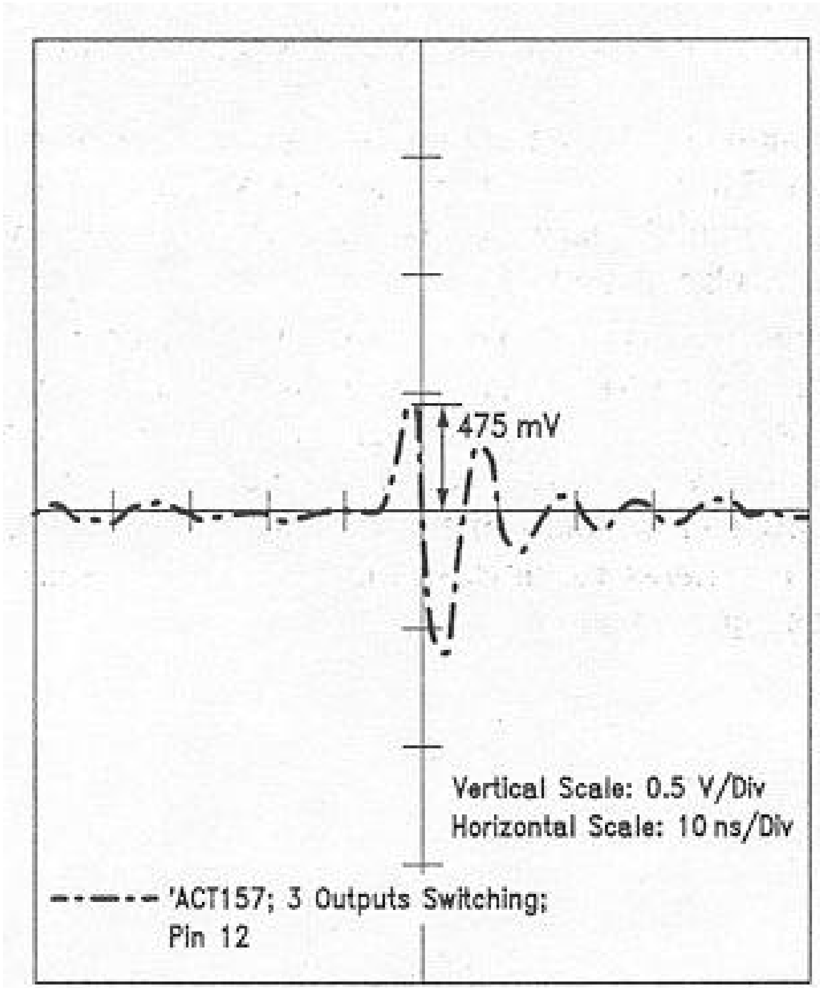
Best-case

Ground Bounce - Measuring

- Design system and test equipment to support measurement of ground bounce
  - Control of patterns
- When using reprogrammable devices
  - Special patterns can be loaded to exercise the I/O buffers and measure ground bounce.

Ground Bounce - Sample Data

‘ACT157 - 3 Outputs Switching



Ground Bounce - A Real Life Problem
HX6256: 256K SRAM

The 256K SRAM in the 28 lead flat pack does not provide a satisfactory ground connection for operation in TTL mode for the Read conditions listed in datasheet HX6256.

The issue arises due to inadequate on-chip power bussing. Various address changes, pre-charge pulses, and switching outputs create a considerable amount of drawdown on the power bussing. Functional performance is achieved by having adequate grounding on the package (ex. Maintaining equivalent package and board grounds). **<u>The 28-lead package in correlation with the 256K SRAM has demonstrated on-chip ground bounce</u>**, which occurs when switching all addresses simultaneously; this situation could cause the device to enter into a state of oscillation.

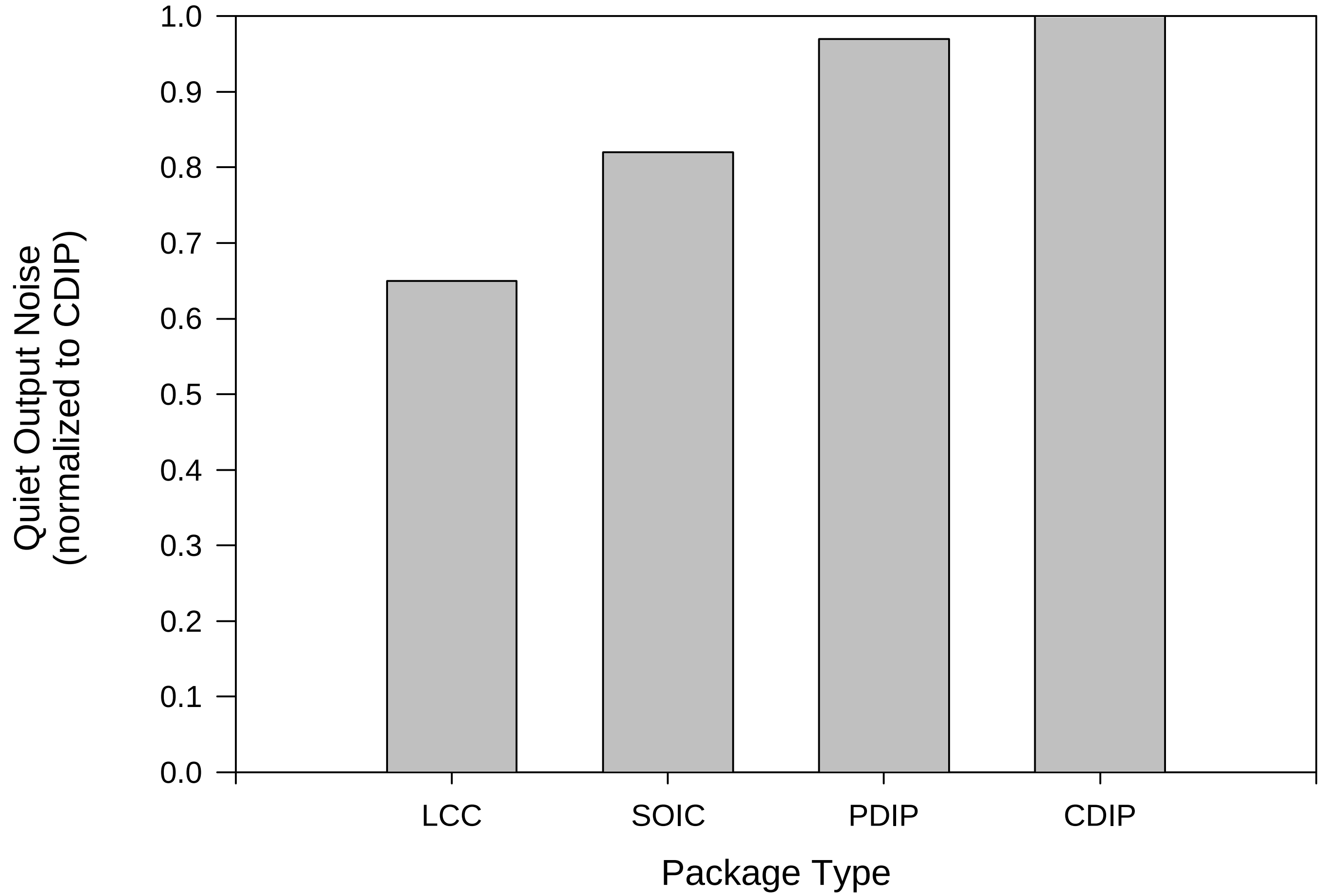
Toggling the NOE pin coincident with an address change could cause the chip to enter oscillation if all of the inputs are toggled together.

Ground Bounce: Package

Lead Inductance

14-pin plastic DIP	8 nH
68-pin plastic DIP	35 nH
68-pin PLCC	7 nH
Wire bonded to hybrid substrate	1 nH
Solder bump to hybrid substrate	0.1 nH

Ground Bounce: Package



<u>Note</u>
CDIP inductance =20 nH
LCC package = 2 nH;
Difference in ground bounce < 35%

National AN-640

Ground Bounce: Loading

- Xilinx
  - Additional capacitance doesn't affect magnitude of the bounce, just duration
  - Resonant Frequency
    - Minimum load, fastest outputs: 340 MHz
    - 50 pF: 90 MHz
    - 150 pF: 40 to 60 MHz
- Agilent
  - Larger the capacitance, the larger the bounce

Reducing Ground Bounce

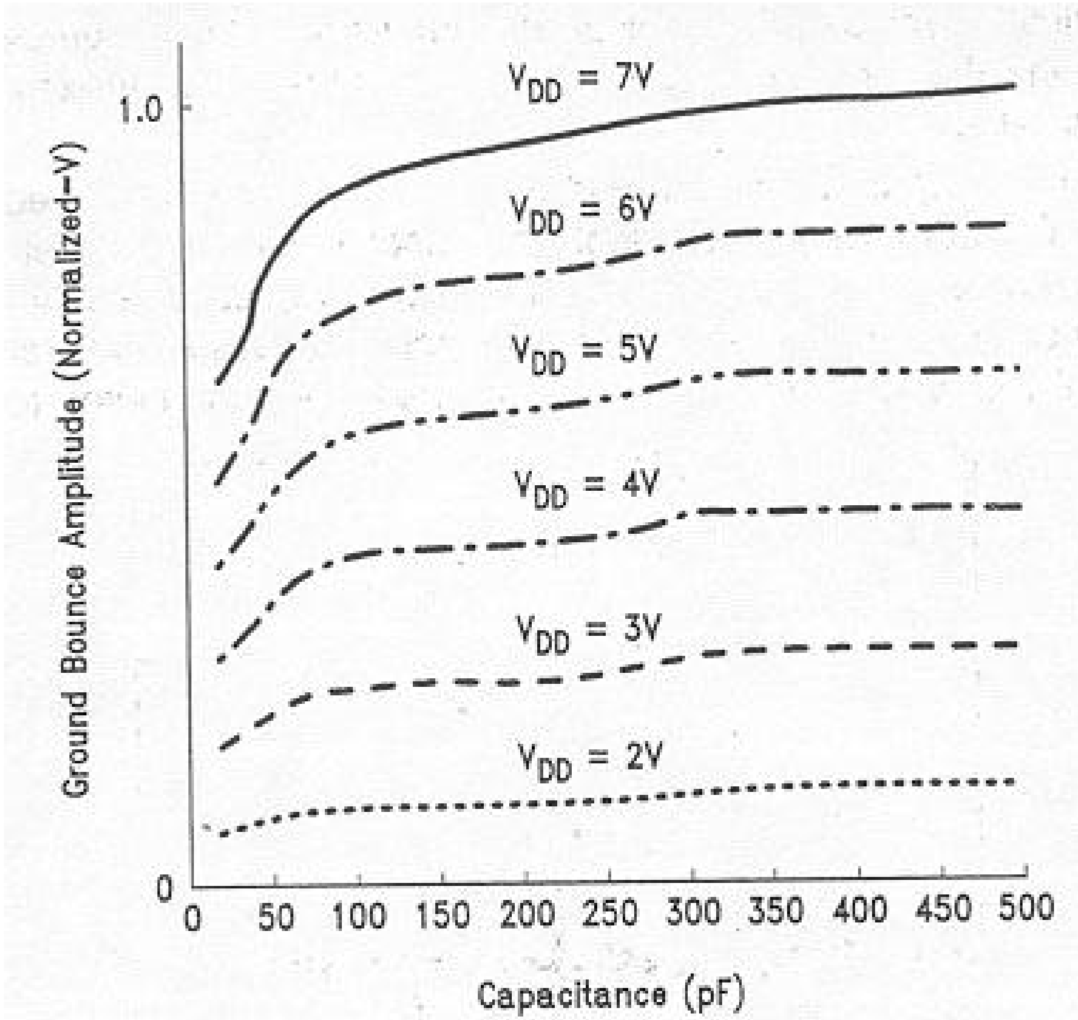
- Use low slew outputs unless needed
- Don’t group SSO’s together; break them up.
  - Xilinx: two for each side of a ground pin
- Control number of SSOs through sequencing
  - Example: Do address and data busses need to switch at the same time?
- For some families [fill in], programming “unused” outputs will improve grounding or supply for output stages.

Reducing Ground Bounce

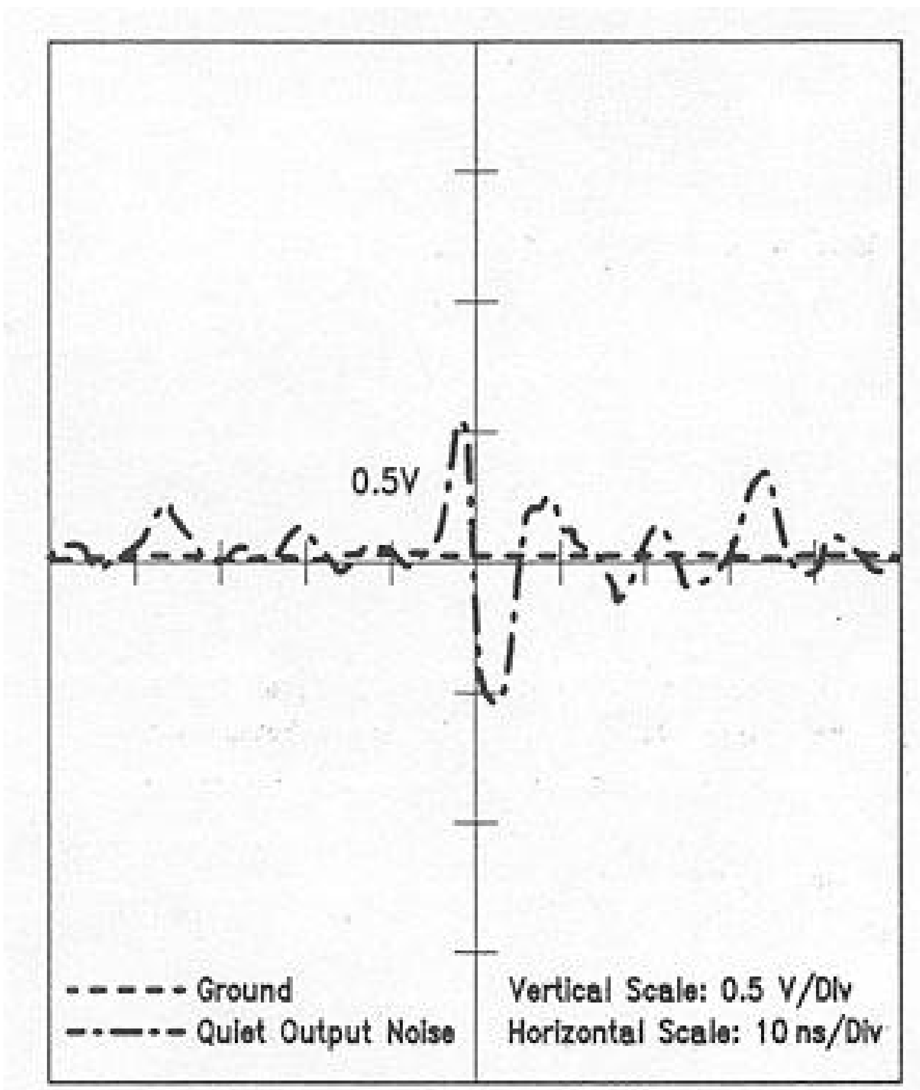
- Use buffers, particularly for large memory arrays or long lines
  - Everything does not have to be inside of the FPGA or ASIC
- Avoid sockets
- For spare pad locations, pre-wire power, ground, and bypass capacitor connections
  - “haywired” power and ground connections will have unneeded inductance.

Ground Bounce: Loading

Data from National Semiconductor



Quiet Outputs (National)
Data from National Semiconductor



- 7 Outputs Switching
- $V_{DD} = 5V$
- Worst-case Pin
- $C_L = 50$ pF

Reducing Ground Bounce (cont'd)

- For SSI/MSI, center ground pins
  - 10-15% reduction in ground bounce
  - Higher edge rates

Reducing Ground Bounce Effects

- Choose input thresholds wisely
  - OK, doesn't reduce ground bounce
    - Reduces the effects of ground bounce
  - TTL V_{IL} = 0.8V
  - Some devices offer programmable 5V CMOS or other input voltage threshold options
- Keep clocks physically away from pins that can cause ground bounce
- Keep clocks close to ground pins

Not Obvious Situations

- SSO When Using JTAG and driving board with test data over multiple parts
- Data pattern sensitivities, particularly with large data busses
  - FFFFFFFF $\rightarrow$ 00000000
- Test cabling, particularly for vibration, thermal/vacuum, and EMI tests.
- High-speed parts that are "haywired" in

Ground Bounce - Some Numbers

From Xilinx Application Note XAPP045

Table 3: Ground Bounce, 16 Outputs Switching, Each with 50 or 150 pF Load, V_{CC} = 5.5V

Load	Slew Rate	High to Low		Low to High	
		V_{OLP}	V_{OLV}	V_{OLP}	V_{OLV}
16 x 50 pF	Slow	670	480	240	240
	Fast	1170	710	480	660
16 x 150 pF	Slow	740	330	210	280
	Fast	1180	420	350	710

Device = XC4005-5
Package = PQ208

Ground Bounce - Some Numbers

Xilinx Recommendations

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC4000E devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For XC4000X devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce. Therefore, the maximum total capacitive load is 300 pF between each external Power/Ground pin pair. Maximum loading may vary for the low-voltage devices.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC4000E devices and 600 pF for XC4000X devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC4000 Series.

Ground Bounce - Some Numbers

Actel Recommendation

Device	Package	20 pf	35 pf	50 pf
A1010A/A1020A	44 PLCC	40	22	16
A1010A/1020A	68 PLCC	60	34	24
A1020A	84 PLCC	80	45	32
A1010A/1020A	84 PGA	80	45	32
A1010A/A1020A	100 PQFP	80	45	32
A1280/A1280XL	PG 176, PQ 160	160	90	64
A1240/A1240XL	PG 132, PQ 144	120	68	48
A1240/A1225/A1225XL	84 PLCC	80	45	32
A1225/A1225XL	100 PGA, PQFP	80	45	32
A1400 Family	84 PLCC	64	48	42
A1400 Family	Other packages	128	64	58

Notes:

1. Double SSO value for low slew drivers in Act 3 family.
2. Signals are simultaneously switching if transition within 10 ns
3. Signals are adjacent; can increase if drivers separated
4. Criteria: 1.5V pulse, 2 ns.

Related Issues

- Propagation Delay
- Dynamic Thresholds

Propagation Delay Affects

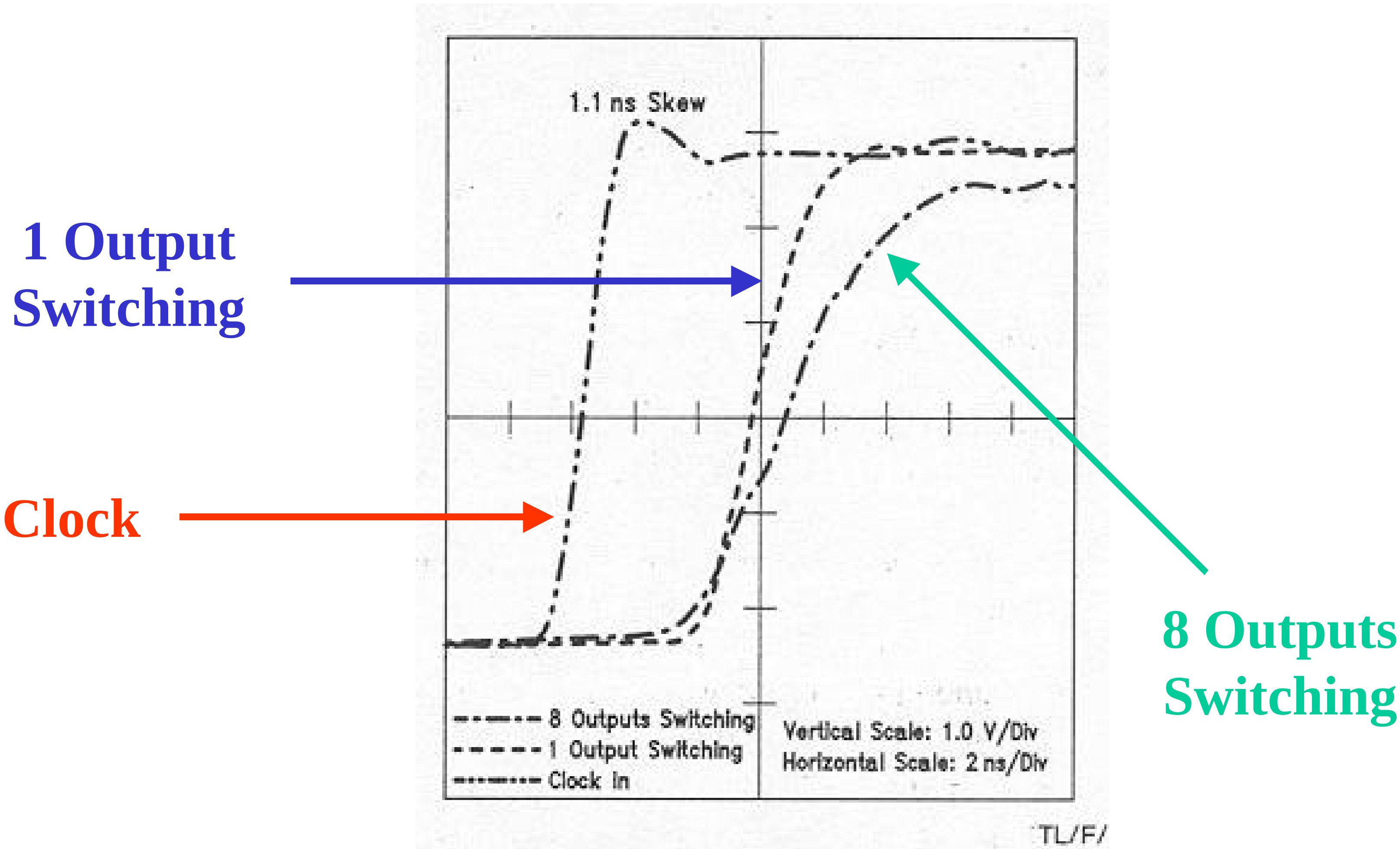
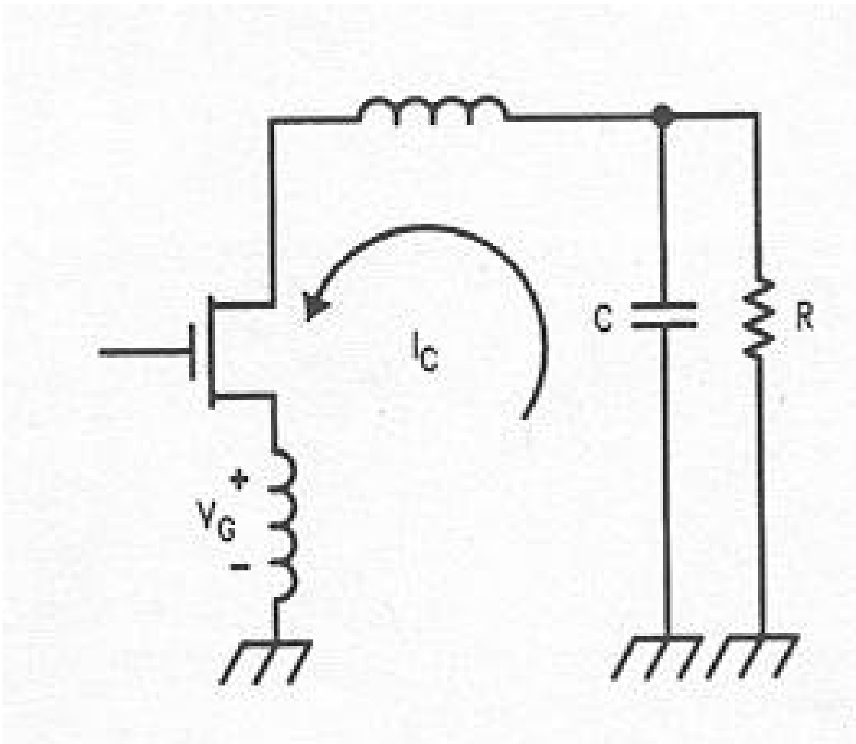
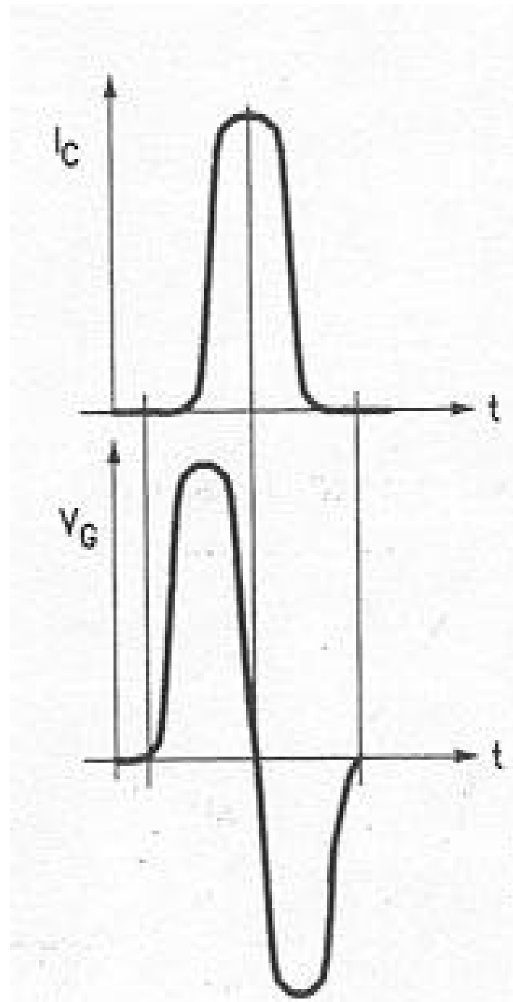


FIGURE 28. Propagation Delay vs Number of Outputs Switching

Affects on Input Thresholds
Ground Reference Shifts





Affects on Input Thresholds
Terms and Specifications (National)

V_{IHD}	The minimum HIGH input level such that normal switching/functional characteristics are observed during output transients.
V_{ILD}	The maximum LOW input level such that normal switching/functional characteristics are observed during output transients.

Affects on Input Thresholds

54ACQ244 @ V_{CC} = 4.5V, T = 25 °C

	Typ	**Worst-Case**
V_{IH}	2.25	3.15
V_{IHD}	3.1	3.5
V_{IL}	2.25	1.35
V_{ILD}	1.9	1.5

References

- **FACT™ Advanced CMOS Logic Databook**, 1990 Edition
- “Understanding and Minimizing Ground Bounce,” Application Note AN-640, National Semiconductor
- “Dynamic Threshold for Advanced CMOS Logic,” Application Note AN-680, R. Mentzer, National Semiconductor.
- “Simultaneously Switching Output Limits for Actel FPGAs,” Actel Corp., April 1996
- **High-Speed Digital Design: A Handbook of Black Magic**, Howard W. Johnson and Martin Graham, 1993
- “Ground Bounce Basics and Best Practices,” P. King, Agilent Technologies.