

# VHDL and Software Issues

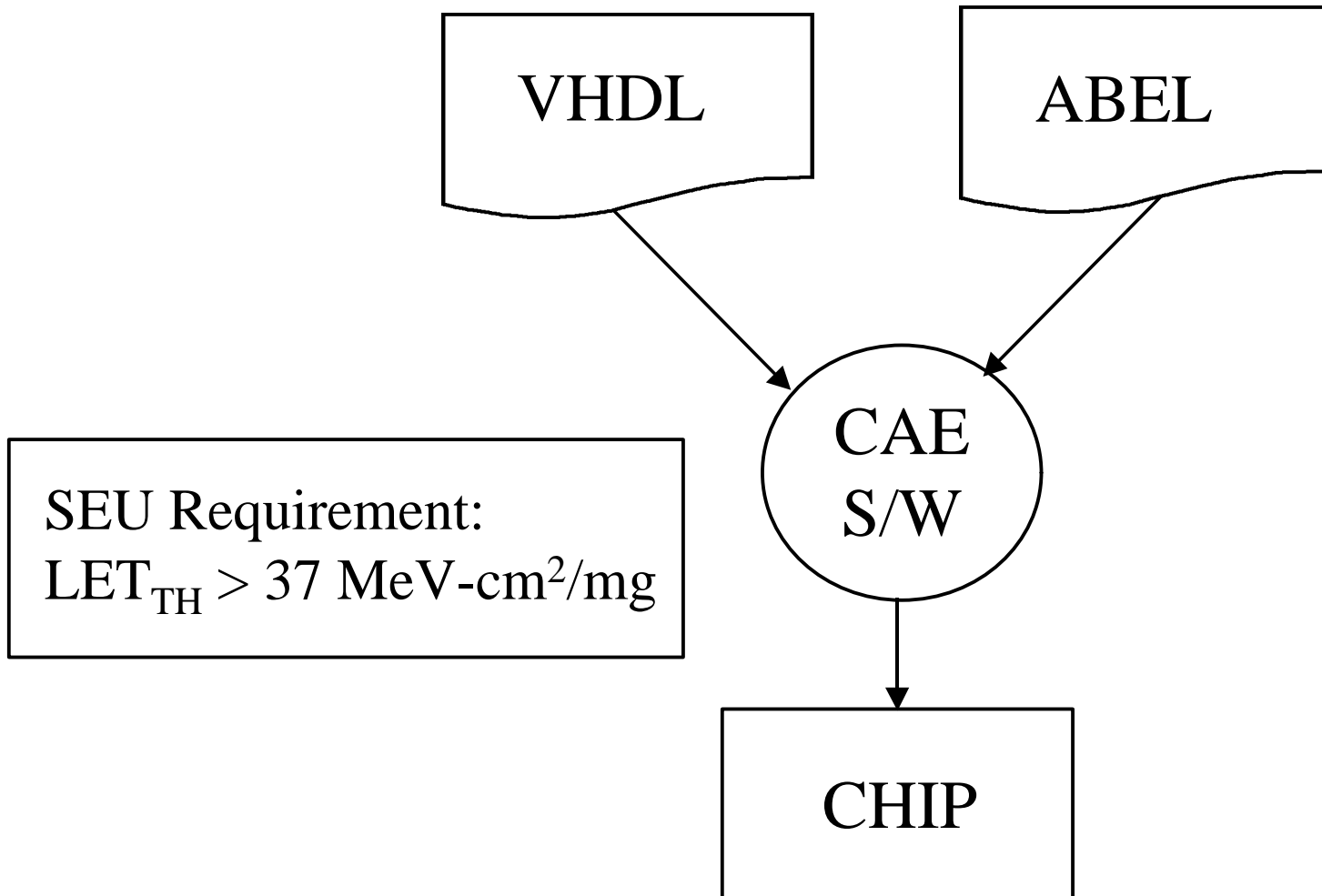
# VHDL “Interface”

```
Library IEEE;
  Use IEEE.Std_Logic_1164.All;
Entity Bool Is
  Port ( X    : In  Std_Logic;
         Y    : In  Std_Logic;
         Z    : Out Boolean    );
End Bool;

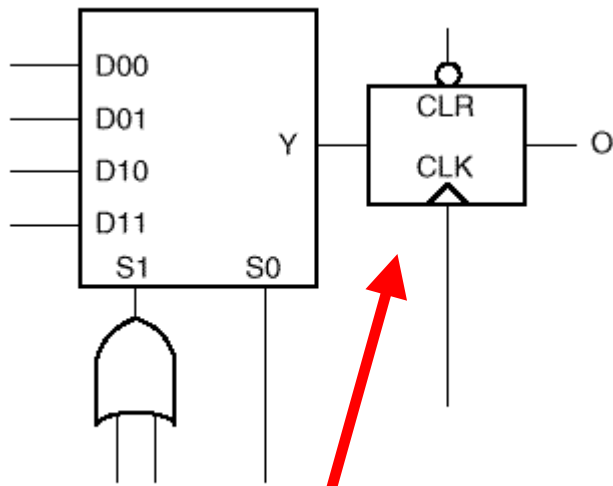
Library IEEE;
  Use IEEE.Std_Logic_1164.All;
Architecture Bool_Test of Bool Is
Begin
  P: Process ( X, Y )
  Begin
    If ( X = Y )
      Then Z <= True;
      Else Z <= False;
      End If;
    End Process P;
  End Bool_Test;
```

Boolean signal was mapped to different logical values in different versions of the same VHDL logic synthesizer

# An HDL Flow

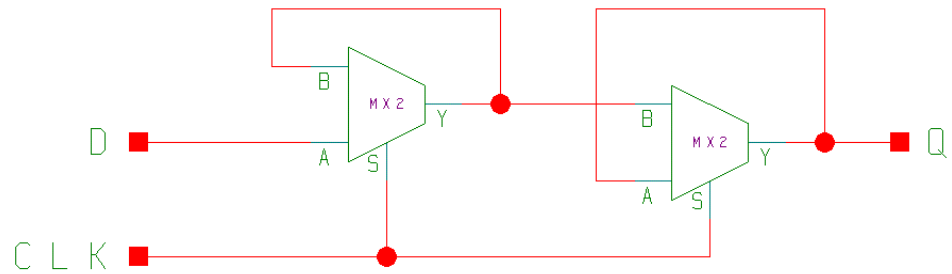


# Act 2 Flip-flop Implementation



Up to 7-input function plus D-type flip-flop with clear

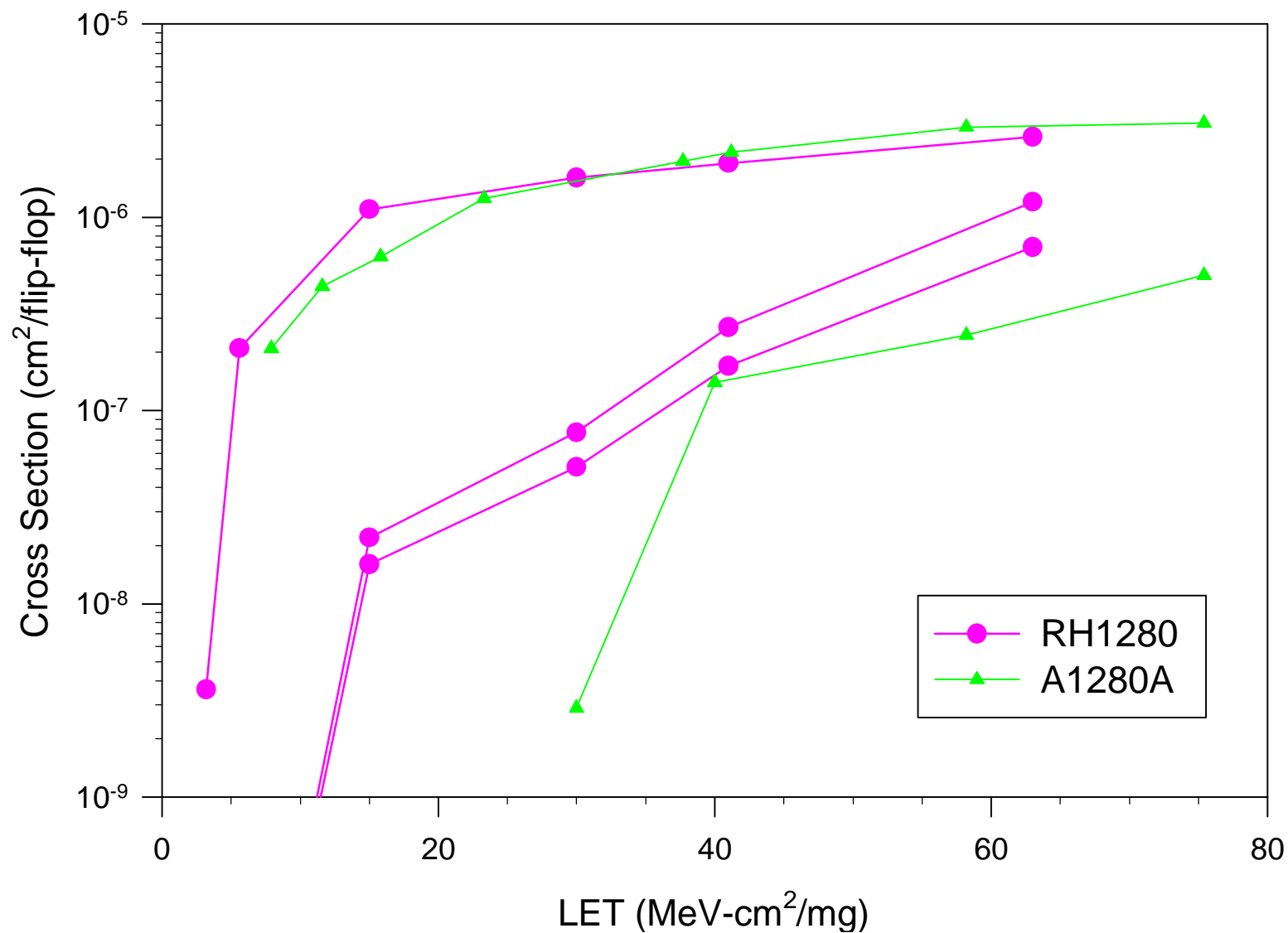
Hard-wired Flip-flop



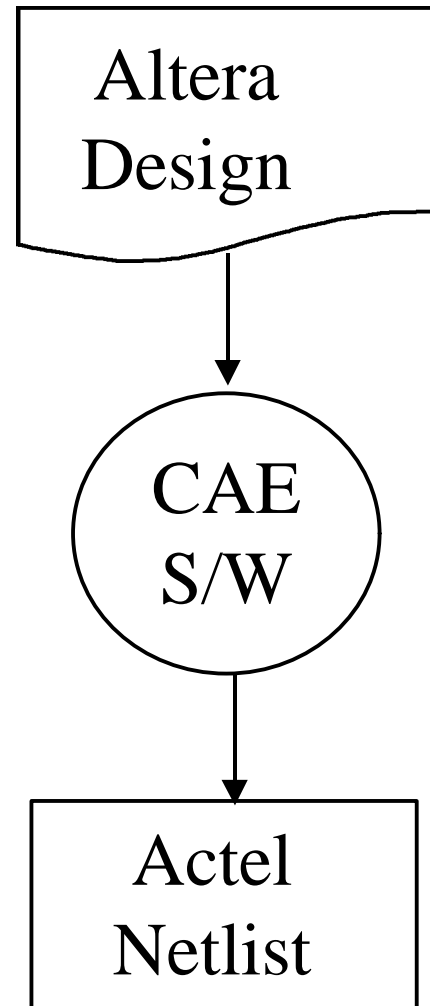
Routed Flip-flop

Feedback goes through antifuses (R) and routing segments (C)

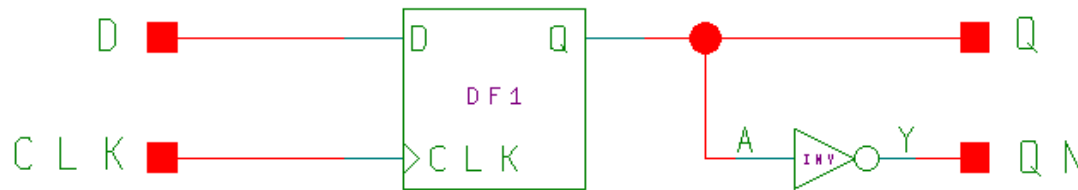
# Act 2 SEU Flip-Flop Data



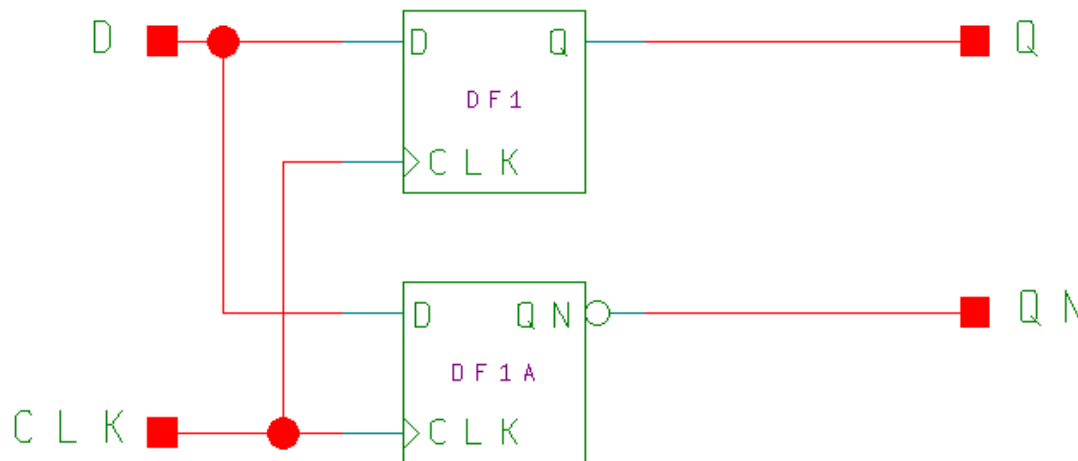
# Logic Translation/Optimization Flow



# Logic Translation/Optimization Implementation



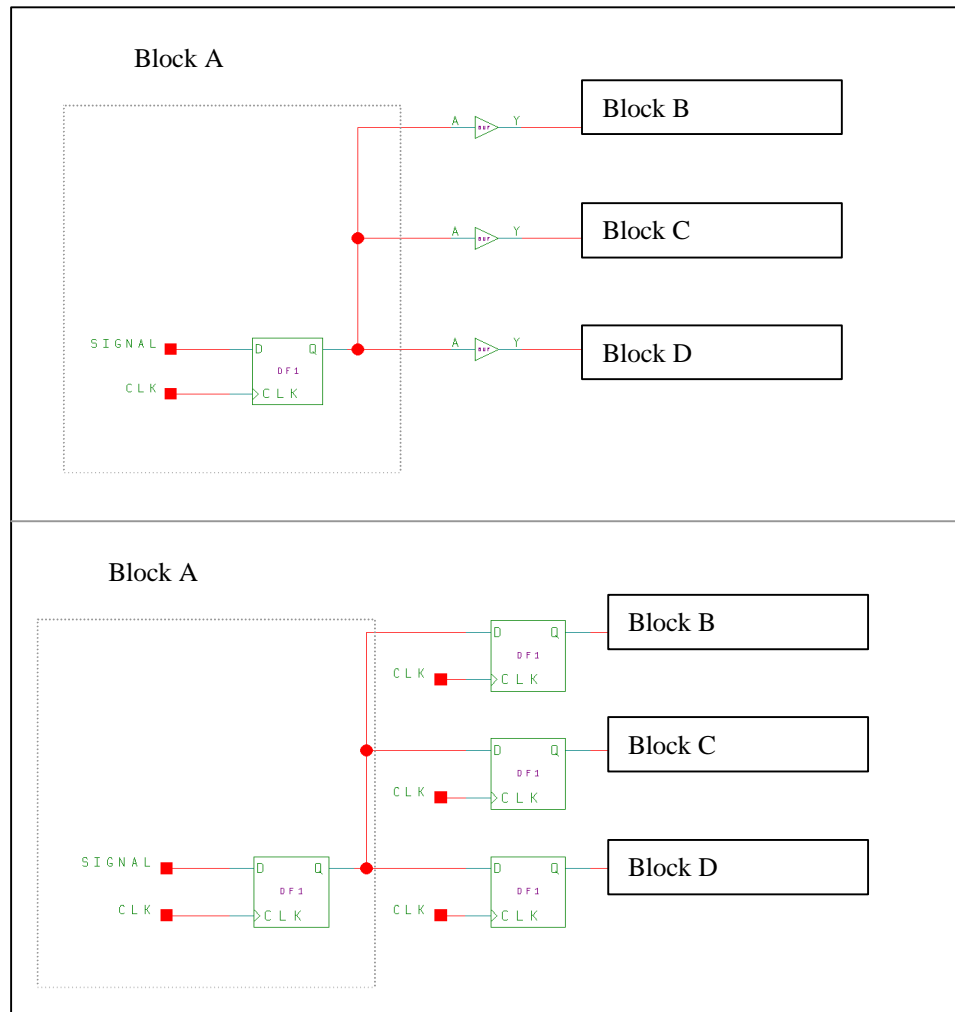
Original



“Optimized”

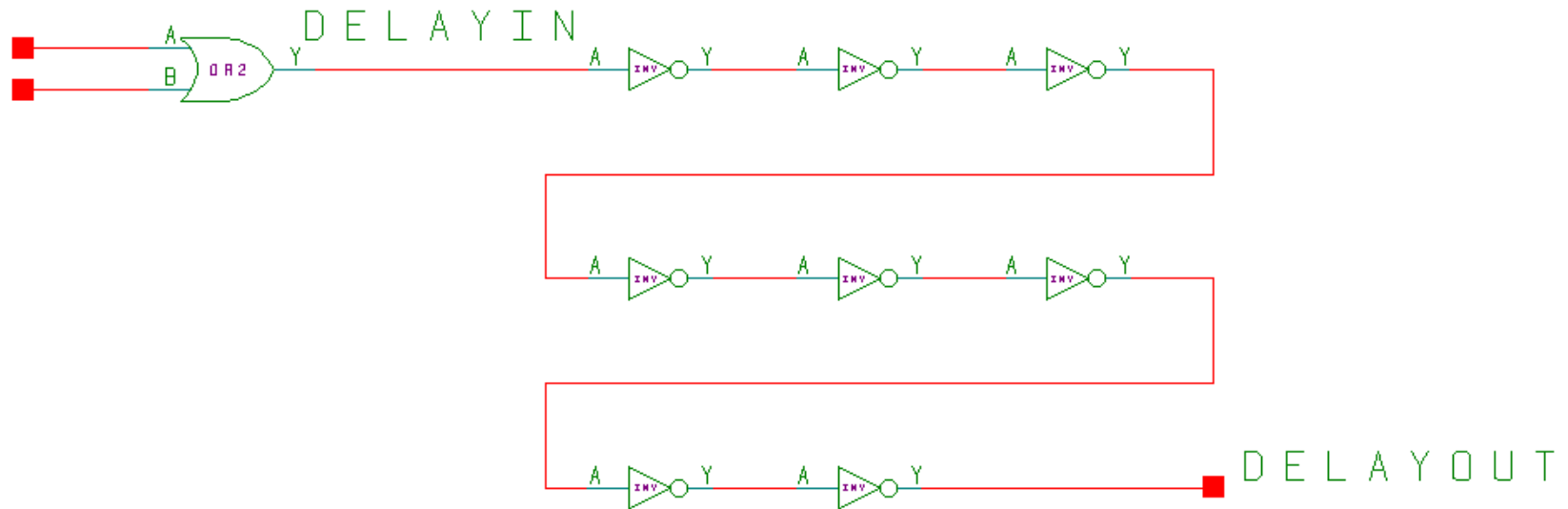
The two circuits are logically equivalent when analyzed with Boolean logic equations with the lower, CAE-optimized circuit, permitting higher device speeds. An SEU analysis shows the addition of a second state variable with an upset resulting in the "optimized" circuit containing a state where  $Q = QN$ , violating the system equations and causing a failure.

# Logic Replication



**Two methods of signal distribution. The top version shows a signal distributed to multiple blocks with buffers driving multiple loads. The bottom version replicates flip-flops, resulting in higher system speeds. Routing delays are significant. Recovery from SEUs with multiple flip-flops are not considered by current computer-aided engineering tools.**

# Delay Generation



# VHDL Code and Synthesizer Analysis

## Case Study - Hardened Clock Generator

- The VHDL synthesizer, unknown to the designer, generated a poor circuit for a TMR voter
  - Used 3 C-Cells for a voter
  - Slowed the circuit down
- The implementation of the voter is hidden from the user
  - Synthesizer generated a static hazard
  - An SEU can result in a glitch on the "hardened" clock signal.

# VHDL Code and Synthesizer Analysis

## Case Study - Hardened Clock Generator

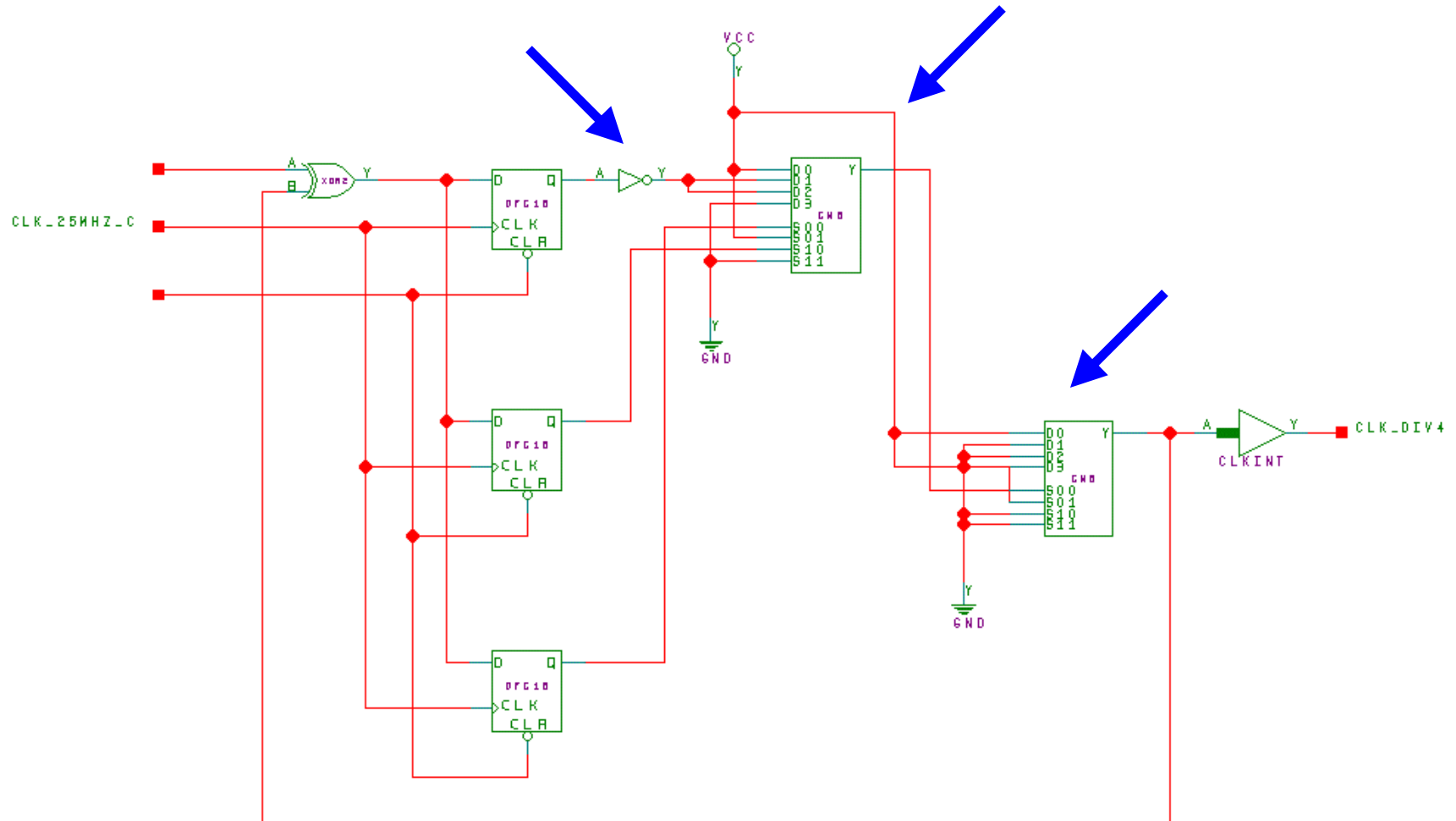
```
-- Divide 25 MHz (40 ns) clock by 4
-- to produce 6.25 MHz clock (160 ns)
-- This clock should be placed on
-- an internal global buffer

clkint1: clkint
Port Map ( A => clk_div_cnt(1),
           Y => clk_div4           );

clkdiv: Process (reset_n, clk)
Begin
    If reset_n = '0' Then
        clk_div_cnt <= "00";
    Elsif clk = '1' And clk'EVENT Then
        clk_div_cnt <= clk_div_cnt + 1;
    End If;
End Process clkdiv;
```

# VHDL Code and Synthesizer Analysis

## Case Study - Hardened Clock Generator



Most significant bit of the counter. 3 C-Cells are used for the voter.