

Power Switching

Power Supply Sequencing

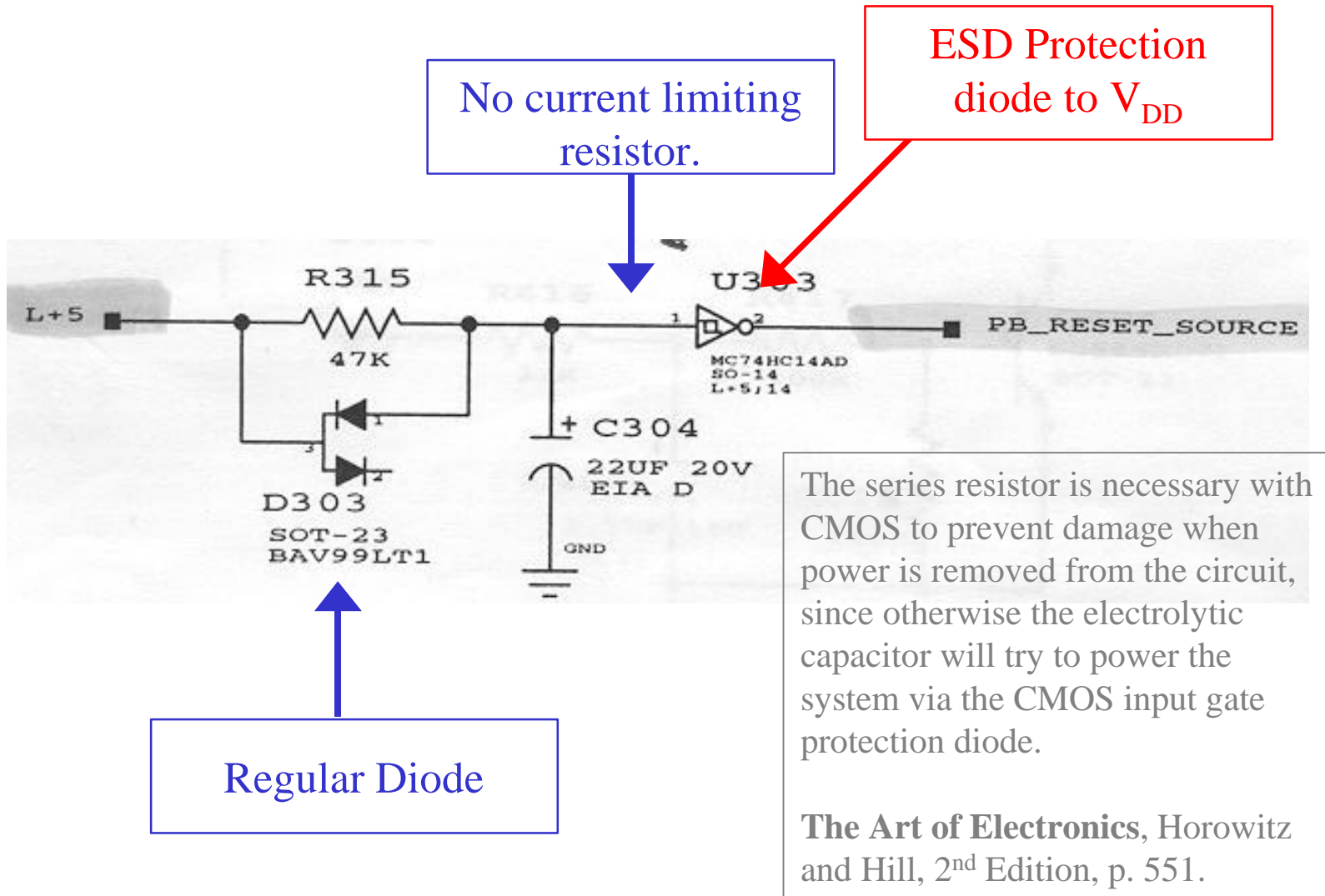
- Protecting I/O's
- Powering Circuits
- RT54SX16/32
 - Perhaps RT54SX32S
 - UTMC buffers
- EEPROMs/write protection
- SMEX/WIRE

Power Supply Sequencing

Issues: Protecting I/O's

- Parasitic/ESD diodes
- PCI clamp diodes
- Cold-sparing capable I/O's

Power-On Reset (POR)



Power Supply Sequencing

RT54SX16/32

Power-Up Sequencing

RT54SX16, A54SX16, RT54SX32, A54SX32

V_{CCA}	V_{CCR}	V_{CCI}	Power-Up Sequence	Comments
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	<u>Possible damage to device.</u>

Power-Down Sequencing

RT54SX16, A54SX16, RT54SX32, A54SX32

V_{CCA}	V_{CCR}	V_{CCI}	Power-Down Sequence	Comments
3.3V	5.0V	3.3V	5.0V First 3.3V Second	<u>Possible damage to device.</u>
			3.3V First 5.0V Second	No possible damage to device.

Power Supply Sequencing

RT54SX32S

- To date, our lab work has shown, on some parts, that when V_{CCI} is applied before V_{CCA} , significant currents, > 10 mA, can be seen flowing into the V_{CCI} pin.
- Power supply sequencing may also affect reliability of the safe power on/off feature.
- These are under investigation.

Power Supply Sequencing

EEPROMs: Hardware Write Protection

3.11.5 Power supply sequence of EEPROMs. In order to reduce the probability of inadvertant writes, the following power supply sequences shall be observed.

a. For device types 1-18, a logic high state shall be applied to WE and/or CE at the same time or before the application of V_{CC} . For device types 16-18, an additional precaution is available, a logic low state shall be applied to RES at the same time or before the application of V_{CC} .

b. For device types 1-18, a logic high state shall be applied to WE and/or CE at the same time or before the removal of V_{CC} . For device types 16-18, an additional precaution is available, a logic low state shall be applied to RES at the same time or before the removal of V_{CC} .

Power Supply Sequencing

EEPROMs: Software Write Protection

To protect against unintentional programming caused by noise generated by external circuits, AS58C1001 has a **Software data protection function**. To initiate Software data protection mode, 3 bytes of data must be input, followed by a dummy write cycle of any address and any data byte. This exact sequence switches the device into protection mode. This 4th cycle during write is required to initiate the SDP and physically writes the address and data. While in SDP the entire array is protected in which writes can only occur if the exact SDP sequence is re-executed or the unprotect sequence is executed.

The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the AS58C1001 to the Non-Protection mode, for normal operation.

Power Supply Sequencing

EEPROMs: Software Write Protection

Enable Protection

Address	Data
5555	AA
2AAA	55
5555	A0

Disable Protection

Address	Data
5555	AA
2AAA	55
5555	80
5555	AA
2AAA	55
5555	20

Power Supply Sequencing SMEX/WIRE

- System applied power simultaneously to the FPGA, drive circuitry, and relay.
- Control FPGA generated both ARM and FIRE signals based on spacecraft opto-isolated inputs.
- Transient analysis not performed.
- Saved 1 relay.

Power Supply Sequencing SMEX/WIRE

