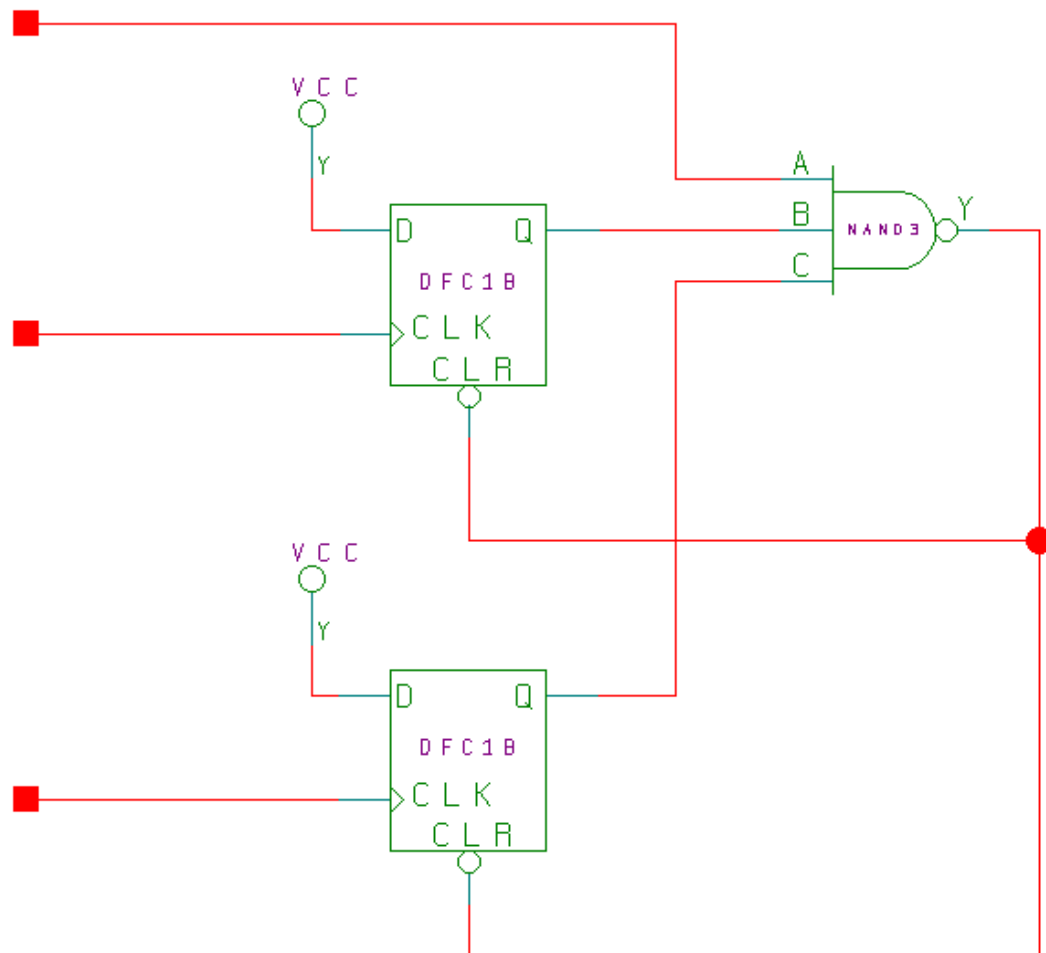


# Asynchronous Logic

Some material from “Asynchronous FPGA Risks,” Ken Erickson, 2000 MALPD International Conference  
September 26-28, 2000.

# Asynchronous Clears

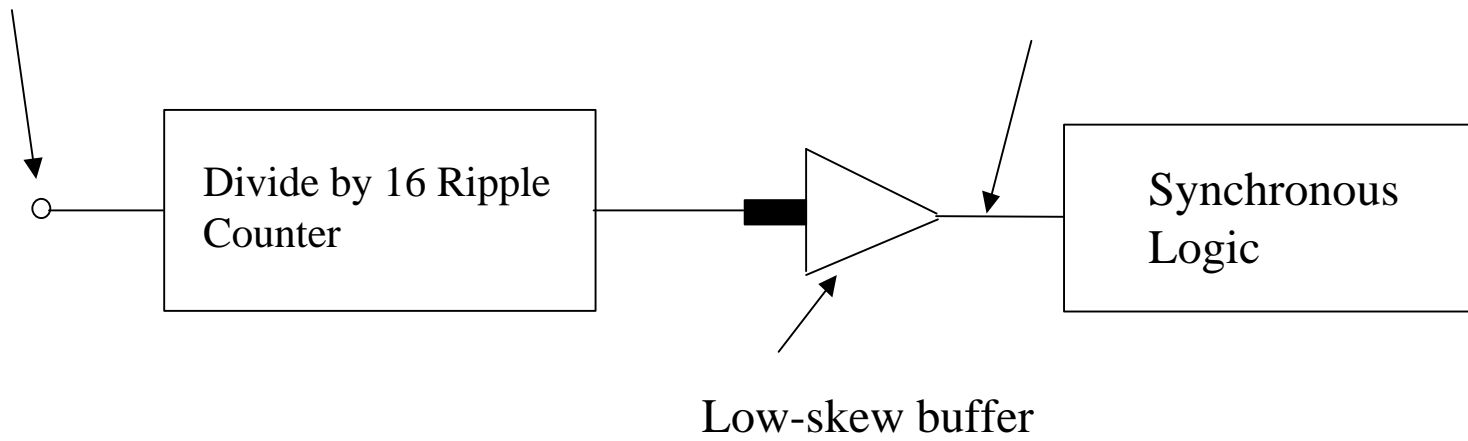


# Synchronous vs. Asynchronous Logic

- Asynchronous signals are not synchronized to a clock.
- Timing Analysis for Asynchronous Circuits
  - Many tools do not support this
  - Complex, sometimes not tractable
  - Error-prone
- Asynchronous logic may result in smaller, faster, or lower power circuits
- Asynchronous logic, well done, is reliable.

# Is It Or Isn't It?

16 MHz high skew clock

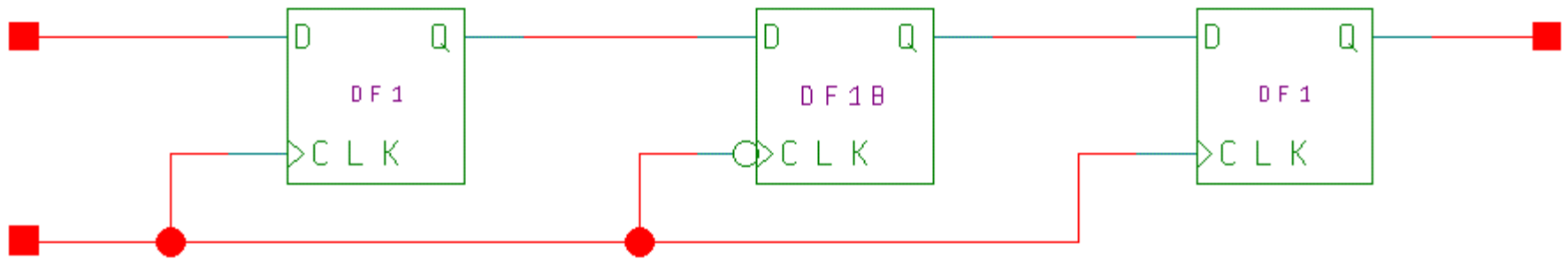


1 MHz low-skew clock

Synchronous  
Logic

Low-skew buffer

# Is It Or Isn't It?



# Common Asynchronous Design Problems

- Design may be marginal
  - Adequate margin non-verifiable
- Aging and radiation effects
  - Can not test for these
- Failures may occur late in the test program
  - i.e., thermal or thermal/vacuum testing
  - **This is always on Friday night**
- System may have unexplained glitches
  - Often difficult to troubleshoot

# Some Examples of Problems

- Spacecraft Experienced Inadvertent Reset During System Testing
  - Only from 17 to 20 °C
  - FPGAs were redesigned
- Lots and lots of ‘rookie mistakes.’
  - No analysis and unknown margin
  - Decoded outputs used as clocks
  - High-skew signals used as clocks
    - Counters
    - Shift Registers

# Case Study

## Potential Race Condition

