

Special Pins

A Very Basic Topic But A Source of
Frequent Failures and Problems

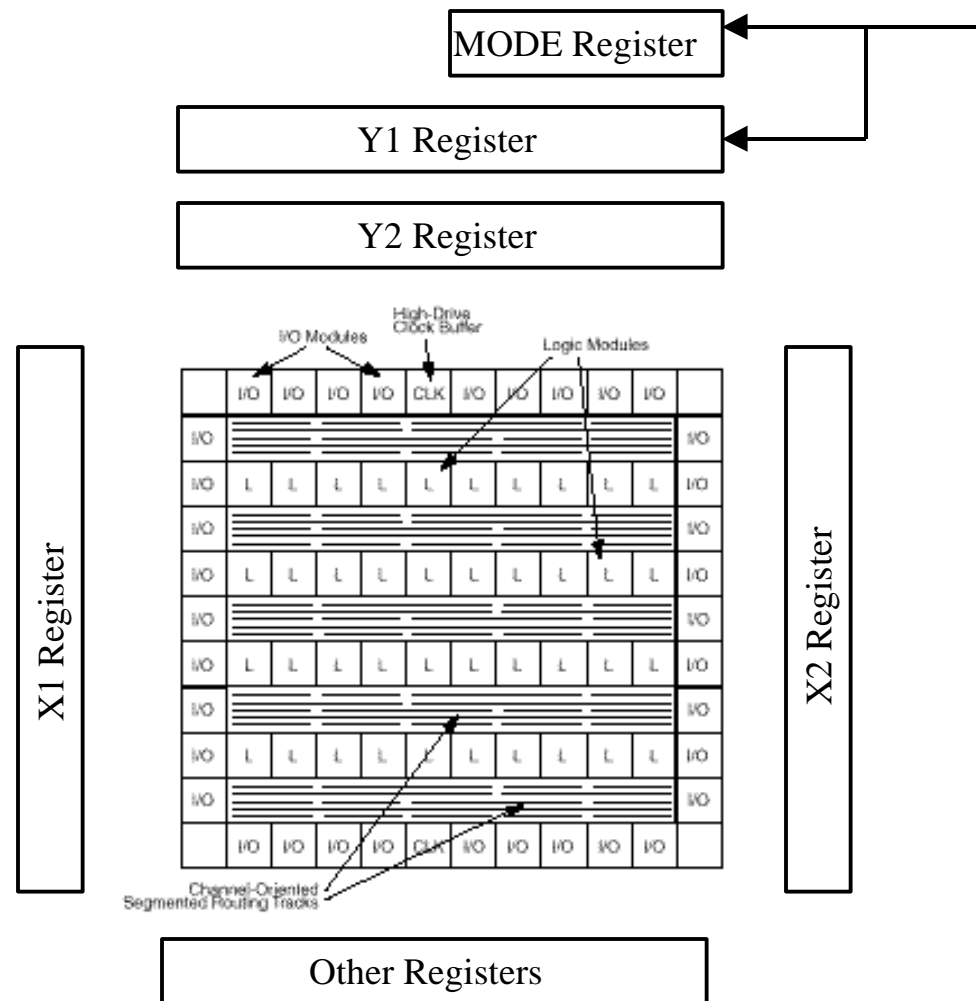
Termination of Special Pins

- MODE pin (test program mode).
- V_{PP} pin (programming voltage).
- TRST* (Reset to JTAG TAP controller)
- TCLK (provides clock to TAP controller)
- SDI, DCLK (varies for each device type)
- Others

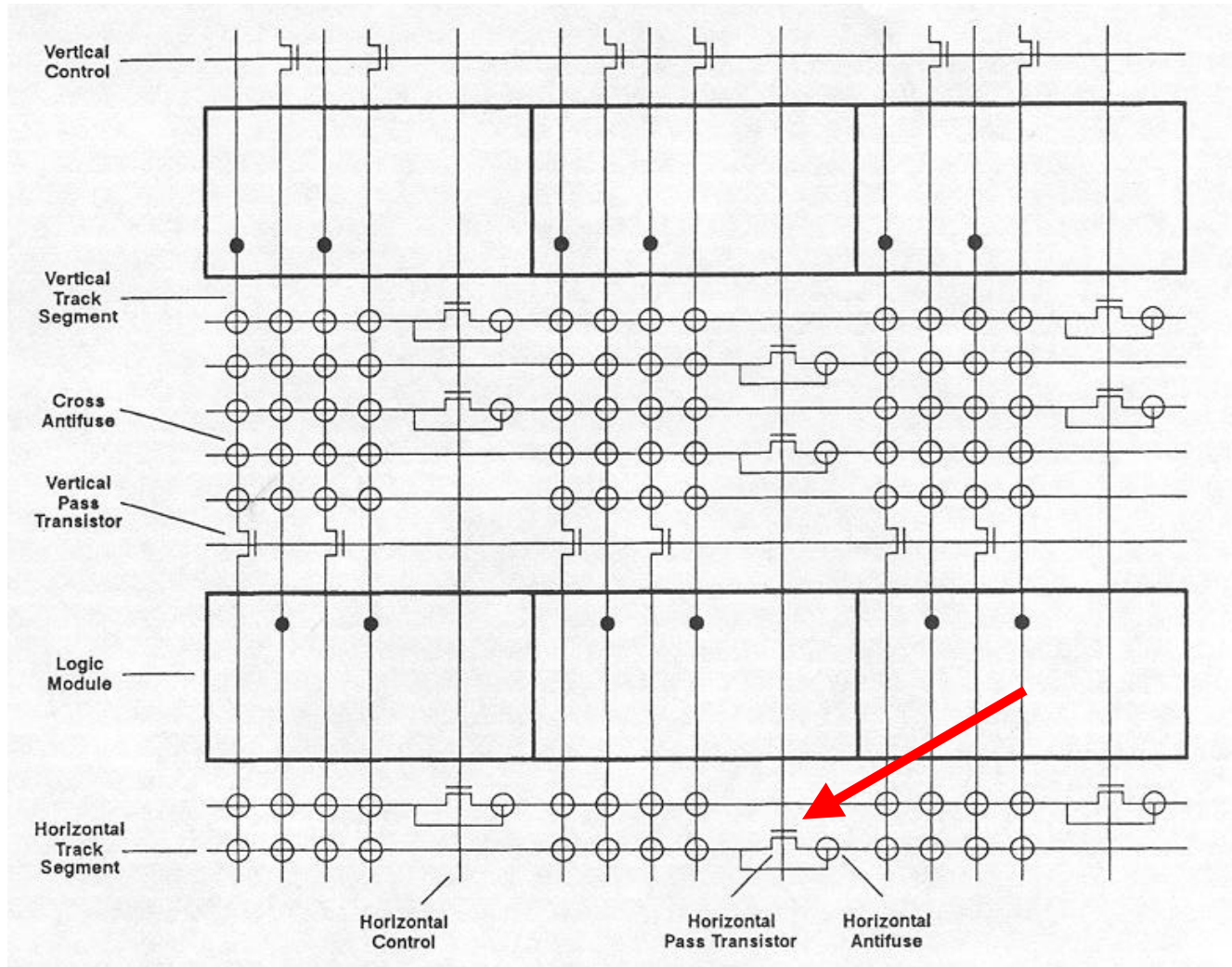
MODE Pin

- Left Floating
 - Device can be non-functional
 - High currents
 - Uncontrolled I/O
- Tied High During Test
 - Working device stopped functioning
 - Power supply rise time key

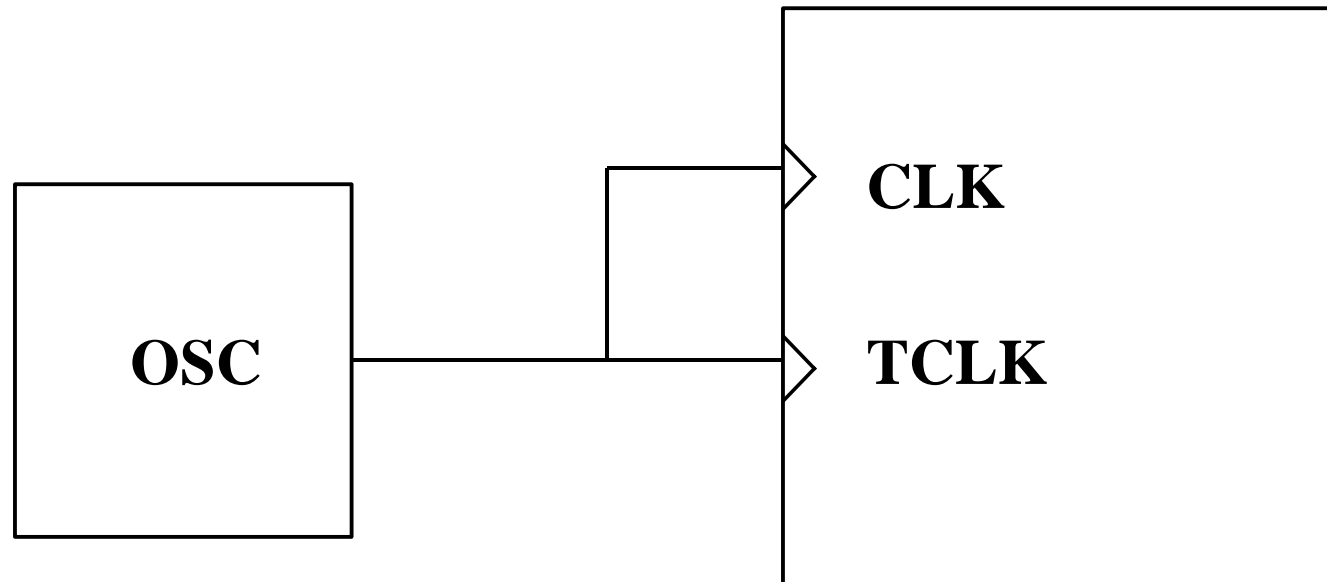
MODE Pin - Test, Debug and Programming Control



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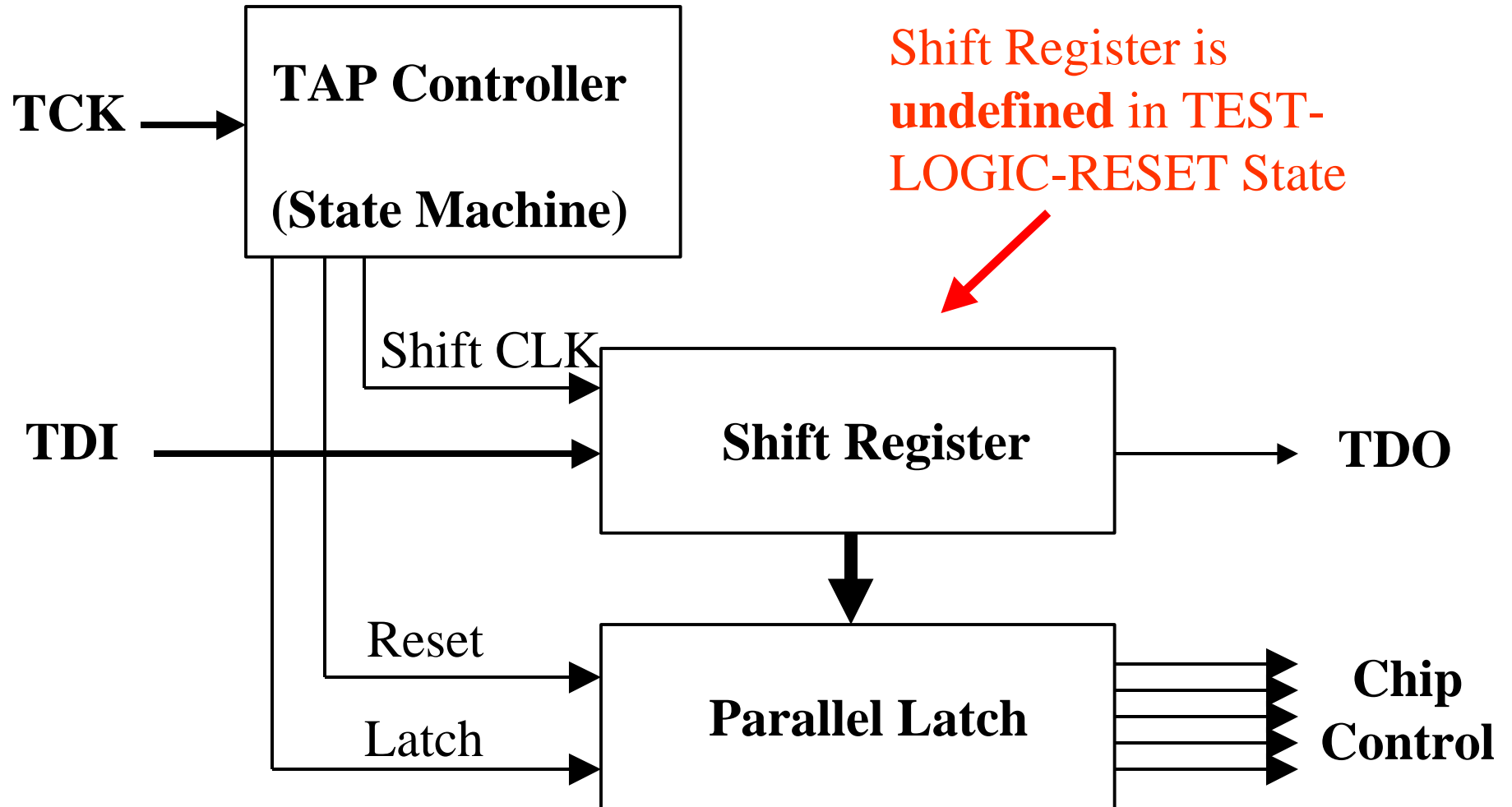


IEEE JTAG 1149.1 TCLK

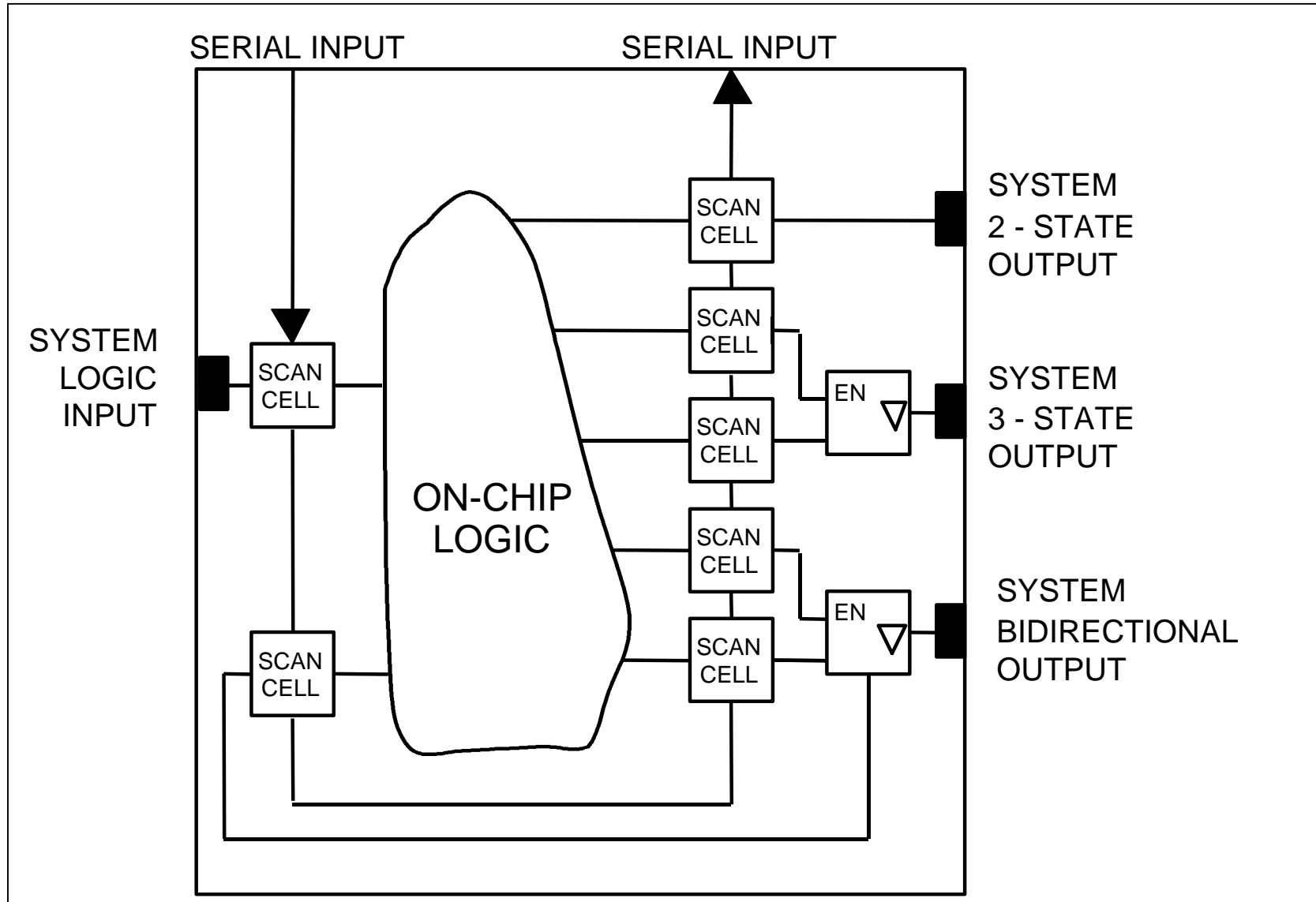


The CLK pin may turn into an output driving low, clamping the oscillator's output at a logic '0'. The TAP controller can not reset and restore I/O operation. Most FPGAs do not have the optional TRST* pin. Note TRST*, when present, has a pull-up.

IEEE JTAG 1149.1 TCLK



IEEE JTAG 1149.1 - Scan Path



IEEE JTAG 1149.1 - Scan I/O Cell

