



Logic Design: Clocking, Timing Analysis, Finite State Machines, and Verification

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Richard B. Katz
National Aeronautics and Space Administration
rkatz@klabs.org

Rod Barto
Spacecraft Digital Electronics
rbarto@klabs.org

Seminar Abstract

The fundamental theme of this seminar will be the design and verification finite state machines for high-reliability applications. The starting point for any synchronous sequential circuit design and analysis is the clock. Clock structures and characteristics, both at the device and application level, will be discussed and their impact on circuit topologies and timing analysis. Starting with the straightforward single-phase, single-edge, low-skew global clocks, different clock structures will be explored for different design goals such as low-power and high-speed. Finite state machines will be covered in detail from two perspectives: the topologies logic as well as applications. Examples of topologies to be covered will include Gray, one-hot, sequential, LFSR, and others. Applications to be covered include synchronizers, arbiters, controllers, and others. Analysis will be performed to determine the robustness of each solution. The results of the analysis will lead to a discussion of error detection and correction and the trade-offs; e.g., some circuits have a higher probability of error but permit 100% detection of all single bit errors. A discussion of error detection and correction methods will show various techniques as well as trade-offs. For example, should the monitoring circuits be located at the lowest possible level or the system level? This will be shown to be a function of the state machine's structure and circuit application.

Seminar Organization

- Clocking
- Finite State Machines, Low Level
- Finite State Machine, Systems Level

Analysis techniques will be a running theme throughout the seminar.

Modules in this Seminar

- Introduction
- Clocking
 - Clock Distribution Topologies
 - Clock Skew
 - DLLs and PLLs
 - Clock Structures: Real Devices
 - Microprocessor Clocks
 - Clock Timing and Skew: Real Devices
 - Clock Upset
 - Miscellaneous Clock Topics

Modules in this Seminar

- Finite State Machines, Low Level
 - Basic Finite State Machines
 - FSM Implementation (1)
 - Event Counters
 - Gray Codes
 - Linear Feedback Shift Registers
 - SEU Hard Counters
 - Resetting Finite State Machines
 - Memory Controllers
 - FSM Implementation (2)

Modules in this Seminar

- Finite State Machine, Systems Level
 - System Timing Analysis
 - System Level Error Handling
 - System Protection: Watch Dog Timer
 - Metastable States
 - Hardware as Software
 - Pipelining

Administrative

- This is a seminar and not a training course.
- Companion www site:
 - <http://klabs.org>
 - Papers, application notes, reports, test data, bug reports, tips, etc.
 - No dedicated search engine
 - set up for searching with Yahoo! and Google.
- MAPLD International Conference
 - <http://klabs.org/mapld>