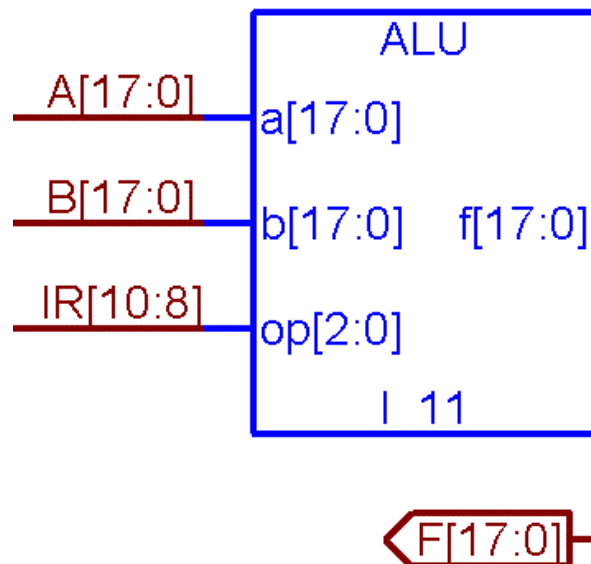


Intellectual Property

IP Cores Trends

- 70's - 1st IP core library: TI TTL databook
- 80's - PLD application notes
- 90's - IP vendors
 - HDL soft cores
 - Schematic crafted firm cores
 - Embedded hard cores (PCI)
- 00's - System on Chip

Arithmetic Logic Unit - Verilog



```
Alu.v - Notepad
File Edit Search Help
always @(op or a or b)
begin
    case (op)
        `plus:      f = a + b;
        `minus:     f = a - b;
        `band:      f = a & b;
        `bor:       f = a | b;
        `unegate:   f = ~a;
        default:    f = 8'hx;
    endcase
end
```

Automatic Component Generation

The image shows the Kompile software interface with several callouts pointing to specific features:

- User Data Input:** Points to the Target field containing `C:\designs\test\Corr_lut.vhd`.
- VHDL Coded for Selected Synthesizer:** Points to the Flavor dropdown menu set to `Synplify`.
- Parameters Selection:** Points to the Size section, where `Address (bits)` is set to `8` and `Data (bits)` is set to `16`.
- Coding Style Selection:** Points to the VHDL Style dropdown menu, which is open and shows options: `Logic 1` (selected), `Logic 0`, `bit CASE`, `word CASE`, and `HArray :-)`.

The right-hand window, titled `Corr_lut.kfr`, displays the generated code as a list of binary strings:

```
Line: 1  
00110001\b 00000100\b  
00110111\b 00000100\b  
00111011\b 00000100\b  
00100011\b 00000100\b  
00010011\b 00000100\b  
01110011\b 00000100\b  
10110011\b 00000100\b  
00110011\b 00000100\b  
01100111\b 00001000\b  
01100100\b 00001000\b  
01100010\b 00001000\b  
01101110\b 00001000\b  
01110110\b 00001000\b  
01000110\b 00001000\b  
00100110\b 00001000\b  
11100110\b 00001000\b  
01100110\b 00001000\b  
11001101\b 00010000\b  
11001110\b 00010000\b  
11001000\b 00010000\b  
11000100\b 00010000\b  
11011100\b 00010000\b
```