



QuickLogic Reliability Report

Q4 1998

INTRODUCTION

This report summarizes QuickLogic Product Reliability. QuickLogic has established aggressive reliability objectives to assure that all products exhibit reliability, which exceeds customer reliability requirements for purchased components. In addition, the quality standard at QuickLogic results in a culture requiring continuous improvement in quality and reliability. This report includes data from the pASIC 1, pASIC 2 and pASIC 3 product families.

Product reliability is assured by a total quality management system. The quality management system is described in detail in the QuickLogic Quality Manual. Key reliability-related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) manufacturing identification of "Maverick Lot" yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing process; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarks.

Product Reliability data is accumulated as a result of new product Qualification Plan activities as well as from the Reliability Monitor Program. All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Reliability strategy requires that every failure which occurs during reliability testing be subjected to failure analysis to determine the failure mechanism. Corrective action is then implemented to prevent future failures. The result is continuous improvement in product reliability. Copies of any specific QuickLogic documents are available through your QuickLogic sales representative.

Reliability Monitors of individual products and packages are generally developed by identifying a process driver device (in most cases the same device used to qualify a process / product / package family). Once the process driver device is identified, the appropriate stress test programs are put in place to adequately monitor the ongoing process average of the specific family. This process average measurement is made by understanding the reliability and quality results of individual samples from production material. The latest production material is assembled and samples are pulled at the outgoing QA portion of the production flow, then randomly placed into specified reliability tests. These tests include early failure rate studies and dynamic long-term life test.

Monitor testing is completed on an ongoing quarterly cycle. Test results are subsequently made available in quarterly cycles. The monitor report details all test results received for the previous quarter. With all of this data, an effective ongoing monitoring method is established which is capable of identifying reliability trends associated with all process/ product/ package families.

TECHNOLOGY

QuickLogic uses a high volume CMOS process technology with single poly and multi-layers of metal. The base CMOS technologies were developed for high speed Logic, SRAM and Flash EPROM. The addition of the low on-resistance and low off-capacitance ViaLink antifuse to these technologies creates a very high speed programmable logic process.

The ViaLink element is located in a via between the two layers of metal. It is created by depositing a very high resistance amorphous silicon film on a standard size tungsten plug via. The silicon is deposited at low temperature and causes no change to the properties of the CMOS transistors and the underlying metal layers. When deposited at low temperatures silicon forms an amorphous structure which can be electrically switched from a high resistance state ($\approx 5 \text{ G-}\Omega$) to a low resistance state ($\approx 30 \Omega$) for an off-to-on ratio of 10^8 . QuickLogic takes advantage of this property to create the ViaLink metal-to-metal antifuse programming element. See Figure 1

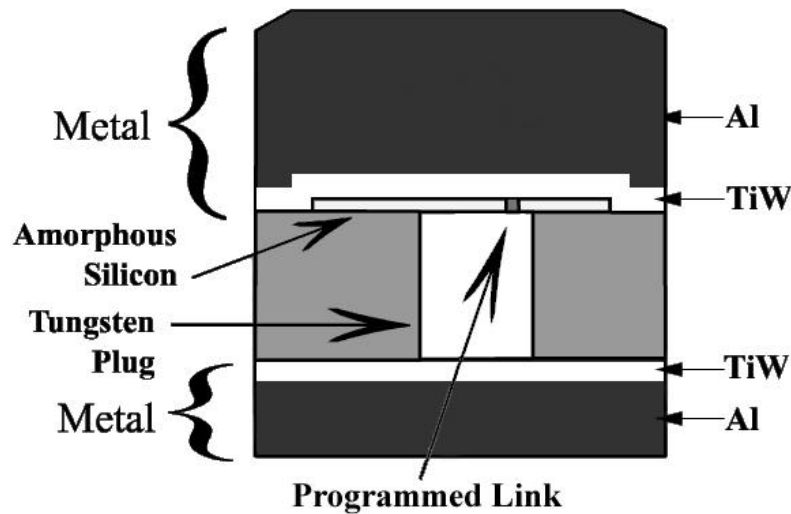


Figure 1. Drawing of ViaLink Cross Section

The programming voltage of the ViaLink element varies with amorphous silicon thickness. For a desired programming voltage between 10-12 volts, the thickness of the amorphous silicon film is approximately 1000 \AA . This thickness is ideal for process control and minimizes the capacitive coupling effect of an unprogrammed element located between the two layers of metal.

Amorphous silicon is deposited with standard semiconductor manufacturing equipment and processing techniques. In addition to antifuse elements, amorphous silicon is used in the high-volume fabrication of image sensors, decode and drive circuits for flat panel displays, and high efficiency solar cells.

FAILURE MECHANISMS IN THE pASIC DEVICE

A variety of failure mechanisms exist in CMOS integrated circuits. Since the overall failure rate is composed of various failure mechanisms, each having different temperature dependence and thus varying time-temperature relationships, it is important to understand the characteristics of each contributing failure mechanism. Table 1 lists several key failure mechanisms that have been characterized for standard CMOS devices, plus the two mechanisms for the programmed and unprogrammed ViaLink elements.

Table 1. Failure Mechanisms in Semiconductor Devices

Failure Mechanism	t_{50} dependence	Activation Energy (E_a)	Detection Tests
Short channel charge trapping (V_T and g_m shifts)	$g_m \approx \exp(-AE)$	Approx. -0.06 eV	Low temp. high voltage oper. life test
Insulator breakdown (leakage, opens)	$\exp(-\beta/E)$ value of β depends on the dielectric and may be temp. dependent.	Approx. 0.3 eV for SiO_2 and dependent on E	High voltage operating life test (HTOL)
Open metal from electrolytic corrosion	$(\%RH)^{-4.5} \exp(E_a/kT)$	0.3 to 0.6	High temp./high humidity/bias test
Masking and assembly defects	$\exp(E_a/kT)$ (Arrhenius)	0.5 eV	High temp and HTOL
Silicon defects (leakage, etc.)	Arrhenius	0.5 eV	High voltage and guard banded tests
Metal line opens from electromigration	$\frac{WT}{J^2} \exp(E_a/kT)$	Approx. 0.7 eV for Al+Cu alloys	HTOL
Stress induced open metal (operative only on non-clad metal systems)	$W^m T^p \exp(E_a/kT)$ (m and p range from 1.3 to 4.7)	0.6 to 1.4 eV (E_a difficult to reproduce)	Temp. cycling
Wire bond failure from excessive gold-aluminum interdiffusion	$1/(Dt)^{1/2}$ where $D = D_0 \exp(E_a/kT)$	0.7 eV	HTOL
Parameter shifts due to contamination (such as Na)	Arrhenius	1.0 eV	High temp. bias
Plastic Chemistry of the package	Arrhenius	1.0 eV	High temp./high humidity/bias test
Polarization in the thin film layers	Arrhenius	1.0 eV	High temp./high humidity/bias test
Microcrack in oxides and thin films	Arrhenius	1.3 eV	HTOL/ Temp Cycling
Unprogrammed ViaLink antifuse	$\exp(-BE)$	0 eV	High V_{CC} static life test
Programmed ViaLink antifuse	$\exp(-PJ)$	0 eV	Low Temperature Operating Life test

In Table 1, t_{50} is the mean time to failure, E is the electric field; E_a is the activation energy; k is the Boltzmann constant ($8.62 \times 10^{-5} \text{ eV}/^\circ\text{K}$); W is the width; t is the thickness; J is current density; g_m is transconductance; V_T is the threshold voltage; A , m and p are constants; T is the absolute temperature; RH is the relative humidity; and D is the diffusion constant.

Various accelerated life tests are used to detect the possible contribution of each mechanism to the overall failure rate of the device. Failure rate data taken at elevated temperature can be translated to a lower temperature through the Arrhenius equation. This equation, in the form of an acceleration factor, AF , can be written as,

$$AF = \exp[-E_a/k(1/T_s - 1/T_o)] \quad (1)$$

where T_s is the stress temperature, T_o is the operating temperature of the device, E_a is the activation energy for that mechanism, and k is the Boltzmann constant.

ACCELERATED LIFE TESTS ON THE pASIC

The purpose of a life test is to predict the reliability and failure rate of a device. However, a device operating under normal operating conditions would require years of testing to determine its long-term reliability. Methods of accelerating failures developed in the industry allow accurate prediction of a device life time and failure rate in a much shorter time duration. Accelerated stress tests are run at high temperature, high voltages, or a combination of both. Table 2 contains the results of the tests performed on programmed pASIC devices, where approximately 4% of ViaLink elements were programmed and the remaining ViaLink elements were left unprogrammed. These percentages are typical for a programmed, fully utilized pASIC device.

Table 2. Accelerated Life Tests on the pASIC Devices

Test	Process Qual. Acceptance Requirements
High Temperature Operating Life, 1000 hrs, 125°C, or 500 hrs 150°C, $V_{cc} = V_{ccmax}$, MIL-STD-883C, Method 1005, Dynamic, 1MHz	<100 FITs @ 55°C, $E_a = 0.7eV$, 60% confidence
Temperature Humidity Bias, 1000 hrs., alternately biased, 85% R.H., 85°C, JEDEC STD 22-B Method A101 or HAST 100 hrs 85% RH., 130°C, JEDEC STD 22-A110	LTPD = 5
Temp. cycle, 300 cycles, -65°C to 150°C, MIL-STD-883C, Method 1010	LTPD = 5
Pressure Pot, 168 hrs., 121°C, 2.0 atm., no bias	LTPD = 5
Low Temperature Operating Life 500 hrs, -55°C, $V_{cc} = V_{ccmax}$, 8 to 15Mhz	< 20 FIT due to programmed ViaLink element

All life test devices were programmed with a proprietary reliability pattern, which stresses the programmed and unprogrammed ViaLinks. A failure is defined as any change in the DC characteristic beyond the data sheet limits and any measurable change in the AC performance.

ACCELERATED LIFE TESTS AND RESULTS

High Temperature Operating Life Test

HTOL is the life test, which operates the device at a high Vcc and high temperature. This test is used to determine the long-term reliability and failure rate of the device in the customer environment. The specific condition of this test is defined by MIL-STD-883D Quality Conformance Test. The devices are operated at Vccmax and 125°C for 1000 hours or 150°C for 500 hours. The acceleration due to temperature can be calculated by using equation (1), assuming an average activation energy of 0.7 eV and an operating ambient temperature of 55°C. The acceleration factor from equation (1), for 55°C and $E_a = 0.7$ eV is 69 for 125°C life test and 224 for 150°C life test.

Failure Rate Calculation

Reliability is the probability that a semiconductor device will perform its specified function in a given environment for a specified period. In other words, reliability is quality over time and environmental conditions. The most frequently used reliability measure for semiconductor devices is the failure rate (λ). The failure rate is obtained by dividing the number of failures observed by the product of the number of devices on test and the interval in hours, usually expressed as percent per thousand hours or failures per billion device hours (FITS). This is called a point estimate because it is obtained from observations on a portion (sample) of the population of devices. To project from the sample to the population in general, one must establish confidence intervals. The application of confidence intervals is a statement of how “confident” one is that the sample failure rate approximates that for the population. To obtain failure rates at different confidence levels, it is necessary to make use of specific probability distributions. The chi-square (χ^2) distribution that relates observed and expected frequencies of an event is frequently used to establish confidence intervals. Chi-square values for 60% confidence intervals for up to 12 failures are shown in Table 3. The relationship between failure rate and the chi-square distribution is as follows:

$$\lambda = \frac{\chi^2(\alpha, \text{d. f.})}{2t}$$

Where:

λ = failure rate

χ^2 = chi-square function

α = (100 – confidence level) / 100

d.f. = degrees of freedom = $2r + 2$

r = number of failures

t = device hours

Table 3. Chi-Square Distribution Function 60% Confidence Level

No of Fails	χ^2 Quantity
0	1.833
1	4.045
2	6.211
3	8.351
4	10.473
5	12.584
6	14.685
7	16.780
8	18.868
9	20.951
10	23.031
11	25.106
12	27.179

The failure rate of semiconductor devices is inherently low. As a result, the industry uses a technique called accelerated testing to assess the reliability of semiconductors. During accelerated tests, elevated stresses are used to produce, in a short period, the same failure mechanisms as would be observed under normal use conditions. The objective of this testing is to identify these failure mechanisms and eliminate them as a cause of failure during the useful life of the product. Temperature, relative humidity, and voltage are the most frequently used stresses during accelerated testing. Their relationship to failure rates has been shown to follow an Eyring type of equation of the form:

$$\lambda = A \exp(\phi kT) * \exp(B/RH) * \exp(CE)$$

Where A, B, C, ϕ , and k are constants, more specifically B, C, and ϕ are numbers representing the apparent energy at which various failure mechanisms occur. These are called activation energies. ‘‘T’’ is the temperature, ‘‘RH’’ is the relative humidity, and ‘‘E’’ is the electric field. The most familiar form of this equation (shown on following page) deals with the first exponential term that shows an Arrhenius type relationship of the failure rate versus the junction temperature of semiconductors. The junction temperature is related to the ambient temperature through the thermal resistance and power dissipation. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then by applying known acceleration factors, estimate the failure rates for lower junction.

High Temperature Storage

High temperature storage test is a 150°C, 1000 hour, unbiased bake. This test accelerates failures due to mobile charge, thermal instabilities, and bond ball intermetallic formation. The results demonstrate the stability of the programmed and unprogrammed ViaLink element and the long term shelf life of the pASIC.

Temperature, Humidity and Bias

The temperature, humidity, and bias test is performed under severe environmental conditions. The device is exposed to a temperature of 85°C and a relative humidity of 85% for 1000 hours, while the pins are alternately biased between 0 and Vccmax voltage (JEDEC STD 22-B). An alternate temperature, humidity and bias test is HAST, a Highly Accelerated Stress Test. This test is similar to the 85°C/85% relative humidity test except that the test is done at 130°C and 85% relative humidity. The vapor pressure of at this condition is 33.5 psia. The pins are bias alternately at Vccmax voltage for 50 hours or 100 hrs (JEDEC STD 22-A110). Some parts were stressed more at a more stringent condition, 140C for 128 hours. These tests are effective at detecting corrosion problems, while also stressing the package and bonding wires.

Temperature Cycle Tests

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. The plastic package, lead frame, silicon die, and die materials expand and contract at different rates. This mismatch can lead to cracking, peeling, or delamination of the in the high stress layers. This test is typically performed to minimum and maximum temperatures of – 65°C to + 150°C for a duration of 300 or 1000 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The air-to-air cycling follows the MIL-STD-883D Quality Conformance Test.

Pressure Pot Tests

Autoclave is an environmental test that measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psi. Autoclave is a highly accelerated and destructive test. Typical test duration is 168 hours. This test forces moisture

into the plastic package and tests for corrosion in the bonding pads and wires, which are not protected by passivation. Corrosion can also occur in passivated areas where there are micro cracks or poor step coverage.

ViaLink ELEMENT RELIABILITY TESTS AND RESULTS

The ViaLink antifuse is a one time programmable device. In the unprogrammed state it has a resistance of greater than one gigaohm and capacitance of less than one femtofarad.

The application of a programming voltage across the antifuse structure, above a critical level causes the device to undergo a switching transition through a negative resistance region into a low resistance state. The magnitude of the current allowed to flow in the low resistance state, the programming current, is predetermined by design. A link of tungsten, titanium, and silicon alloy is formed between metal one and metal two during the programming process.

The link has a metallic-like resistivity of the order of 500 micro-ohms-cm and is responsible for the low 50 ohm resistance that is a unique characteristic of the QuickLogic ViaLink antifuse [3].

The link forms a permanent, bi-directional connection between two metal lines. The size of the link, and hence, the resistance, depends on the magnitude of the programming current. Figure 2 shows the relationship between programming current and programmed link resistance. Figure 3 shows the distribution of link resistance for a fixed programming current.

Unprogrammed ViaLink Element Reliability

Reliability studies on an antifuse focus on the ability of an unprogrammed and a programmed device under stress to remain in the desired state. In the context of standard IC testing, the antifuse should be stressed under conditions similar to those for a dielectric (in the unprogrammed state) and for a conductor (in the programmed state).

For ViaLink elements in the unprogrammed state, the tests must determine their ability to withstand applied voltages over the range of operating conditions without changing resistance or becoming programmed. Amorphous materials might be expected to show gradual changes in resistance as a result of relaxation or annealing. Reliability studies have been designed to explore these effects. An analysis of the unprogrammed reliability follows. A more detailed presentation of the unprogrammed ViaLink reliability mechanism was presented at the 1994 International Reliability Physics Symposium [5].

When a ViaLink element is stressed at high electric fields its resistance can decrease from the initial 1 G- Ω value. The reliability testing program examined the time for the resistance to reach 50 M- Ω at different stress fields. Figures 4 & 5 illustrate that because of time constraints (\approx 500 years), it is impossible to detect this effect at normal operating fields in systems. To keep the data consistent, all reported resistances are at 20°C unless specified.

The pASIC devices are designed to operate with resistances of the unprogrammed ViaLink element from 50 M- Ω to greater than 1 G- Ω at 20°C. Even with all unprogrammed ViaLink elements at 50 M- Ω , the pASIC devices remain within the guaranteed speed and standby I_{cc} specifications at all temperatures.

Figure 4 shows the time required for a ViaLink element to reach 50 M- Ω under various applied electric fields at different temperatures. The time required for the change is not accelerated by temperature over the studied range of electric fields. The activation energy, E_a , for this process is zero.

Figure 5 shows the time required for a ViaLink element to reach 50 M- Ω under various electric field stresses. A range of amorphous silicon thicknesses has been included in this chart. The data can be modeled using the equation,

$$t_{50M\Omega} = t_0 \exp(-BE) \quad (3)$$

Fig. 2. Resistance vs 1 / Programming Current
 $R = 0.810 / I_p$

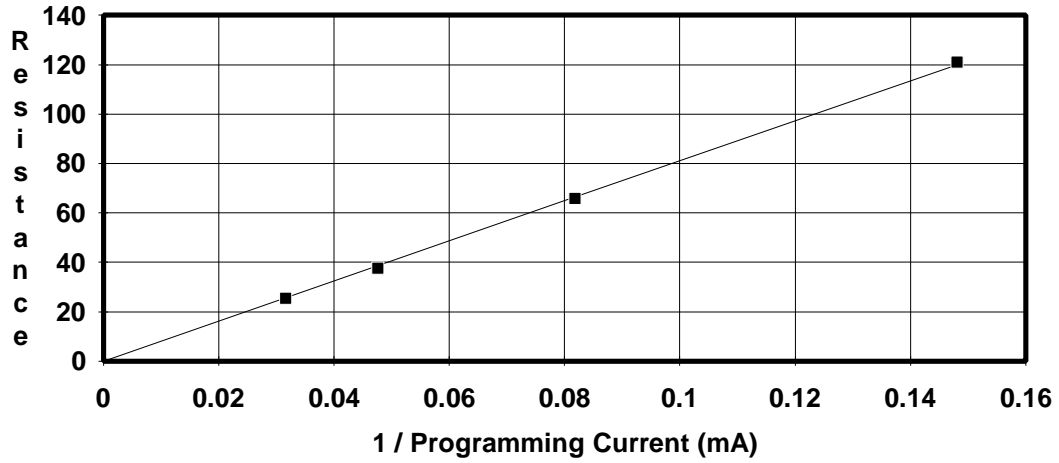
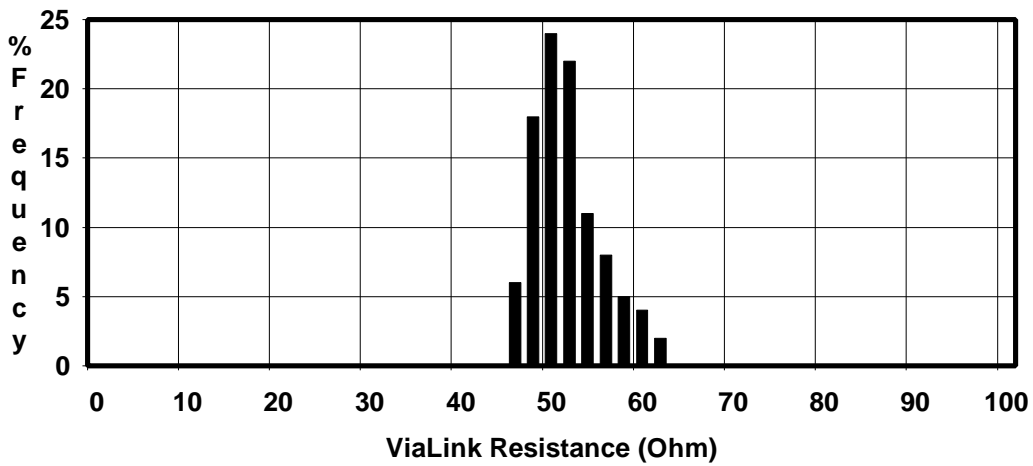


Fig. 3. Distribution of ViaLink Resistance at $I_p = 15$ mA
Average = 52.3 Ohms Std Deviation = 3.69



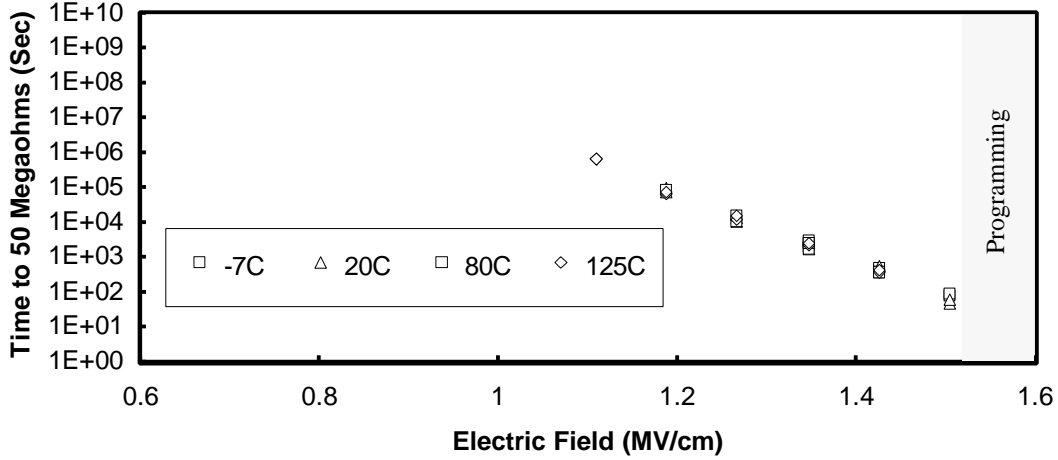
where the time to 50 M- Ω decreases exponentially with increasing applied electric field. The constant t_0 is 3×10^{15} seconds and the field acceleration factor, B, is 20 cm/MV. The model is valid for electric fields, E, below 1.5 MV/cm. Above this field, the amorphous silicon antifuse programs with a different mechanism. This mechanism is an advantage over dielectric antifuses where the unprogrammed reliability mechanism, Time Dependent Dielectric Breakdown, is the same as the programming mechanism. The electric field for 5.0 volt Vcc operation with a typical amorphous silicon thickness is 0.61 MV/cm, which extrapolates $t_{50M\Omega}$ to 1.5×10^{10} seconds, or 500 years. The time to 50 M- Ω for the worst case amorphous silicon thickness and operating at worst case Vcc is in excess of 30 years.

The high field effect is predicable, reproducible and reversible. This effect is inherent to the amorphous silicon in the ViaLink element [4]. The pASIC device has been designed to operate where the effect is minimized and has no impact on the reliability of the pASIC device. The pASIC device lifetime extrapolations are based on the average unprogrammed ViaLink element since the effect on the increased Icc of the pASIC is the sum of the leakages through the unprogrammed ViaLink elements. The time dependent resistance of the ViaLink elements does not degrade the functionality or AC performance of the pASIC.

Accelerated Stress Tests for Unprogrammed ViaLink Elements

The high field effect is created in the packaged pASIC devices through a high Vcc static life test. This test stresses the unprogrammed ViaLink element with a Vcc = 7.0 volts for 1000 hours. Over 600 pASIC devices from twelve lots have been tested. This condition stresses over 20,000 unprogrammed ViaLink elements in each QL8X12. The failure criteria for the pASIC device for this test is the same as the previous tests, with emphasis placed on the standby Icc, which increases as the resistance of the unprogrammed ViaLink element decreases. The acceleration factor for this stress is calculated by using equation (3) to find the ratio of the $t_{50M\Omega}$ for E = 0.61 MV/cm at 5 volts and E = 0.85 MV/cm at 7 volts. This test has an acceleration factor = 130 for the unprogrammed ViaLink element. The test results in Table 3 show that no device has failed this stress in more than 220 million equivalent device hours. Four lots have 6000 hours of test which is equivalent over 80 years of operation. The High Vcc Static test was not done on the 0.65 micron pASICs because the submicron CMOS devices are not reliable at these very high voltages. The reliability stresses of the unprogrammed ViaLink for the 0.65 micron process was done on test structures where the ViaLink could be stress independently from the CMOS.

**Fig. 4. Temperature Dependence of Time to 50 Megaohms
Lot 617 Wafer 8**



**Fig. 5. Electric Field Acceleration of Unprogrammed ViaLink
Element from 6 Production Lots**

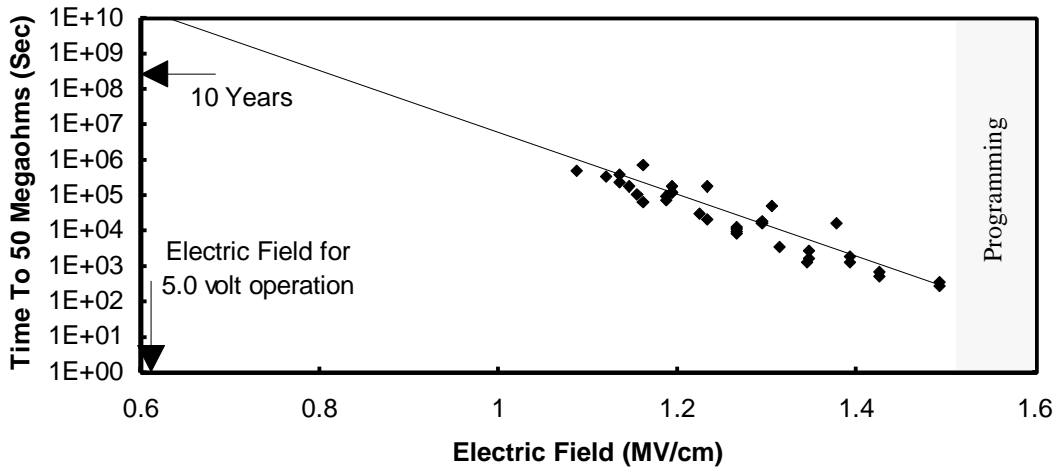


Table 3. Results of High V_{cc} Static Life Test

High Vcc Static Life Test

Vcc = 7.0v, Static, Temp = 25C

Package	Fab lot	Device	Quantity	Total hours	Failures	Equivalent dev hrs
68 PLCC	16558	QL8X12	14	3650	0	6.6E+06
68 PLCC	18362	QL8X12	38	1907	0	9.4E+06
68 PLCC	19194	QL8X12	110	1756	0	2.5E+07
68 PLCC	19618	QL8X12	101	1464	0	1.9E+07
68 PLCC	20454	QL8X12	100	2800	0	3.6E+07
68 PLCC	34515	QL8X12	37	1000	0	4.8E+06
68 PLCC	35421	QL8X12	36	1000	0	4.7E+06
68 PLCC	35422	QL8X12	33	1000	0	4.3E+06
68 PLCC	33403	QL8X12A	100	1000	0	1.3E+07
68 PLCC	34515	QL8X12A	36	6000	0	2.8E+07
68 PLCC	35421	QL8X12A	34	6000	0	2.7E+07
68 PLCC	35422	QL8X12A	36	6000	0	2.8E+07
Total			675		0	2.2E+08

Programmed ViaLink Element Reliability

The reliability tests on the programmed ViaLink element must demonstrate the stability of the link resistance in the programmed state. While an increase in resistance of the programmed device may not be catastrophic, a higher resistance can affect the device operating speed. Because the programmed ViaLink element is part of the on-chip interconnect, reliability tests should be similar to those that are normally used to validate the integrity of metal interconnects.

In operation, the programmed ViaLink elements are subjected to capacitive switching current of the interconnect network. They do not experience any DC current or voltage. See Figure 6. Each switching pulse forces a capacitive charging current to flow through programmed ViaLink elements into the network on the rising edge, and an opposite, or discharging current, to flow on the falling edge. Each cycle is analogous to a read pulse for a memory device. A 10% increase in resistance was set as the read disturb criteria for the ViaLink element. The typical impedance of a network is about 500Ω with the programmed ViaLink element contributing 50Ω. A 10% increase in the ViaLink resistance will increase the network impedance by approximately 5Ω, or 1%. This increase in resistance will increase a network delay in the pASIC device by about the same proportion.

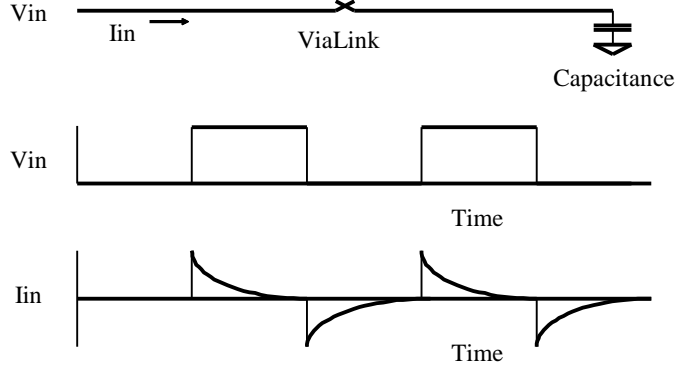


Fig. 6. Switching of Programmed ViaLink Antifuse

Programmed ViaLink elements were stressed under severe capacitive currents. AC stresses rather than DC stresses were used to accelerate the failures for closer correlation with actual operation. Figure 7 shows that the mean number of read cycles to disturb, N_{50} , for 25°C and 250°C is identical. The lack of an observable temperature dependence indicates that the activation energy is 0, or the self heating in the antifuse is high enough to make the 225°C ambient delta insignificant. Figure 8 shows the acceleration of the read disturb at high AC current densities through the programmed ViaLink element. Thus, the number of cycles to disturb can be modeled as,

$$N_{50} = N_0 \exp(-PJ) \quad (4)$$

Where $N_0 = 7 \times 10^{41}$ cycles is a constant, $P = 1.2 \text{ cm}^2/\text{MA}$ is the current density acceleration factor, and J is the peak AC current density through the link [6].

The pASIC is designed to operate at worst case AC current density of $35 \times 10^6 \text{ A/cm}^2$. The N_{50} for this condition is 4×10^{23} cycles. The failure rate can be calculated using the cumulative density $F(t)$,

$$F(t) = \Phi \ln [(N/N_{50})/\sigma] \quad (5)$$

The failure distribution can be determined by plotting the data on a log normal probability scale versus the log of the number of cycles to failure. See Figure 7. The shape parameter, σ , is $\ln(N_{50}/N_{16}) = 2.5$. The shape parameter is relatively large because it includes the measurement tolerances of the current density.

Fig 7. Temperature Dependence of Accelerated Read Disturb

J is the same for both temperatures

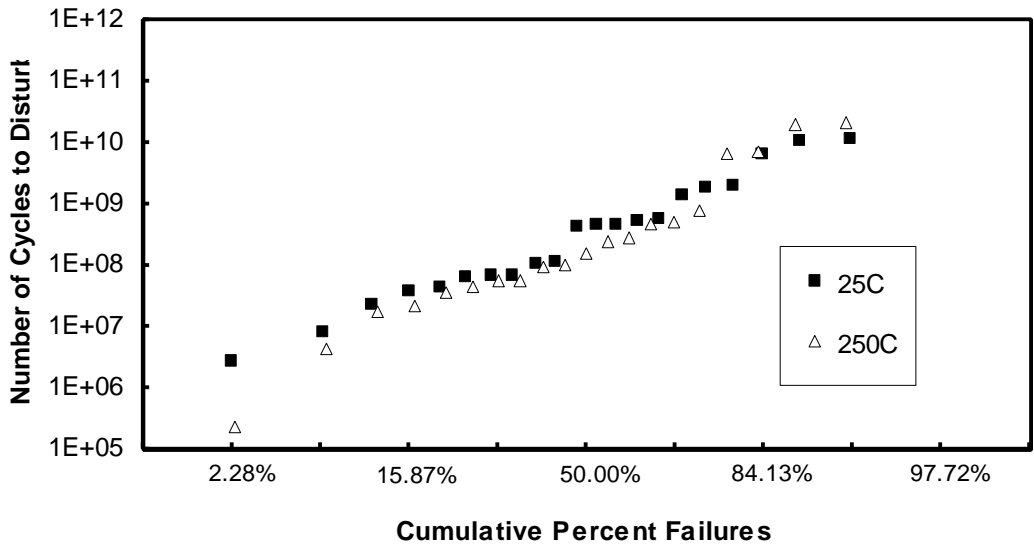
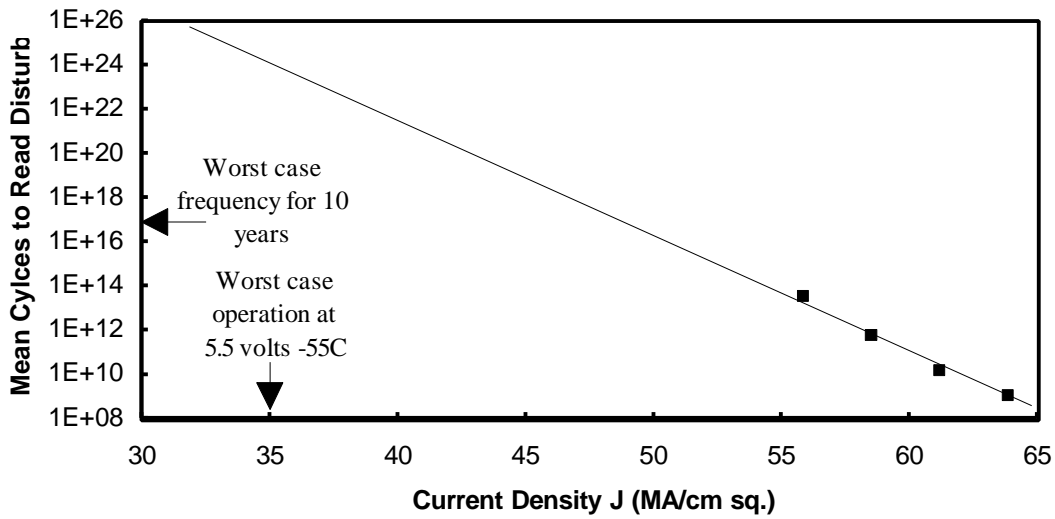


Fig. 8. Acceleration of Read Disturb for Programmed ViaLink Element



High AC current density occurs at low frequencies where there is sufficient time for the network to be fully charged or discharged. At frequencies above 50 MHz, AC current through a ViaLink element decreases due to incomplete charging and discharging cycle. The worst case process, programming and operating conditions will produce an operating current density of 35×10^6 A/cm² in the present pASIC devices. Using equation (5), the cumulative failure rate for the ViaLink element operating at 35×10^6 A/cm² for 1.6×10^{16} read cycles (equivalent to continuous operation at 50 MHz for 10 years) is less than 0.1 parts per billion. The worst case pattern in a programmed QL16x24B has less than 1200 ViaLink elements operating at the high current density. Most of the programmed ViaLink elements operate at much lower current densities. The failure rate of the programmed ViaLink element in the QL16x24B contributes less than 0.01 FIT to the overall failure rate.

Results of High Temperature Operating Life Test

The pASIC device is a highly reliable Field Programmable Gate Array. The addition of the ViaLink to a CMOS process does not measurably increase the failure rate of the pASIC devices above that of normal CMOS logic products. The following is the summary of the High Temperature Operating Life data for all the pASIC devices. The four failures were not related to the ViaLink.

Total Equivalent Device Hours at 55° C: 400,000,000
 60% Confidence FIT: **12**

High Temperature Operating Life Test

Vcc = 5.5V, Dynamic, f = 1 MHz, Temp = 125C

Package	Fab lot	Device	Quantity	168	Failures @ hours	
					500	1000
68 PLCC	18362	QL8X12	100	0	0	0
68 PLCC	19194	QL8X12	100	0	0	0
68 PLCC	19618	QL8X12	100	0	0	0
68 PLCC	20454	QL8X12	100	0	0	0
68 PLCC	20470	QL8X12	76	0	0	0
68 PLCC	20534	QL8X12	82	0	0	0
68 PLCC	21786	QL8X12	76	0	0	0
68 PLCC	33669	QL8X12	70	0	0	0
68 PLCC	34515	QL8X12	100	0	0	0
68 PLCC	35421	QL8X12	100	0	0	0
68 PLCC	34267	QL8X12A	100	0	0	0
68 PLCC	36129	QL8X12A	100	0	0	0
68 PLCC	40673	QL8X12A	51	0	0	0
68 PLCC	1346945	QL8X12B	100	0	0	0
68 PLCC	1351104	QL8X12B	100	0	0	0
68 PLCC	1409354	QL8X12B	100	0	0	1
84 PLCC	20762	QL12X16	100	0	0	0
84 PLCC	22164	QL12X16	100	0	0	1
84 PLCC	23001	QL12X16	100	0	0	0
84 PLCC	23093	QL12X16	36	0	0	0
84 PLCC	22988	QL12X16	32	0	0	0
84 PLCC	23091	QL12X16	38	0	0	0
84 PLCC	35284	QL12X16	100	0	0	0
84 PLCC	36935	QL12X16	100	0	0	0
84 PLCC	36936	QL12X16	98	0	0	0
84 PLCC	37448	QL12X16	65	0	0	0
84 PLCC	37449	QL12X16	74	0	0	0
84 PLCC	39068	QL12X16	54	0	0	0
84 PLCC	40670	QL12X16	50	0	0	0
84 PLCC	40672	QL12X16	50	0	0	0
84 PLCC	1415570	QL12X16B	67	0	0	0

84 PLCC	1418672	QL12X16B	73	0	0	0
84 PLCC	1328491	QL16x24B	2	0	0	0
84 PLCC	1337713	QL16x24B	22	0	0	0
84 PLCC	1337739	QL16x24B	19	0	0	0
84 PLCC	1407324	QL16X24B	20	0	0	0
84 PLCC	1407325	QL16X24B	38	0	0	0
84 PLCC	1413492	QL16X24B	6	0	0	0
84 PLCC	5-6	QL16X24B	24	0	0	0
84 PLCC	15-18	QL16X24B	46	0	0	0
84 PLCC	various	QL16X24B	9	0	0	0
208 PQFP	1452956*	QL 24X32B	50	0	0	
208 PQFP	1507188*	QL 24X32B	15	0	0	
208 PQFP	1509257*	QL 24X32B	106	0	0/76	
208 PQFP	1511279*	QL 24X32B	199	0	0	
208 PQFP	1515408*	QL 24X32B	80	0	0	
208 PQFP	2606566*	QL2007	50	0	0	
208 PQFP	2608853*	QL2007	50	1	0	
208 PQFP	2608853*	QL2007	46	0	0/25	
208 PQFP	2610103*	QL2007	50	0	0	
208 PQFP	2615768*	QL2009	50	0	0	
280 PQFP	2641048*	QL2009	50	0	0	
280 PQFP	2649998*	QL2009	50	0	0	
84PLCC	2630668*	QL2005	50	0	0	
84PLCC	2630679*	QL2005	50	0	0	
84PLCC	2647844*	QL2003	50	0	0	
84PLCC	2648952*	QL2003	50	0	0	
68PLCC	2733102*	QL8X12B	50	0	0	
84PLCC	2722759.E1*	QL2003	50	0	0	
84PLCC	2721664*	QL2003	50	0	0	
208PQFP	2709184.E2*	QL2009	50	0	0	
208PQFP	2712514.E*	QL2009	100	0	0	
208PQFP	2712514*	QL2009	50	0	0	
208PQFP	2722806.E1*	QL2005	50	0	0	
208PQFP	2730778.E2*	QL2009	50	1	0	
208PQFP	2709184.E3*	QL2009	100	0	0	
208PQFP	2730778.E1*	QL2009	100	0	0	
Total			4424	2	0	2

* Temperature = 150°C

High Temperature Operating Life Test

V_{cc} = 3.6V, Dynamic, f = 1 MHz, Temp = 150C

Package	Fab lot	Device	Quantity	Failures @ hours		
				168	500	1000
208PQFP	D60112.00	QL3025	50	0	0	
208PQFP	D60112.01	QL3025	50	0	0	
208PQFP	D60200.00	QL3025	100	0	0	
208PQFP	D60111.00	QL3025	50	0	0	
208PQFP	D60266.00	QL3060	50	0	0	
208PQFP	D60265.00	QL3060	50	0	0	
Total			350	0	0	

The pASIC devices do not have a significant infant mortality failure rate. There were only two failures during the first 168 hours of life test. Therefore, from the results shown above, the pASIC has been operating for 400 million equivalent device hours with four failures. One was due to a gate oxide failure. The failure in the QL8X12B was due to a particle at via etch. The last two failures were due to a metal short. The particles have been significantly reduced as part of an ongoing quality and yield improvement.

High Temperature Storage Test

No bias, Temp = 150C

Package	Fab lot	Device	Quantity	168	Failures @ hours	
					500	1000
68 PLCC	18362	QL8X12	35	0	0	0
68 PLCC	19194	QL8X12	35	0	0	0
68 PLCC	19390	QL8X12	35	0	0	0
68 PLCC	34515	QL8X12	35	0	0	0
68 PLCC	35421	QL8X12	35	0	0	0
68 PLCC	35422	QL8X12	35	0	0	0
208 PQFP	2701240*	QL2009	45	0	0	0
144 TQFP	2712469*	QL2007	45	0	0	0
84 PLCC	2640901*	QL2007	43	1	0	0
Total			343	1	0	0

* at 165C

The one failure at 165°C was due to input leakage, which was not bake recoverable.

Temperature, Humidity, and Bias Test

Temp = 85C, 85% R.H., pins alternately biased at 5.5v

Package	Fab lot	Device	Quantity	168	Failures @ hours	
					500	1000
68 PLCC	19194	QL8X12	100	0	0	0
68 PLCC	19618	QL8X12	100	0	0	0
68 PLCC	19454	QL8X12	100	0	0	0
68 PLCC	34515	QL8X12	35	0	0	0
68 PLCC	35421	QL8X12	35	1	0	0
68 PLCC	35422	QL8X12	35	0	0	0
84 PLCC	20762	QL12X16	29	0	0	0
84 PLCC	23000	QL12X16	24	0	0	0
84 PLCC	23001	QL12X16	24	0	0	0
Total			482	1	0	0

Temp = 130C, 85% R.H., pins alternately biased at 5.5v

Package	Fab lot	Device	Quantity	Failure @ hours	
				50	128@140C
100TQFP	36936	QL12X16	15	0	
100TQFP	37447	QL12X16	13	0	
100TQFP	37448	QL12X16	17	0	
68PLCC	1409354	QL8X12B	25		0
68PLCC	1409353	QL8X12B	20		0
84PLCC	1402176	QL16X24B	30		0
84PLCC	1402177	QL16X24B	15		0
84PLCC	1410389	QL16X24B	15		0
84PLCC	1408334	QL16X24B	16		0
84PLCC	1450263	QL16X24B	14		0
84PLCC	1417657	QL16X24B	22		0
84PLCC	10885	QL16X24B	2		0
144TQFP	1412454	QL16X24B	14	0	
144TQFP	1413492	QL16X24B	15	1	
144TQFP	49403007	QL16X24B	16	0	

144TQFP	1411431	QL16X24B	15	0
144TQFP	1417657	QL16X24B	45	0
208 PQFP	1508232	QL 24X32B	11	0
208 PQFP	1513339	QL 24X32B	79	0
208 PQFP	2606566	QL2007	77	0
256BGA	2639818	QL2009	45	0
Total			521	1 0

The above result shows that the pASIC had three failures from the total 482 units in 85/85 and one failure in HAST. The first failure was a short due a particle under metal 2. The one HAST failure in the QL16X24B was due to a metal short. The ongoing quality and yield improvement effort has reduced the defect level.

Temperature Cycle Test
Air-to-air, -65C to 150C

Package	Fab lot	Device	Quantity	Failures @ Cycle		
				250	500	1000
68 PLCC	18362	QL8X12	35	0	0	0
68 PLCC	19194	QL8X12	35	0	0	0
68 PLCC	19618	QL8X12	35	0	0	0
68 PLCC	34515	QL8X12	35	0	0	0
68 PLCC	35421	QL8X12	35	0	0	0
68 PLCC	35422	QL8X12	35	0	0	0
68 PLCC	39017	QL8X12A	38	0	0	0
84 PLCC	20762	QL12X16	29	0	0	0
84 PLCC	22999	QL12X16	24	0	0	0
84 PLCC	23000	QL12X16	24	0	0	0
84 PLCC	39068	QL12X16	85	0	0	1
84 PLCC	38980	QL12X16	37	0	0	0
84 PLCC	38979	QL12X16	65	0	0	0
100TQFP	36934	QL8X12A	30	0	0	0
100TQFP	36128	QL8X12A	30	0	0	0
100TQFP	36129	QL8X12A	30	0	0	0
100TQFP	37447	QL12X16	30	0	0	0
100TQFP	37448	QL12X16	30	0	0	0
100TQFP	36936	QL12X16	30	0	0	0
84PLCC	1409378	QL12X16B	30	0	-	0
84PLCC	1417657	QL16X24B	31	0	-	0
84PLCC	1416600	QL16X24B	16	0	-	0
144TQFP	1342851	QL16X24B	25	0	-	0
144TQFP	1405263	QL16X24B	15	0	-	0
144TQFP	1351123	QL16X24B	15	0	-	0
144TQFP	1417657	QL16X24B	30	0	-	0
208 PQFP	1445679	QL 24X32B	45	0	-	0
208 PQFP	1452955	QL 24X32B	30	0	-	0
208 PQFP	1452956	QL 24X32B	15	0	-	0
144TQFP	1509242	QL 24X32B	45	0	-	0
208 PQFP	2606566	QL2007	45	0	-	0
208 PQFP	2608853	QL2007	44	0	-	0
208 PQFP	2615768	QL2009	50	0	-	-
208 PQFP	2641048	QL2009	50	0	-	-
208PQFP	2709184.E1	QL2009	50	0	-	-
208PQFP	0925AENG2	QL3025	23	0	-	-
208PQFP	WAFER4	QL3025	22	0	-	-
208PQFP	2648936.E	QL24X32B	23	0	-	-
208PQFP	2650159.E	QL24X32B	22	0	-	-
144TQFP	0925AENG3	QL3025	23	0	-	-

144TQFP	WAFER3	QL3025	22	0	-	-
84PLCC	D60251.00	QL3012	23	0	-	-
84PLCC	D60298.00	QL3012	22	0	-	-
256PBGA	D60111	QL3025	22	0		
256PBGA	D60112	QL3025	23	0		
256PBGA	2639818	QL2009	45	0		
208PQFP	D60266.00	QL3060	45	1		
208PQFP	D60265.00	QL3060	45	0		
208PQFP	D60427.00	QL3060	45	0		
Total			1633	1	0	1

The results show that the pASIC had one failure. The failure was due to a lifted bond. The second failure was due to cracked passivation.

Pressure Pot Test

Pressure = 2.0 atm., Temp = 121C, no bias

Package	Fab lot	Device	Quantity	48	Failures @ hours	
					96	168
68 PLCC	18362	QL8X12	35	0	0	0
68 PLCC	19194	QL8X12	35	0	0	0
68 PLCC	19390	QL8X12	35	0	0	0
68 PLCC	34515	QL8X12	35	0	0	0
68 PLCC	35421	QL8X12	35	0	0	0
68 PLCC	35422	QL8X12	35	0	0	0
84 PLCC	20762	QL12X16	28	0	0	0
84 PLCC	22999	QL12X16	25	0	0	0
84 PLCC	23000	QL12X16	24	0	0	0
100TQFP	36936	QL12X16	15	-	-	0
100TQFP	37447	QL12X16	15	-	-	0
100TQFP	37448	QL12X16	15	-	-	0
68PLCC	1346945	QL8X12B	15	-	-	0
68PLCC	1350096	QL8X12B	15	-	-	0
68PLCC	1350104	QL8X12B	15	-	-	0
84PLCC	1417657	QL16X24B	30	-	-	0
84PLCC	1416600	QL16X24B	15	-	-	0
84PLCC	1409360	QL16X24B	36	-	-	0
84PLCC	1410389	QL16X24B	15	-	-	0
84PLCC	1350093	QL16X24B	15	-	-	0
84PLCC	1403209	QL16X24B	15	-	-	0
84PLCC	1402177	QL16X24B	15	-	-	0
144TQFP	1342851	QL16X24B	15	-	-	0
144TQFP	1405263	QL16X24B	15	-	-	0
144TQFP	1351123	QL16X24B	15	-	-	0
144TQFP	1417657	QL16X24B	30	-	-	0
208 PQFP	1445679	QL 24X32B	30	-	-	0
208 PQFP	1452955	QL 24X32B	30	-	-	0
208 PQFP	1452956	QL 24X32B	30	-	-	0
208 PQFP	2606566	QL2007	45	-	-	0
208 PQFP	2615768	QL2009	45	-	-	0
208PQFP	0925AENG2	QL3025	23	-	-	0
208PQFP	WAFER4	QL3025	22	-	-	0
144TQFP	0925AENG3	QL3025	23	-	-	0
144TQFP	WAFER3	QL3025	22	-	-	0
84PLCC	D60251.00	QL3012	23	-	-	0
84PLCC	D60298.00	QL3012	22	-	-	0
256PBGA	D60111	QL3025	22			0

256PBGA	D60112	QL3025	23	0
256PBGA	2639818	QL2009	45	0
208PQFP	D60266.00	QL3060	23	0
208PQFP	D60265.00	QL3060	22	0
Total			1043	0

Accelerated Stress Tests for Programmed ViaLink elements

The low temperature operating life test stresses the pASIC devices with $V_{cc} = V_{ccmax}$ at approximately 15 MHz for 500 hours at -55°C . The lack of an ambient temperature dependence on read disturb allow QuickLogic to stress at any temperature without changing the deprogramming cycle dependence. Cold temperature operation was chosen because it accelerates the stress by increasing the drive current of the CMOS devices. This test stresses the programmed ViaLink elements at $40 \times 10^6 \text{ A/cm}^2$ for 5.4×10^{13} cycles. The acceleration factor, calculated from equation (4), is 380. This test is equivalent to 2.0×10^{16} switching cycles or continuous operation under worst case condition at 50 MHz for 12 years at the worst case current density of $35 \times 10^6 \text{ A/cm}^2$. Over 1000 pASIC devices from many lots have been stressed. The failure criteria are the same as previously described, with emphasis placed on careful monitoring of AC performance. Test results below show that there have been no failures of the programmed ViaLink.

Low Temperature Operating Life Test

$V_{cc} = 6.0\text{v}$, Dynamic, $f = 15\text{MHz}$, Temp = -55°C

Package	Fab lot	Device	Quantity	168	Failures @ hours	
					500	1000
68 PLCC	34267	QL8x12A	100	0	0	0
68 PLCC	36128	QL8x12A	100	0	0	0
68 PLCC	36129	QL8x12A	150	0	0	0
68 PLCC	36934	QL8x12A	70	0	0	0
84 PLCC	20762	QL12X16	100	0	0	0
84 PLCC	22999	QL12X16	100	0	0	0
84 PLCC	23001	QL12X16	100	1	0	0
84 PLCC	36935	QL12X16	100	0	0	0
84 PLCC	36936	QL12X16	100	2	0	0
84 PLCC	38713	QL12X16	50	0	0	0
84 PLCC	1323368	QL16x24B	4	0	0	0
84 PLCC	1337713	QL16x24B	10	0	0	0
84 PLCC	1337739	QL16x24B	20	0	0	0
68 PLCC	1409353	QL8X12B	150	0	0	0
68 PLCC	1409354	QL8X12B	150	0	0	0
84 PLCC	1409390	QL12X16B	200	0	0	0
84 PLCC	1409360	QL12X16B	40	0	0	0
84 PLCC	1410389	QL16X24B	33	0	0	0
84 PLCC	404333	QL16X24B	66	0	0	0
84 PLCC	404788	QL16X24B	1	0	0	0
208 PQFP	1452956	QL 24X32B	50	0	0	0
208 PQFP	1507188	QL 24X32B	50	0	0	0
208 PQFP	1509257	QL 24X32B	47	0	0	0
208 PQFP	2608853	QL2007	50	0	0	0
208 PQFP	2606566	QL2007	50	0	0	0
208 PQFP	2610103	QL2007	49	0	0	0
208 PQFP	2615768*	QL2009	50	0	0	0
208 PQFP	2630678*	QL2009	50	0	0	0

208 PQFP	2641048*	QL2009	50	0		
84PLCC	2630668*	QL2005	50	0	0	
84PLCC	2630679*	QL2005	50	0	0	
84PLCC	2642211*	QL2005	50	0		
84PLCC	2647844*	QL2003	50	0	0	
84PLCC	2648952*	QL2003	50	0	0	
84PLCC	2703449*	QL2003	50	0		
68PLCC	2701210*	QL8X12B	50	0	0	
84PLCC	2625023*	QL16X24B	25	0	0	0
84PLCC	2631793*	QL16X24B	25	0	0	0
84PLCC	2639765*	QL16X24B	45	0	0	0
84PLCC	2634242*	QL16X24B	5	0	0	0
84PLCC	2719338M.E1*	QL2003	50	0	0	
84PLCC	2711389*	QL2003	50	0		
84PLCC	2722759.E*	QL2003	50	0	0	
84PLCC	2712664*	QL2003	50	0	0	
84PLCC	2709181*	QL2005	50	0		
84PLCC	2705678*	QL2005	50	0	0	
84PLCC	2702389*	QL2005	50	0		
84PLCC	608528*	QL12X16B	100	0	1	
208PQFP	2709184.E2*	QL2009	50	0	0	
208PQFP	2712514*	QL2009	50	0	0	
208PQFP	2719339.E*	QL2005	50	0	0	
208PQFP	2648909*	QL24X32B	50	0	0	
208PQFP	2726218.E3*	QL2007	50	0	0	
208PQFP	2711388*	QL2007	50	0	0	
208PQFP	2708067*	QL2007	50	0		
208PQFP	2708050*	QL2007	50	0		
208PQFP	2705747*	QL2009	50	0	0	
208PQFP	2706892*	QL2009	50	0		
208PQFP	2709134*	QL2009	50	0		
208PQFP	2649052*	QL2007	47	0	0	
208PQFP	2647843*	QL2007	48	0	0	
Total			3635	3	1	0

* T= -65°C Vcc=5.5V

Low Temperature Operating Life Test

Vcc = 3.6v, Dynamic, f = 15MHz, Temp = -65°C

Package	Fab lot	Device	Quantity	168	Failures @ hours	
					500	1000
208PQFP	0827AENG1	QL3025	50	0	0	
208PQFP	D60200.00	QL3025	54	0	0	
208PQFP	WAFER4	QL3025	50	0	0	
208PQFP	D60112.01	QL3025	50	0	0	
208PQFP	D60112.01	QL3025	50	0	0	
208PQFP	D60265.00	3060	50	0	0	
208PQFP	D60427.00	3060	50	0	0	
208PQFP	D60266.21	3060	50	0		
Total			4044	0	0	

This Low Temperature Operating Life test stresses the programmed ViaLinks at 40×10^6 A/cm². The acceleration factor for this test is 380. The results in above show no failure on programmed ViaLink elements in over 110 million equivalent device hours. There were four failures unrelated to the ViaLink element. Two were a metal one to metal two short. The other two devices shorted when a power surged. We have corrected the power supply problem.

Conclusion on Life Tests

The testing reported here establishes the reliability of the pASIC devices. No failures have been observed in 400 million equivalent device hours of high temperature operating life. The observed failure rate is 10 FIT and the failure rate with a 60% confidence is 12 FIT with no significant infant mortality. The acceleration factors that can lead to the degradation of the programmed and unprogrammed ViaLink elements were studied. The pASIC devices are designed to operate at voltages and currents where the failure rate of the ViaLink element does not measurably increase the failure rate of the pASIC device above that of normal CMOS products.

Up to date data on new parts can be obtained from QuickLogic.

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