

Introduction

This report summarizes QuickLogic Product Reliability. QuickLogic has established aggressive reliability objectives to assure that all products exhibit reliability exceeding customer reliability requirements for purchased components. In addition, the QuickLogic quality standard results in a culture requiring continuous product improvement in quality and reliability. This report includes data from the QuickLogic 0.65 μ m, 0.35 μ m, and 0.25 μ m technology families.

Product Reliability data is accumulated as a result of new product Qualification plan activities as well as from the Reliability and Quality Monitoring program. All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. The reliability strategy requires that every failure encountered during reliability testing be subjected to failure analysis to determine the failure mechanism. A corrective action is then implemented to prevent future failures. The result of this process is continuous improvement in product performance and reliability.

Reliability and Quality Monitoring Programs

The Reliability and Quality Monitoring programs of new processes, new products/devices and new package/assembly vendors are designed to ensure that QuickLogic products satisfy the internal and external customer requirements before transfer into production.

The Reliability and Quality Monitoring program requirements are outlined in **Table 1** through **Table 4**.

Table 1: Requirement for Wafer Process Qualification

Test #	Reliability Test	Reference Spec Mil-Std-883/ JEDEC/STACK	Condition	Duration	Lot Qty	SS/Lot	Acceptance
A	High Temperature Operating Life (HTOL)	Mil-Std-883 Mtd 1005	T = 125°C, Vccmax Dynamic OR Vccmax, T = 125°C ^a	168, 1000 hrs Optional Read Pt 500 OR 168, 500 hrs	3	50	0 fail
B	Low Temperature Operating Life (LTOL)	Mil-Std-883 Mtd 1005	T = -65°C, Vccmax, 1 MHz	168, 500 hrs	3	50	0 fail
C	Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	JESD22-A101, JEDEC22-A113 OR JESD22-A110, JEDEC22-A113	T = 85°C, 85% R.H., Pins alt. Bias Vccmax OR T = 110°C, 85% R.H., 17.7psia, Pins alt. Bias Vccmax	Post Preconditioning, 168, 500, 1000 hrs OR Post Preconditioning, 264 hrs	1 or 2	45 (min. sample size)	LTPD = 5 @90% confidence
D	Temperature Cycling (TC) with Preconditioning	JESD22-A104, JEDEC22-A113	T = -65°C/+150°C OR For Laminate, T = -55°C/+125°C ^b	300 cycles OR 1,000 cycles	1 or 2	45 (min. sample size)	LTPD = 5 @90% confidence
E	High Temperature Storage (HTS)	Mil-Std-883 Mtd 1008	T = 150°C, unbiased	168 Opt., 500 Opt., 1,000 hrs	1 or 2	45 (min. sample size)	LTPD = 5 @90% confidence
F	SEM Analysis or Construction Analysis				1	1	

- a. For 0.35µm and older technology, the temperature is 150°C.
- b. For Plastic Quad Flat Pack (PQFP) packages use conditions of -65°C/+150°C (Air to Air) and 300 cycles.
For Plastic Ball Grid Array (PBGA) packages use conditions of -55°C/+125°C (Air to Air) and 1000 cycles.

Table 2: Requirement for Device Qualification

Reliability Test	Reference Spec Mil-Std-883/ JEDEC/STACK	Condition	Duration	Lot Qty	SS/Lot	Acceptance
ESD	Mil-Std-883 Mtd 3015.7	HBM	> 2000 Volts all Pins	3	3	0 fail
Latch-Up	EIA / JESD78	QL Spec 08-003	Current injection T = 25°C	3	3	0 fail

Table 3: Requirement for Plastic Package / Assembly Qualification

Test #	Reliability Test	Reference Spec Mil-Std-883/ JEDEC/STACK	Condition	Duration	Lot Qty	SS/Lot	Acceptance
1	Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	JESD22-A101-B, JESD22-A113 OR JESD22-A110, JESD22-A113	T = 85°C, 85% R.H., Pins alt. Bias Vccmax OR T = 110°C, 85% R.H., 17.7 psia, Pins alt. Bias Vccmax	Post Preconditioning, 168, 500, 1000 hrs OR Post Preconditioning, 264 hrs	1 or 2	45 (min. sample size)	LTPD = 5 @90% confidence
2	Temperature Cycling (TC) with Preconditioning	JESD22-A104, JEDEC22-A113	T = -65°C/+150°C OR For Laminate, T = -55°C/+125°C	300 cycles OR 1,000 cycles	1 or 2	45 (min. sample size)	LTPD = 5 @90% confidence
3	High Temperature Storage (HTS)	Mil-Std-883 Mtd 1008	T = 150°C, unbiased	168 Opt, 500 Opt, 1,000 hrs	1 or 2	45 (min. sample size)	LTPD = 5 @90% confidence
4	Pressure Pot with Preconditioning ^a OR Unbiased HAST with Preconditioning ^a	JESD22-A102-C, JEDEC22-A113 OR JESD22-A118, JEDEC22-A113	T = 121°C, 30 psia, saturated steam OR T = 110°C, 85% R.H., 17.7 psia	96 hrs OR 264 hrs	1 or 2	45 (min. sample size)	LTPD = 5 @90% confidence
5	Moisture Resistance	JESD22-A112	Per Spec JESD22-A112		3	3	Determine Level
6	Solderability	Group B7 Mil-Std-883			1	3	LTPD = 5 @90% confidence
7	Lead Fatigue				1	3	0 fail
8	Ball Shear				1	5	0 fail
9	Bond Pull				1	5	0 fail
10	Physical Dimension				3	15	LTPD = 5 @90% confidence

a. Unbiased HAST for BGA package and Pressure Pot for all other packages

Table 4 shows the reliability qualification summary.

Table 4: Qualification Requirement Summary

Technology	New Process, New Device	Qualified Process, New Device	Qualified Process & Device, New Package	Qualified Process & Device, Package, New Assembly Facility
0.65µm ^a	Table 1, 2, 3	Table 1, 2, 3	Table 3	Table 3
0.35µm ^b	Table 1, 2, 3	Table 1, 2, 3	Table 3	Table 3
0.25µm ^c	Table 1, 2, 3	Table 1, 2, 3	Table 3	Table 3

- a. pASIC1 and pASIC2 Products
- b. pASIC3, QuickRAM, QuickPCI, and QuickFC products
- c. Eclipse, EclipsePlus, and QuickSD products

Failure Rate Calculation

Reliability is the probability that a semiconductor device will perform its specified function in a given environment for a specified period of time. In other words, reliability is quality over time and environmental conditions.

The most frequently used reliability measure for semiconductor devices is the failure rate (λ). The failure rate is obtained by dividing the number of failures observed by the product of the number of devices on test and the interval in hours, usually expressed as percent per thousand hours or failures per billion device hours (FITS). The relationship between failure rate and the chi-square distribution is as follows:

$$\text{Failure Rate} = \lambda = \frac{\chi^2(\alpha, \text{d. f.})}{2t}$$

Where:

λ = failure rate

χ^2 = chi-square function

α = (100 – confidence level) / 100

d.f. = degrees of freedom = $2r + 2$

r = number of failures

t = device hours (# of devices × # of hours × acceleration factor)

In the failure rate calculation, acceleration factors (AF) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. The acceleration factor is calculated using the Arrhenius equation:

$$AF = \exp \left\{ \frac{E_a}{K} \left[\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right] \right\}$$

Where:

AF = Acceleration Factor

E_a = Thermal Activation Energy (0.7eV is assumed and used in the failure rate calculation)

K = Boltzmann's Constant (8.63×10^{-5} eV/K)

T_{use} = use Temperature ($^{\circ}\text{C} + 273$)

T_{stress} = Life Test Stress Temperature ($^{\circ}\text{C} + 273$)

Data Summaries

Table 5 summarises the High Temperature Life Test data.

Table 5: HTOL Summary for QuickLogic Devices

Technology	0.65 μm	0.35 μm	0.25 μm
Failure	9 fails	7 fails	0 fail
Equivalent Device Hrs. @ 55°C	5.50E+08	2.50E+08	6.90E+06
FIT Rate ^a	19.1	33.6	116
MTBF ^b	5.24E+07	2.98E+07	8.62E+06

a. FIT is calculated base on 0.7ev, 60% C.L. and T_j of 55°C.

b. MTBF is calculated as $\text{MTBF} = 10\text{E}+09/\text{FIT rate}$.

Reliability results are summarized in Table 6 to Table 10.

Table 6: HTOL Results

Technology	# of Units Tested	# of Failures
0.65 μm	5124	9 ^a
0.35 μm	1557	7 ^b
0.25 μm	100	0

a. Causes of failures for 0.65 μm technology:

1. due to gate oxide
2. due to a particle
3. and 4. due to metal short
- 5., 6., 7., 8., and 9. due to noise in Vcc supply signal

b. Causes of failures for 0.35 μm technology:

1. and 2. due to incorrect power supply
3. and 4. due to latch up
- 5., 6., and 7. due to incorrect programming Algorithm

Table 7: LTOL Results

Technology	# of Units Tested	# of Failures
0.65 μm	3635	4 ^a
0.35 μm	254	0
0.25 μm	100	0

a. Causes of failures for 0.65 μm technology:

None of the failures were related to the programmed vialink.

1. and 2. due to metal short
3. and 4. due to surge on power supply

The Package Reliability Test results are summarized in **Table 8** through **Table 10**.

Table 8: 0.65 μm Technology

Reliability Test	PLCC		PQFP		TQFP		PBGA	
	# of Units Tested	# of Failures	# of Units Tested	# of Failures	# of Units Tested	# of Failures	# of Units Tested	# of Failures
Temperature Humidity Bias (THB) OR High Accelerated Stress Test (Biased HAST)	482	3 ^a	167	0	150	1 ^b		
Temperature Cycling (TC)	854	1 ^c	1152	4	623	1 ^d	90	0
High Temperature Storage (HTS)	210	0	225	0	135	0		
Pressure Pot OR Unbiased HAST	518	0	225	0	171	0	45	0

- a. The THB failures were due to a particle.
- b. The HAST failure was due to a metal short.
- c. The temp. cycle failures were due to lifted bond.
- d. See footnote c. above.

Table 9: 0.35 μm Technology

Reliability Test	PLCC		PQFP		TQFP		PBGA	
	# of Units Tested	# of Failures	# of Units Tested	# of Failures	# of Units Tested	# of Failures	# of Units Tested	# of Failures
Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning	45 (Biased HAST)	0	50 (THB)	0	45	0	46 (Biased HAST)	0
Temperature Cycling (TC) with Preconditioning	310	0	1791	1 ^a	380	0	477	0
High Temperature Storage (HTS)	45	0	135	0	45	0	45	0
Pressure Pot with Preconditioning OR Unbiased HAST with Preconditioning	155 (Pressure Pot)	0	235 (Pressure Pot)	0	55	0	171	0

- a. The failure was due to Vcc and Gnd short.

Table 10: 0.25 μm Technology

Reliability Test	PQFP		PBGA	
	# of Units Tested	# of Failures	# of Units Tested	# of Failures
Temperature Humidity Bias (THB) with Preconditioning OR High Accelerated Stress Test (Biased HAST) with Preconditioning			45	0
Temperature Cycling (TC) with Preconditioning	46	0	100	0
High Temperature Storage (HTS)			45	0
Pressure Pot with Preconditioning OR Unbiased HAST with Preconditioning	46	0	100 (Pressure Pot)	0

Contact Information

Telephone: 408 990 4000 (US)
 416 497 8884 (Canada)
 44 1932 57 9011 (Europe)
 49 89 930 86 170 (Germany)
 852 8106 9091 (Asia)
 81 45 470 5525 (Japan)

E-mail: info@quicklogic.com
 Support: support@quicklogic.com
 Web site: <http://www.quicklogic.com/>

Revision History

Table 11: Revision History

Revision	Date	Originator and Comments
Rev. A	August 2002	Paul Micallef and Brian Faith

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