Lattice Semiconductor

Product Reliability Report

ORCA, ispLSI, ispGDX, ispMACH, GAL Products

First Half 2002

Summary Version

INTRODUCTION

Oregon-based Lattice Semiconductor Corporation designs, develops and markets the broadest range of high-performance ISP™ programmable logic devices (PLDs), Field Programmable Gate Arrays (FPGAs) and Field Programmable System Chip (FPSC) devices. Lattice offers total solutions for today's system designs by delivering the most innovative programmable silicon products that embody leading-edge system expertise. Lattice products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEM customers in the fields of communication, computing, computer peripherals, instrumentation, industrial controls and military systems. Lattice Semiconductor was founded in 1983 and is based in Hillsboro, Oregon.

This report summarizes the reliability testing results for Lattice Semiconductor products as of July 2002.

LATTICE RELIABILITY

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs. All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Policy (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from the Lattice Semiconductor sales office.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Tables 1 and 2. Ongoing production is monitored based on the requirements outlined in Tables 3 and 4. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

Table 1: STANDARD QUALIFICATION TESTING

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005, JESD22-A108-A GAL Products ispLSI Products MACH Products	125° C, 5.5/3.6V/2.5V Vcc, 168, 500, 1000, 2000 hours. Preconditioned with 100 read/write cycles Preconditioned with 1000 read/write cycles Preconditioned with 30 read/write cycles	77/lot 2 lots	Design, Fab Process Package Qualification
High Temp Data Retention	Lattice Procedure # 87-101925, JESD22-A103-B	Vcc=5.25/3.6V, 150° C, 2K hours, Devices are preconditioned with 100 read/write cycles	77/lot 2 lots	Design, Fab Process, Package Qualification
Temperature Cycling	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Cond. B JESD22-A104-B	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45/lot 2 lots	Design, Fab Process, Package Qualification
Endurance - Program/Erase Cycling	Lattice Procedure, # 70-101569 JESD22-A117	Program/Erase ispLSI devices to 100,000 cycles GAL devices to 10,000 cycles	10/lot 2 lots	Design, Fab Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD- 883, Method 3015.7 JEDS22-A114-A	Supply voltage applied during measurement=5V/3.6 V/2.5V HBM minimum 2000V	3 parts/lot 2 lots	Design, Fab Process, Package Qualification
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101-A	Charged Device model (CDM) sweep to 1500 volts	3 parts/lot 2 lots	Design, Fab Process, Package Qualification
Latch Up Resistance	Lattice Procedure # 70-101570, JESD78	±200ma on I/O's, Vcc +50% on Power Supplies	2 parts/lot 2 lots typical	Design, Fab Process, Package Qual
Moisture Resistance 85/85 Biased HAST	Lattice Procedure # 70-101571, JESD22-A101-B JESD22-A110-B	Vcc = 5.0/3.3V/2.5V biased 85° C, 85% Relative Humidity, 1000 hours Vcc= 5.0/3.3V biased 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45/package family	Design, Fab Process Package Qualification Plastic Pkg. only

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE	PERFORMED ON
Solderability	Lattice Procedure # 70-100212, MIL-STD-883E, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245° C + 5° C	3 devices 22 leads/device	Package Qualification
Lead Integrity	Lattice Procedure # 70-100192, MIL-STD-883E, Method 2004	PDIP, CDIP packages	3 devices	PDIP, CDIP package Qualification
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Unbiased HAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45/package family	Fab Process, Package Qualification Plastic Pkg. only
Surface Mount Pre-conditioning	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020B JESD-A113-B CPLD - MSL 3 SPLD - MSL 1	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles. 168hr. 85/85 Soak 3 SMT simulation cycles.	100 devices/ Package Family	Plastic Packages only

Table 2: ADDITIONAL QUALIFICATION TESTS

(For Hermetic/Military Products Only) Testing is done 1 time/year/pkg. type

TEST	STD	TEST CONDITIONS	SAMPLE SIZE	PERFORMED ON
Wire Bond Strength Bond Strength Group B	Lattice Procedure # 70-100220 MIL-STD- 883, Method 2011, Condition D	6 gr. min. for 1.25 mil gold wire 3 grs min. for 1.25 mil AL wire	15 pieces per pkg. per year 15 leads	Design, Fab Process, Package Qualification
Thermal Shock	Lattice Procedure # 70-100612, MIL-STD- 883, Method 1011	Measure all dimensions listed on the case outline and compare with case outline limits. Note any failed dimensions on the lot traveler. 4/30/97	15 pieces per pkg. per year	Hermetic packages only
Vibration	Lattice Procedure # 70-100613, MIL-STD- 883 Method 2007.2	Leakage, visual, functional 20-2000 Hz for 10 min. 20q's for 4 min. in 3 planes, limit of .06" (24 mm) of movement	15 leads 15 pieces per pkg. per year	Hermetic packages only
Salt Water Spray Salt Atmosphere	Lattice Procedure # 70-100614, MIL-STD- 883 Method 1009.8	Less than 5% of metal surfaces covered with corrosion	15 pieces per pkg. per year	Hermetic packages only
Constant Acceleration Centrifuge	Lattice Procedure # 70-100611, MIL-STD- 883 Method 2001.2	Acceleration = 30kg-m/sec. Leakage, visual, functional	15 pieces per pkg. per year	Hermetic packages only Design, Fab Process, Package Qualification
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	All package types
Resistance to Solvents Mark Permanency	Lattice Procedure # 70-101102, MIL-STD-883, Method 2015	Mark legible in one of 4 solutions. Monitor if mark is degrading.	4 units 3 lots of each pkg.	All package types
Mechanical Shock	Lattice Procedure # 70-100613, MIL-STD- 883, Method 2002 Condition B	Leakage, visual, functional 1500gms for 5ms.	15 pieces per pkg. per year	Hermetic packages only

Table 3: RELIABILITY MONITOR TESTING

TEST	STD	TEST CONDITIONS	SAMPLE SIZE	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 70-101566, MIL-STD-883, Method 1005, JESD22-A108-A GAL Products ispLSI Products MACH Products	125° C, 5.5/3.6 Volts, 168, 1000 hours. Preconditioned with 100 read/write cycles Preconditioned with 1000 read/write cycles Preconditioned with 30 read/write cycles	Early Life 200 devices/ Process Technology/ Month Inherent Life 100 devices/ Process Technology/ Month	Released Process Technologies

Table 4: QA PACKAGE MONITOR TESTING

TEST	STD	TEST CONDITIONS	SAMPLE SIZE	PERFORMED ON
Resistance to Solvents	Lattice Procedure # 70-101102, MIL-STD-883, Method 2015	Mark legible in one of 4 solutions. Monitor if mark is degrading.	10 units/ Package family/ Assembly facility /month	All package
Lead Integrity	Lattice Procedure # 70-100192, MIL-STD-883E, Method 2004	PDIP, CDIP packages	5 devices / Package family/ Assembly facility /month	PDIP packages only
Solderability	Lattice Procedure # 70-100212, MIL-STD-883E, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245°C+5°C	22 leads 3 devices/ Package family/ Assembly facility /month	All packages
Scanning Acoustic Tomography	Lattice Procedure # 70-103772 IPC/JEDEC J-STD-035		10 units/ Package family/ Assembly facility /month	All plastic packages

TEST METHODS

HIGH TEMPERATURE OPERATING LIFE (HTOL)

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. A pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at maximum operating voltage and 125°C. Prior to operating life testing, all In-System Programmable High Density Logic devices receive a number of program and erase cycles.

HIGH TEMPERATURE DATA RETENTION

The High Temperature Data Retention test measures the Electrically Erasable cell (E^2 cell) reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the E^2 cell reliability is determined by monitoring the cell margin after biased static operation at 150°C or 125°C based on technology. All cells in all arrays are life tested in both programmed and erased states.

TEMPERATURE CYCLING

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling of between -55°C and +125°C in an air environment consistent with JEDEC “Temperature Cycling” standard JESD22-A104-A Condition B.

ENDURANCE PROGRAM/ERASE CYCLING

Endurance testing measures the durability of the device through programming and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array.

ESD CHARACTERIZATION

HUMAN BODY MODEL

Human Body Model ESD testing consists of applying positive and negative pulses to individual pins with respect to various combinations of the remaining pins. Lattice

Semiconductor's ESD Characterization Procedure, document #70-100844, is based upon the JEDEC Standard EIA/JESD22-A114-A, “Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)”. Lattice Semiconductor's ESD procedure differs from the JEDEC procedure in that it is a characterization procedure rather than a classification procedure and, as such, checks and reports each test condition separately. Lattice Semiconductor employs 1 pulse with a 0.5 second delay between pulses. A failure is defined as an input or output leakage which exceeds 10µA with $V_{IN}/V_{OUT} = 0$ to maximum Vcc.

All Lattice Semiconductor products meet at least 2000V with respect to Human Body Model ESD testing.

CHARGED DEVICE MODEL

The Charged Device Model (CDM) ESD test simulates the transfer effect of electrostatic charge accumulated on the device due to improper grounding. For example, a device may become charged when sliding down the feeder in an automated assembler. If the charged device contacts the insertion head or some other conductive surface, a rapid discharge may occur from the device to the metal object.

Lattice Semiconductor utilizes the CDM socketed discharge method. This model simulates a charged IC coming into contact with a low impedance conductive surface. The device under test is placed in a socket, charged from a high-voltage source, and then discharged. Lattice Semiconductor employs 3 pulses with a 1 second delay between pulses. A failure is defined as an input or output leakage which exceeds +/- 10µA with $V_{IN}/V_{OUT} = 0$ to maximum Vcc.

All Lattice Semiconductor products meet at least 1000V with respect to Charged Device Model ESD testing.

LATCH-UP RESISTANCE

Latch-up testing consists of stressing all input and I/O pins in an effort to turn-on any parasitic bipolar (PNPN) structures. The latch-up condition is characterized by runaway supply current with possible damage to the part occurring if the latch-up condition is maintained.

MOISTURE RESISTANCE TESTING
TEMPERATURE HUMIDITY BIASED (85°C/85% RH)

85°C/85% relative humidity with Vcc bias and alternate pin biasing is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package.

BIASED HAST

Biased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Biased HAST conditions are 130°C, 85% relative humidity, and 2 atmospheres of pressure.

UNBIASED HAST

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface which can cause chemical corrosion. Unbiased HAST conditions are 130°C, 85% relative humidity, and 2 atmospheres of pressure.

SURFACE MOUNT PRECONDITIONING TESTING

The Surface Mount Preconditioning Test is used to model the surface mount assembly conditions during component solder processing.

All Lattice High Density Products are preconditioned consistent with JEDEC JESD22-A113-B "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing" Moisture Sensitivity Level 3 (MSL 3). CPLD devices are subjected to 10 temperature cycles between -55°C and +125°C in an air environment, a bake for 24 hours at 125°C to establish a baseline for the package moisture content, a controlled moisture soak for 192 hours at 30°C/60% relative humidity, followed by 3 thermal cycles through a reflow simulation temperature profile appropriate to the package body size.

All GAL (SPLD) Products are preconditioned consistent with JEDEC Moisture Sensitivity Level 1 (MSL 1) thermal package moisture sensitivity and dry-pack storage requirements. GAL devices are subjected to 10 temperature cycles between -55°C and +125°C in an air environment, a bake for 24 hours at 125°C establish a baseline for the package moisture content, a controlled moisture soak for 168 hours at 85°C/85% relative humidity, followed by 3 thermal cycles through a reflow simulation temperature profile.

3.0 PRODUCT/PROCESS TECHNOLOGY INDEX

BY PRODUCT

FPGA/FPSC (sorted alphabetically)

<u>BY PRODUCT</u>

<u>CPLDs</u> (sorted alphabetically)

ispGDX80A . . . . UltraMOS VI Process
ispGDX80VA . . . . UltraMOS 8 Process
ispGDX120A . . . . UltraMOS VI Process
ispGDX160 . . . . UltraMOS VI Process
ispGDX160A . . . . UltraMOS VI Process
ispGDX160V . . . . UltraMOS VI Process
ispGDX160VA . . . . UltraMOS 8 Process
ispGDX240VA . . . . UltraMOS 8 Process
ispLSI 1016 . . . . UltraMOS IV Process
ispLSI 1016E . . . . UltraMOS V Process
ispLSI 1016EA . . . . UltraMOS VI Process
ispLSI 1024 . . . . UltraMOS IV Process
ispLSI 1024EA . . . . UltraMOS VI Process
ispLSI 1032 . . . . UltraMOS IV Process
ispLSI 1032E . . . . UltraMOS VI Process
ispLSI 1032EA . . . . UltraMOS VI Process
ispLSI 1048 . . . . UltraMOS IV Process
ispLSI 1048E . . . . UltraMOS VI Process
ispLSI 1048EA . . . . UltraMOS VI Process
ispLSI 1048C . . . . UltraMOS IV Process
ispLSI 2032 . . . . UltraMOS VI Process
ispLSI 2064 . . . . UltraMOS V Process
ispLSI 2096 . . . . UltraMOS V Process
ispLSI 2128 . . . . UltraMOS V Process
ispLSI 2032A . . . . UltraMOS VI Process
ispLSI 2064A . . . . UltraMOS VI Process
ispLSI 2096A . . . . UltraMOS VI Process
ispLSI 2128A . . . . UltraMOS VI Process
ispLSI 2032E . . . . UltraMOS VI Process
ispLSI 2064E . . . . UltraMOS VI Process
ispLSI 2096E . . . . UltraMOS VI Process
ispLSI 2128E . . . . UltraMOS VI Process
ispLSI 2032V . . . . UltraMOS V Process
ispLSI 2064V . . . . UltraMOS V Process
ispLSI 2096V . . . . UltraMOS V Process
ispLSI 2128V . . . . UltraMOS V Process
ispLSI 2032VE . . . . UltraMOS VI Process
ispLSI 2032VE date code “D”. . . . . UltraMOS 8 Process
ispLSI 2064VE . . . . UltraMOS VI Process

<u>BY PRODUCT (CONT’D.)</u>

ispLSI 2064VE date code “D”. . . . . UltraMOS 8 Process

ispLSI 2096VE . . . . UltraMOS VI Process
ispLSI 2096VE date code “D”. . . . . UltraMOS 8 Process
ispLSI 2128VE . . . . UltraMOS VI Process
ispLSI 2128VE date code “D”. . . . . UltraMOS 8 Process
ispLSI 2192VE . . . . UltraMOS VI Process
ispLSI 2192VE date code “D”. . . . . UltraMOS 8 Process
ispLSI 2032VL . . . . UltraMOS VI Process
ispLSI 2064VL . . . . UltraMOS VI Process
ispLSI 2096VL . . . . UltraMOS VI Process
ispLSI 2128VL . . . . UltraMOS VI Process
ispLSI 2192VL . . . . UltraMOS VI Process
ispLSI 3160 . . . . UltraMOS VI Process
ispLSI 3192 . . . . UltraMOS V Process
ispLSI 3256A . . . . UltraMOS VI Process
ispLSI 3256E . . . . UltraMOS VI Process
ispLSI 3320 . . . . UltraMOS VI Process
ispLSI 3348 . . . . UltraMOS VI Process
ispLSI 5128VE . . . . UltraMOS 8 Process
ispLSI 5256VA . . . . UltraMOS VI Process
ispLSI 5256VE . . . . UltraMOS 8 Process
ispLSI 5384VA . . . . UltraMOS VI Process
ispLSI 5384VE . . . . UltraMOS 8 Process
ispLSI 5512VA . . . . UltraMOS VI Process
ispLSI 5512VE . . . . UltraMOS 8 Process
ispLSI 8840 . . . . UltraMOS VI Process
ispLSI 8600V . . . . UltraMOS VI Process
ispLSI 8840V . . . . UltraMOS VI Process
ispLSI 81080V . . . . UltraMOS VI Process

BY PRODUCT (CONT'D.)

MACH (sorted alphabetically)

M4-128	. . . .	EE7 Process
M4-192	. . . .	EE7 Process
M4-256	. . . .	EE7 Process
M4-32	. . . .	EE7 Process
M4-64	. . . .	EE7 Process
M4-96	. . . .	EE7 Process
M4A3-32	. . . .	EE8 Process
M4A3-64	. . . .	EE8 Process
M4A3-96	. . . .	EE8 Process
M4A3-128	. . . .	EE8 Process
M4A3-192	. . . .	EE8 Process
M4A3-256	. . . .	EE8 Process
M4A3-384	. . . .	EE8 Process
M4A3-512	. . . .	EE8 Process
M4A5-32	. . . .	EE8 Process
M4A5-64	. . . .	EE8 Process
M4A5-96	. . . .	EE8 Process
M4A5-128	. . . .	EE8 Process
M4A5-192	. . . .	EE8 Process
M4A5-256	. . . .	EE8 Process
M4LV-128	. . . .	EE7 Process
M4LV-192	. . . .	EE7 Process
M4LV-256	. . . .	EE7 Process
M4LV-32	. . . .	EE7 Process
M4LV-64	. . . .	EE7 Process
M4LV-96	. . . .	EE7 Process
M5-128	. . . .	EE65 Process
M5-128/1	. . . .	EE8 Process
M5-192	. . . .	EE65 Process
M5-192/1	. . . .	EE8 Process
M5-256	. . . .	EE65 Process
M5-256/1	. . . .	EE8 Process
M5-320	. . . .	EE7 Process
M5-320 date code "L"	. . . .	EE8 Process
M5-384	. . . .	EE7 Process
M5-384 date code "L"	. . . .	EE8 Process
M5-512	. . . .	EE7 Process
M5-512 date code "L"	. . . .	EE8 Process

BY PRODUCT (CONT'D.)

M5LV-128	. . . .	EE7 Process
M5LV-128 date code "L"	. . . .	EE8 Process
M5LV-256	. . . .	EE7 Process
M5LV-256 date code "L"	. . . .	EE8 Process
M5LV-320	. . . .	EE7 Process
M5LV-320 date code "L"	. . . .	EE8 Process
M5LV-384	. . . .	EE7 Process
M5LV-384 date code "L"	. . . .	EE8 Process
M5LV-512	. . . .	EE7 Process
M5LV-512 date code "L"	. . . .	EE8 Process

GALs (sorted alphabetically)

ispGDS14 . . . . UltraMOS IV Process
ispGDS18 . . . . UltraMOS IV Process
ispGDS22 . . . . UltraMOS IV Process
ispGAL22LV10 . . . . UltraMOS VI Process
ispGAL22V10C . . . . UltraMOS V Process
GAL16LV8C . . . . UltraMOS V Process
GAL16LV8D . . . . UltraMOS VI Process
GAL16LV8ZD . . . . UltraMOS IV Process
GAL16V8D . . . . UltraMOS VI Process
GAL16V8Z . . . . UltraMOS IV Process
GAL16V8ZD . . . . UltraMOS IV Process
GAL16VP8B . . . . UltraMOS IV Process
GAL18V10B . . . . UltraMOS IV Process
GAL20LV8D . . . . UltraMOS VI Process
GAL20LV8ZD . . . . UltraMOS IV Process
GAL20RA10B . . . . UltraMOS IV Process
GAL20V8B . . . . UltraMOS IV Process
GAL20V8C . . . . UltraMOS V Process
GAL20V8Z . . . . UltraMOS IV Process
GAL20V8ZD . . . . UltraMOS IV Process
GAL20VP8B . . . . UltraMOS IV Process
GAL20XV8B . . . . UltraMOS IV Process
GAL22LV10C . . . . UltraMOS V Process
GAL22LV10D . . . . UltraMOS VI Process
GAL22LV10Z . . . . UltraMOS IV Process
GAL22LV10ZD . . . . UltraMOS IV Process
GAL22V10D . . . . UltraMOS VI Process
GAL26CLV12D . . . . UltraMOS VI Process
GAL26CV12B . . . . UltraMOS IV Process
GAL26CV12C . . . . UltraMOS V Process
GAL6001B . . . . UltraMOS IV Process
GAL6002B . . . . UltraMOS IV Process

BY TECHNOLOGY

COM 1 – 0.25 CMOS

OR2T15B
OR2T40B
OR3L165B
OR3L225B
ORT4622
OR3LP26B

0.3 CMOS

OR2T15A
OR2T26A
OR2T40A
OR3T20
OR3T30
OR3T55
OR3T80
OR3T125
OR3TP12

0.35 CMOS

OR2C04A
OR2C06A
OR2C08A
OR2C10A
OR2C12A
OR2C15A
OR2C26A
OR2C40A
OR3C55
OR3C80
OR2T04A
OR2T06A
OR2T08A
OR2T10A

ULTRAMOS 8 PROCESS

CPLDs

ispLSI 5000VE Family
ispGDXVA Family
ispLSI 2000VE Family

ULTRAMOS VI PROCESS

CPLDs

ispLSI 1000EA Family
ispLSI 2032
ispLSI 2000A Family
ispLSI 2000E Family
ispLSI 2000VE Family
ispLSI 2000VL Family
ispLSI 5000V/VA Family
ispGDX Family
ispGDXV Family
ispLSI 8000 Family
ispLSI 8000V Family
ispLSI 1000E Family
ispLSI 3160
ispLSI 3256A
ispLSI 3256E
ispLSI 3320
ispLSI 3448

GAL Devices

GAL16V8D
GAL16LV8D
GAL20LV8D
GAL22V10D
GAL22LV10D
ispGAL22LV10
GAL26CLV12D
GAL26CV12D

UltraMOS V PROCESS

CPLDs

ispLSI 2064
ispLSI 2096
ispLSI 2128
ispLSI 2000V Family
ispLSI 3192

GAL Devices

GAL16LV8C
GAL22LV10C
GAL20V8C
GAL26CV12C
ispGAL22V10C

BY TECHNOLOGY (CONT'D.)

UltraMOS IV PROCESS

CPLDs
ispLSI 1000 Family

GAL Devices
GAL16LV8ZD
GAL16V8Z
GAL16V8ZD
GAL16VP8B
GAL18V10B
GAL20LV8ZD
GAL20RA10B
GAL20V8B
GAL20V8Z
GAL20V8ZD
GAL20VP8B
GAL20XV10B
GAL22LV10Z
GAL22LV10ZD
GAL6001B
GAL6002B
ispGDS14
ispGDS18
ispGDS22

BY TECHNOLOGY (CONT'D.)

EE8 PROCESS

CPLDs
M4A3-32
M4A3-64
M4A3-96
M4A3-128
M4A3-192
M4A3-256
M4A3-384
M4A3-512

M4A5-32
M4A5-64
M4A5-96
M4A5-128
M4A5-192
M4A5-256

M5LV-128 date code "L"
M5LV-256 date code "L"
M5LV-320 date code "L"
M5LV-384 date code "L"
M5LV-512 date code "L"

M5-128/1
M5-192/1
M5-256/1
M5-320 date code "L"
M5-384 date code "L"
M5-512 date code "L"

BY TECHNOLOGY (CONT'D.)

EE7 PROCESS

CPLDs
M4-128
M4-192
M4-256
M4-32
M4-64
M4-96
M4LV-128
M4LV-192
M4LV-256
M4LV-32
M4LV-64
M4LV-96
M5-320
M5-384
M5-512
M5LV-128
M5LV-256
M5LV-320
M5LV-384
M5LV-512

EE65 PROCESS

CPLDs
M5-128
M5-192
M5-256

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Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT. These FIT rates are adjusted to an ambient temperature of 55°C with a 60% upper confidence level.

The results of the present Lattice Semiconductor technology families are summarized in the table below.

Technology	HTOL - FIT rate Failures/device hours	Data Retention Failures/device hours	ESD HBM	 CDM
UltraMOS 8	16.8 FIT 1 Failures/ 5,070,168 device hours	0 Failures/ 6,146,000 device hours	at least 2000V	at least 1000V
UltraMOS VI	7.4 FIT 4 Failures/ 24,462,100 device hours	6 Failures/ 25,725,840 device hours	at least 2000V	at least 1000V
UltraMOS V	39.8 FIT 8 Failures/ 10,834,504 device hours	11 Failures/ 15,885,836 device hours	at least 2000V	at least 1000V
UltraMOS IV	17.3 FIT 4 Failures/ 10,454,000 device hours	6 Failures/ 27,436,504 device hours	at least 2000V	at least 1000V
EE6.5	51.4 FIT 5 Failures/ 4,165,496 device hours	0 Failure/ 2,500,000 device hours	at least 2000V	at least 1000V

Technology	HTOL - FIT rate Failures/device hours	Data Retention Failures/device hours	ESD HBM	 CDM
EE7	18.9 FIT 0 Failure/ 2,667,533 device hours	0 Failure/ 3,256,000 device hours	at least 2000V	at least 1000V
EE8	40.9 FIT 8 Failure/ 9,552,069 device hours	0 Failure/ 3,088,707 device hours	at least 2000V	at least 1000V
EE9	22.7 FIT 1 Failure/ 2,961,516 device hours	1 Failure/ 1,379,428 device hours	at least 2000V	at least 1000V
0.35 CMOS - 5 VOLT	63.0 FIT 4 Failure/ 1,068,000 device hours	Not Applicable	at least 2000V	at least 1000V
0.35 CMOS - 3 VOLT	32.6 FIT 2 Failure/ 1,224,000 device hours	Not Applicable	at least 2000V	at least 1000V
0.30 CMOS - 5 VOLT	79 FIT 1 Failure/ 330,000 device hours	Not Applicable	at least 2000V	at least 1000V
0.30 CMOS - 3 VOLT	30 FIT 0 Failure/ 396,500 device hours	Not Applicable	at least 2000V	at least 1000V
COM 1 0.25 CMOS - 3 VOLT	8.8 FIT 0 Failure/ 1,342,000 device hours	Not Applicable	at least 2000V	at least 1000V

Detailed data for the testing described in this report is available on request.