TEMPORALLY REDUNDANT LATCH FOR PREVENTING SINGLE EVENT DISRUPTIONS IN SEQUENTIAL INTEGRATED CIRCUITS

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TABLE OF CONTENTS

I. Introduction ... 1
II. Background ... 2
III. An Emerging SEU Mechanism ... 7
IV. Conventional Hardening to SETs ... 14
V. ASIC Design Synthesis ... 15
VI. Temporal Sampling Latch ... 16
A. Latch Construction ... 16
B. Clocking Scheme ... 18
C. Circuit Operation ... 18
D. Elimination of Upsets ... 20
E. Clock Generation ... 24
F. Fast Mode Operation ... 27
G. Speed Tradeoff ... 27
H. Size Tradeoff ... 29
I. Scan Chain Testing ... 30
J. Static Data Storage ... 32
K. Miscellaneous Considerations ... 32
L. Connection to Design Synthesis ... 34
VII. Multiple Bit Heavy Ion Strikes ... 36
A. Type 1 ... 36
B. Type 2 ... 38
C. Type 3 ... 38
VIII. Summary ... 39
IX. References ... 40

LIST OF FIGURES

1. Charge Collection due to an Ion Passing through a Junction. 4
2. Critical Transient Width vs Feature Size for Unattenuated Propagation. 8
3. Typical Sequential Circuit Topology. 10
4. Temporal Relationship for Latching a Data SET as an Error. 11
5. Temporal Relationship for a Clock SET to Cause an Error. 12
6. Temporal Sampling Latch with Sample and Release Stages. 17
7. Temporal Latch Control Clocks Derived from Master Clock. 19
8. Sample Node Values for One Computation Cycle. 21
9. Simple (Non-SEU Immune) Control Clock Generator Circuit. 25
10. Final SEU Immune Control Clock Generator Circuit. 26
11. Circuit to Select Between SEU Immune and Fast Modes of Operation. 28
12. Scan Chain Testing Approach for the Error Immune Temporal Latch. 31
13. Shift Register Configuration to Self Scrub Errors for Statis Data Storage. 33

I. INTRODUCTION

As the microelectronics industry has advanced, integrated circuit (IC) designs have experienced dramatic increases in both density and speed. The reason for these increases is largely due to the decreasing feature sizes with which these devices can be manufactured. (By the feature size of a given manufacturing technology, we refer to the minimum gate length of a CMOS transistor in that technology.) These advances are not without serious implications for microelectronics used in space applications where ICs are subjected to hostile environments that result in total ionizing dose effects primarily due interactions with trapped electrons and protons as well as single event effects (SEE) primarily do to interactions with cosmic rays (high energy heavy ions), high energy protons, and high energy neutrons. Of these effects, SEUs (single event upsets) represent the radiation-induced hazard most difficult to avoid in spaceborne microelectronics systems.

In this report we consider bulk CMOS (complimentary metal oxide silicon) device technologies and their response to the cosmic ray environment of space. (We are not addressing here any specific total-dose issues.) The threefold purpose of this report is to:

1. clarify the impact that shrinking device sizes will have on single event upsets in spaceborne microelectronics due to the cosmic ray environment,

2. explain how single event transients (SETs) in the combinatorial logic of a circuit will, in the near future, become important in spaceborne systems as we begin using ICs having device feature sizes smaller than 0.35 micron, and

3. propose a new and unique circuit design methodology that can, with minor tradeoffs, totally eliminate SEUs and even multiple bit upsets (MBUs) from sequential circuit designs.

We will first provide some background to the reader in the area of SEU mechanisms and describe their implications for present day spaceborne microelectronics. We will then discuss an emerging SEU mechanism that will begin to impact the operation space systems fabricated in the next one or two generations of technology. Problems with using conventional approaches to harden future generations of ICs will also be discussed, particularly with regard to incompatibilities of these approaches with automated design synthesis and layout tools.

The remainder of this paper will then present and describe a new temporal sampling latch approach that is inherently immune at any technology feature size to both present day upset mechanisms and to emerging upset mechanisms. The new approach not only addresses upsets in latches, but also addresses upsets caused by transients in combinatorial logic, global clock signals, and global control signals. The new approach, when applied with special latches and a lower clock frequency can also eliminate multiple bit upsets in sequential circuit designs. Finally, since the resulting circuit is inherently SEU hard, the new approach lends itself naturally for use with automated design tools.

II. BACKGROUND

A number of scaling models have been used in the industry over the past few years [1]. These include lateral scaling where only the gate length is scaled, constant voltage scaling where the supply voltage V_{DD} is kept constant, and constant field scaling where V_{DD} is decreased as the gate oxide thickness is decreased to maintain a constant electric field in transistors. As features sizes in non-radiation hardened commercial fabrications have shrunk below 1.0 micron (several years ago) to 0.18 microns (currently) and continue to shrink to a projected 0.05 microns (by the year 2012) [2], the constant field scaling model has proven to be the most practical since it avoids several deleterious effects of high fields (gate oxide breakdown and hot electrons).

For constant field scaling, as all physical device dimensions (such as gate length L, gate width W, and gate oxide thickness T_{OX}) are reduced, the supply voltage V_{DD} and the threshold voltage V_{TH} are also reduced proportionately. This results in proportionately lower drain current (I), proportionately lower load capacitance (C), and proportionately lower circuit gate delay ($C*V_{DD}/I$). The lower transistor current for constant field scaling also means that metallization current densities (responsible for electromigration) increase less rapidly than for constant voltage scaling for which transistor current remains constant. Also, for low power systems, constant field scaling (in which V_{DD} scales proportionately) is the only viable alternative since it results in substantially lower (by the square of the scaling) power dissipation.

To understand the implications that scaling has on the single event response of microelectronics we will first review the basic concepts of energy loss, charge collection, and upset due to a cosmic ray striking a junction in an IC device. This will be brief and qualitative. Many good summaries exist [3, 4, 5] that review these concepts in more detail.

When an energetic ion passes through any material it loses energy through interactions with the material. The energy loss is primarily due to the interactions of the ion with the bound electrons in the material, causing an ionization of the material and the formation of a dense track of electron-hole pairs. The rate at which the ion loses energy is historically termed the stopping power (dE/dx). The incremental energy dE is usually measured in units of MeV while the material thickness is usually measured as a mass thickness in units of mg/cm^2. The radiation effects community has subsequently adopted the term LET (linear energy transfer) for the stopping power and, to be consistent, that is the term we shall use.

In silicon, 3.6 eV of energy is needed to create a single electron-hole pair. From the density of silicon (2.42 gm/cm^3) we see that a 1 micron thickness converts to a mass thickness of 0.242 mg/cm^2. Also one electron charge equals 1.60×10^{-7} pico-Coulomb (pC). Therefore in silicon, the amount of electron-hole pairs dQ along a track of length L for an ionizing particle having a stopping power LET is given by:

$$dQ \quad (pC) \quad = \quad 0.011 * L\ (microns) * LET\ (MeV - cm^2 / mg)$$

Thus an ion with an LET of 100 Mev-cm^2/mg leaves approximately 1 pC of electron-hole pairs along each micron of its track.

In bulk silicon these electron-hole pairs are of no consequence since they will eventually recombine. In the presence of electric fields, however, the electron-hole pairs will be quickly separated as they drift in opposite directions in the field and be quickly collected by whatever voltage sources are responsible for the field. In bulk CMOS ICs, such electric fields are present across every pn junction in the device. Each and every circuit signal node in the IC is typically isolated from V_{DD} by one or more such junctions (PMOS transistor drains) and isolated from ground (V_{SS}) by one or more such junctions (NMOS transistor drains).

Figure 1 illustrates the effect of an ion passing through an NMOS drain junction on an IC. We show an *n+* NMOS drain diffusion formed in a *p-* epitaxial (epi) layer on a *p+* substrate. The illustrated junction isolates a circuit node at positive voltage (+V) relative to the substrate (V_{SS}).

The ion produces a dense track of electron-hole pairs that behave much like a conductive plasma which perturbs the potential contours forming a funnel region. A prompt component of current is observed at the circuit signal node as the electric field in the junction and funnel regions separate the electron and hole free carriers. For the geometry of Figure 1, electrons are collected by the circuit node and holes are collected by the substrate node resulting in a negative current pulse on the NMOS diffusion node which tends to discharge the signal voltage. This prompt current pulse is short-lived, lasting on the order of only 100 to 200 picoseconds. A delayed current component is produced by diffusion of the electrons and holes from regions where the electric field is zero. These charges may, if they do not recombine, eventually reach a field region where they are collected. This delayed component may last as long as several hundred nanoseconds. Little charge is collected from the *p+* substrate region since the recombination rate is high due to the high doping concentration. If the signal voltage on an NMOS drain is zero, the electric fields will be essentially zero and no appreciable charge collection will occur.

Similar processes occur in the vicinity of PMOS drain diffusions formed in n-wells biased to V_{DD}. In this case electric fields will be present and charge will be collected by the PMOS drain if the signal voltage is at zero volts. The collection depth for this case will be less (approximately one half the well depth) since the well-substrate junction is always reverse biased and will also collect charge.

High energy protons and neutrons are also known to produce similar effects indirectly through nuclear reactions within the silicon. In these cases, a heavy ion recoil reaction byproduct passes through a junction and produces a similar charge collection current pulse. In space, high energy protons primarily originate from the trapped protons radiation belts and from solar flares. For high-altitude aircraft, both high energy neutrons and protons are encountered as reaction byproducts found in cosmic ray showers formed when an energetic heavy ion from space undergoes a nuclear reaction in the atmosphere.

The prompt component of current described above has been responsible for SEUs observed in spaceborne circuits, typically static latches and SRAMs (static random access memories), over the last 10-15 years. The effect that this current has on the circuit depends on the response of the circuit to the charge collected on the signal node. Basically, the capacitance

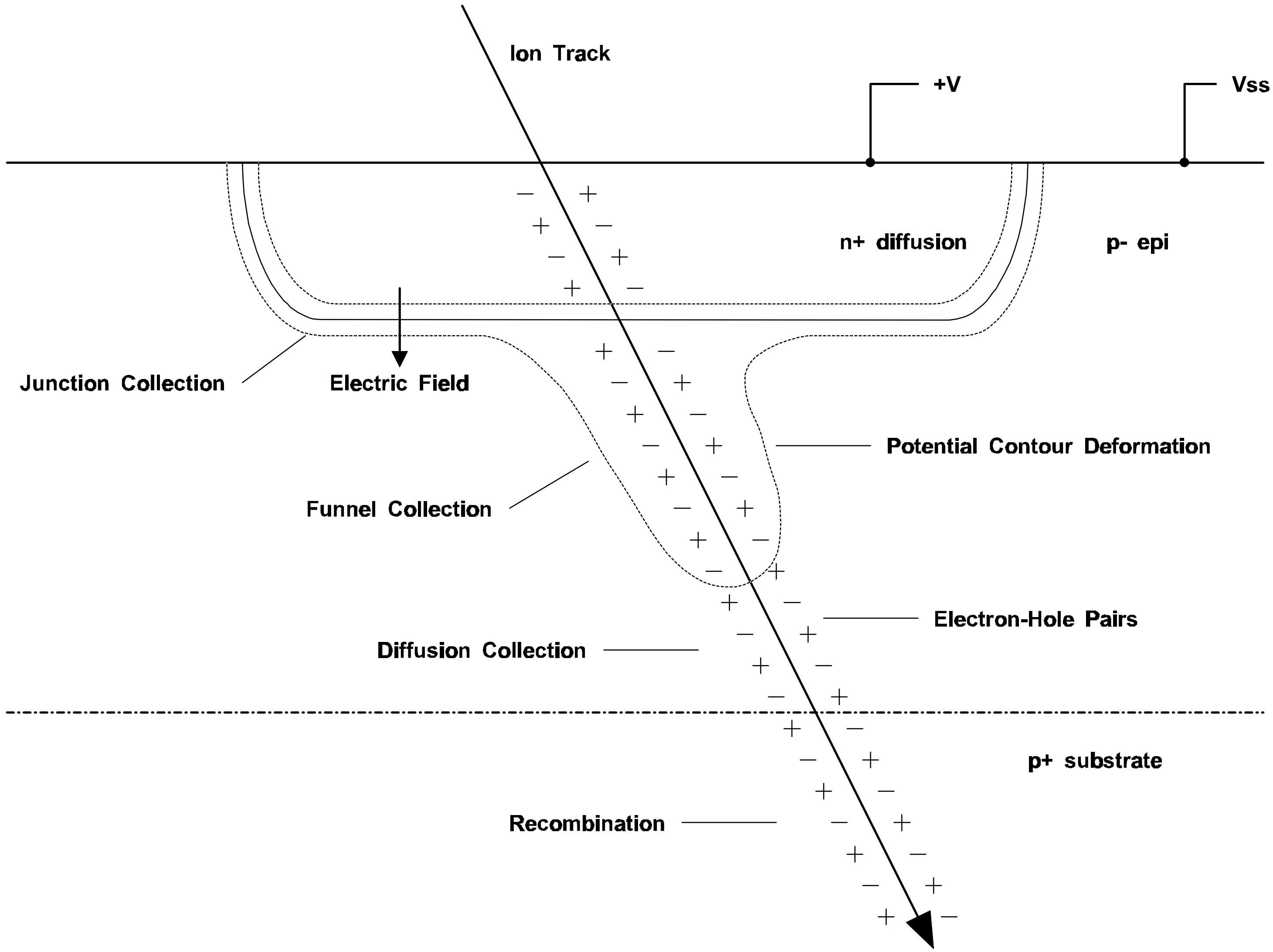

Figure 1. Charge Collection Due to an Ion Passing Through a Junction.

of the signal node will (to first order) determine how large a voltage swing dV will result from the collection of a charge dQ according to dV=dQ/C. (This is exact only in the approximation that the circuit is too slow to dissipate the charge in several hundreds of picoseconds.) High drive transistors will mitigate this effect since they will more quickly dissipate the collected charge. Also, and most importantly for latches and SRAMs, positive gain feedback loops will cause a data bit flip once the collected charge reaches a critical value (Qcrit) sufficient to drive a node voltage past the switching voltage.

These charge collection and circuit response discussions have been included only for background and are admittedly oversimplified. More detailed discussions of these effects, and SRAM circuit response in particular, can be found in [6].

Spaceborne microelectronics typically lag behind their commercial counterparts by one or two generations because of the more complicated fabrication steps needed to achieve the total-dose hardening requirements of space. Radiation-hardened ICs are presently being fabricated in 0.8 micron to 0.7 micron feature sizes. SEU in static latches and SRAMs became an important issue once feature sizes dropped below 10 microns and the critical charge for upsetting a circuit dropped below 1 pC (roughly corresponding to a particle LET of 50 MeV-cm^2/mg and a collection depth of 2 microns). It has really been the internal feedback loops within the latches that made SEUs important over the last decade for these types of circuits.

Static latch SEU vulnerability has been calculated [7] and measured [5] as a function of technology feature size to establish the relationship between the critical charge needed to upset the circuit and the technology feature size. All results indicate that the critical charge needed to upset a latch decreases as the square of the feature size. If this relation holds as electronics feature sizes decrease from 0.8 micron (present day spaceborne) to 0.18 micron (present day commercial), the critical charge will decrease by nearly a factor of 20.

Experimentally observed LETs for 0.8 micron standard cell latch designs have been as low as 5 MeV-cm^2/mg and as high as 20 MeV-cm^2/mg. Even with thinner epi layers, 0.18 micron designs could have SEU threshold LETs no higher than 1 MeV-cm^2/mg. While the area cross section for a heavy ion hit will be a factor of 20 lower, the integral fluency of cosmic rays above 1 MeV-cm^2/mg is 1000 times larger than the fluency above 20 MeV-cm^2/mg for a geosynchronous orbit [3]. This implies an SEU error rate (per bit) increase of a factor of 50. Since 0.18 micron designs will likely have 20 times the number of latches on a given die size as 0.8 micron designs, the total IC error rate will be 1000 times larger.

Clearly novel approaches will be needed to alleviate the problem. The radiation-effects community has historically focused on the problem of SEUs in SRAMs and latches. Some of the most interesting work has focused on latches for use in ASIC (application specific integrated circuit) designs, although the results could conceivably also be applied to SRAM designs. The first such latch [8] uses a cross-isolation method to ensure that the state of the latch cannot be altered by a heavy ion strike on any single critical node. A more recent design [9], termed the DICE (dual interlocked storage cell) latch, also cannot be upset with a single node strike.

Each of these latches can, however, be upset if a single cosmic ray traveling through the IC at a shallow angle nearly parallel the surface of the die simultaneously strikes two sensitive junctions. The geometrical cross section for this happening, while small, may still be significant for some spaceborne applications (for typical standard cell layouts, error rates can be usually be reduced by a factor of 10^4). Cross sections and error rates for multiple junction strikes will be discussed later in more detail. We mention these latches here because they will later be of use in our proposed approach to additionally eliminate multiple bit upsets from sequential circuit designs.

III. AN EMERGING SEU MECHANISM

Cosmic rays can also induce transients in combinatorial logic, in global clock lines, and in global control lines. These single event transients, or SETs, have only minor effects in present 0.8 to 0.7 micron technologies since the speed of these circuits is insufficient to propagate the 100 to 200 ps SET any appreciable distance through the circuit. However, as smaller feature size (and thus faster) technologies find their way into spaceborne systems, these transients will be indistinguishable from normal circuit signals.

This is illustrated in Figure 2 which shows, as a function of technology feature size, the critical transient pulse width needed in order to propagate without attenuation through an infinitely long chain of inverters. At pulse widths smaller that the critical width, the inherent inertial delay of the gate will cause the transient to be attenuated and the pulse will, after passing a few gates, die out. At pulse widths equal to or larger than the critical width, the transient will propagate through the gate just as though it were a normal circuit signal. As a general rule of thumb, transients of width greater than the critical width will propagate through any number of gates without attenuation, transients of width less than half the critical width will terminate in the first gate, and transients of intermediate width will propagate through a varying number of stages.

The curve in Figure 2 is the result of SPICE [10] simulations performed for various technology feature sizes (shown by the dots on the curve) between 1.2 microns (1200 nm) and 0.13 microns (130 nm). A generic set of SPICE model parameters was developed using known model parameters for technology sizes between 1.2 microns and 0.7 microns, inclusive. The constant field scaling rules were applied to the generic model and to the transistor sizes to predict model parameters at the smaller feature sizes. Our scaled values of various critical parameters (V_{DD}, Vth, and T_{OX}) were consistent throughout with projections published in the National Technology Roadmap for Semiconductors [2]. The solid curve in Figure 2 simply connects the simulation points while the dashed curve simply extrapolates the points to 0.05 micron (50 nm), the projected feature size of commercial technologies in the year 2012.

As discussed earlier, cosmic ray induced transients have pulse widths of 100 to 200 picoseconds. We see from Figure 2 that in the next one or two generations of spaceborne microelectronics systems, when feature sizes drop below 0.35 microns, SETs will no longer be attenuated within the gates of a circuit and will propagate as normal circuit signals. This will have serious, if not grave, implications for sequential circuits.

Figure 3 illustrates a typical circuit topology found in nearly all sequential circuits. The data from the first latch (U1) is typically released to the combinatorial logic on a falling clock edge, at which time logic operations are performed gates. The output of the combinatorial logic reaches the second latch (U2) sometime before the next falling clock edge. At this clock edge, whatever data happens to be present at its input (and meeting the setup and hold times) is stored within the latch.

If a heavy ion strike occurs within the combinatorial logic block, and the logic is fast enough to propagate the induced transient, then the SET will eventually appear at the input of the

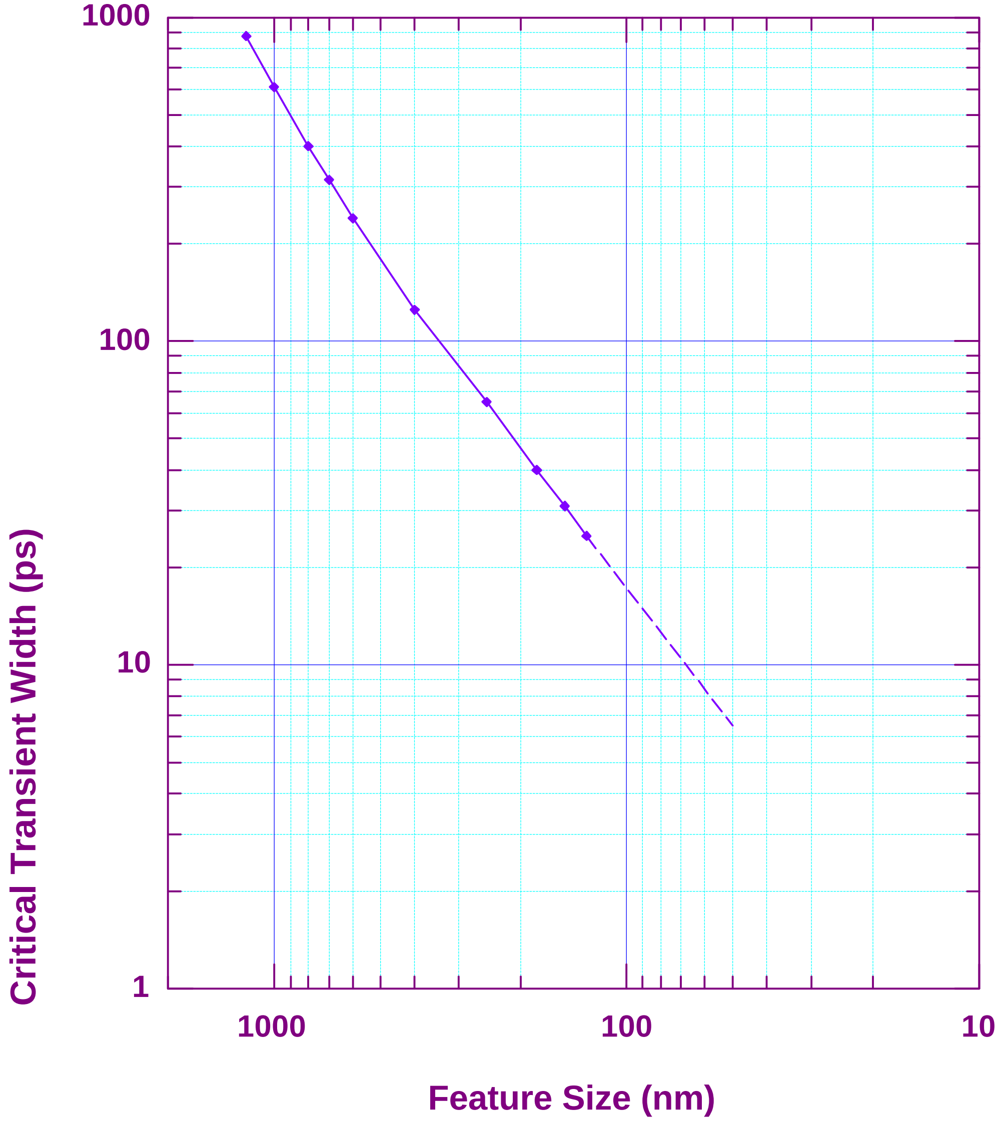

Figure 2. Critical Transient Width vs Feature Size for Unattenuated Propagation.

second latch in Figure 3 where it may be interpreted as a valid signal. Whether or not the SET gets stored as real data depends on the temporal relationship between its arrival time and the falling edge of the clock. Additional invalid transients can occur at the combinatorial logic outputs as a result of SETs generated within global signal lines that control the function of the logic. An example of this would be SETs generated in the instruction lines to an ALU (Arithmetic Logic Unit).

Figure 4 illustrates this temporal relationship for the case that the true data is low and a positive SET appears at the input to the latch. The transient will be incorrectly interpreted as valid data and subsequently stored in the latch if it is high during the time period extending from a setup time before the clock edge and to a hold time after the clock edge. The figure shows four times at which an SET can arrive, with (a) and (d) satisfying a non-latching condition and (b) and (c) satisfying the earliest and latest, respectively, arrival times for a latching condition. Clearly the latch must be fast enough so that the setup time plus the hold time is less than the width of the SET.

Figure 5 illustrates the temporal relationship for another type of SET that can cause invalid data to be stored in the latch. In this case, the transient occurs on the clock line itself. The true data, shown at the top, satisfies the latch setup and hold times relative to the falling clock edge in order for it to be correctly stored under normal circuit operation as shown in (a). The figure also shows three SETs on the clock line, one negative transient (b) and two positive transients (c) and (d). The clock SET of (c) does not cause any problems since it comes and goes after the high data has been stored and while the data remains high. The SET of (b) causes a low to be incorrectly stored. The SET of (d) causes the latch to store a low in place of the previously stored high. Note that transient (d) need not be coincident with the falling data to cause a problem. The latch will be corrupted for any clock line transient whose falling edge is later than the data falling edge.

The radiation-effects community is becoming aware of the problem and the propagation of SETs has recently been investigated [11] as part of an effort to develop software for estimating error rates in complex VLSI (very large scale integration) designs. The thrust of this effort was to develop algorithms and software, based on experimentally observed transient pulse attenuation through combinatorial gates, to predict SET induced error rates in future generation ASICs. Test circuits were fabricated for this effort in a 1.0 micron CMOS process. Pulsed laser illumination of circuit junctions was used to induce transient pulses wide enough to propagate appreciable distances (heavy ion induced pulses are too narrow to produce effects in a 1.0 micron process). It should be noted that the authors observed a critical transient pulse width (infinite transmission through their inverter chain test circuits) of 680 ps, which compares favorably with 610 ps that we calculate (Figure 2) with our generic scaled SPICE models.

It is also important to note how the various error rates (latch SEU and combinatorial logic SET) in sequential circuits depend on the clock frequency. Upsets can occur in latches only when the clock is low and the latch is in a hold state. Since the clock is always low 50% of the time, latch SEU rates do not depend on the clock frequency. However, SETs produced in the combinatorial logic will be stored if they reach the latch input coincident with clock edges, the number of which depend linearly on the frequency. Thus the SEU rate for latches is independent

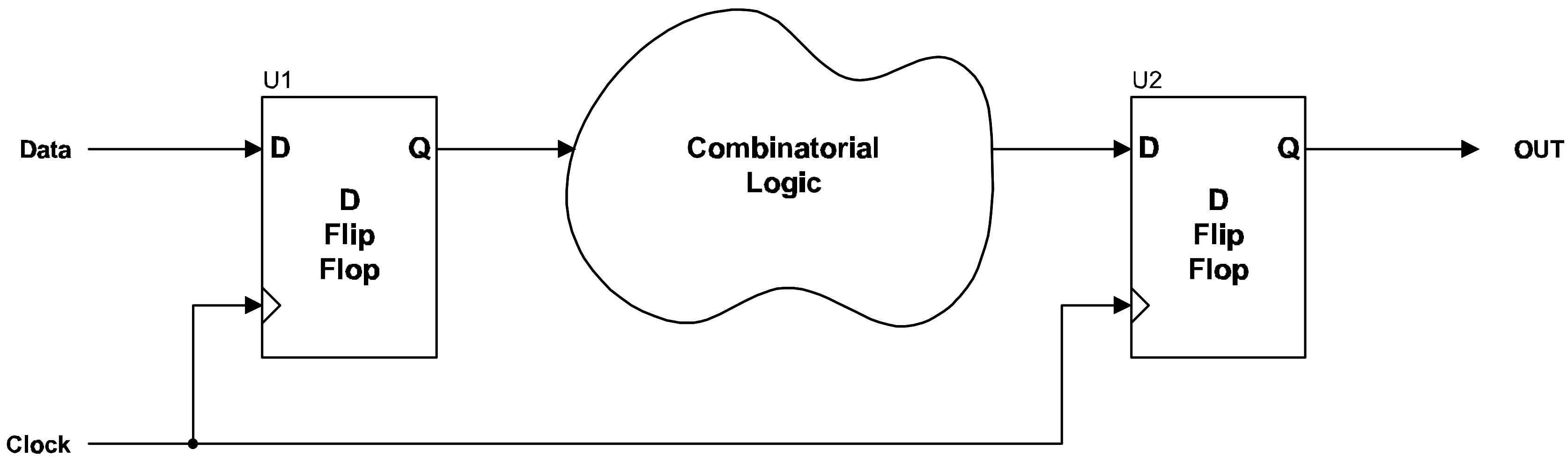

Figure 3. Typical Sequential Circuit Topology.

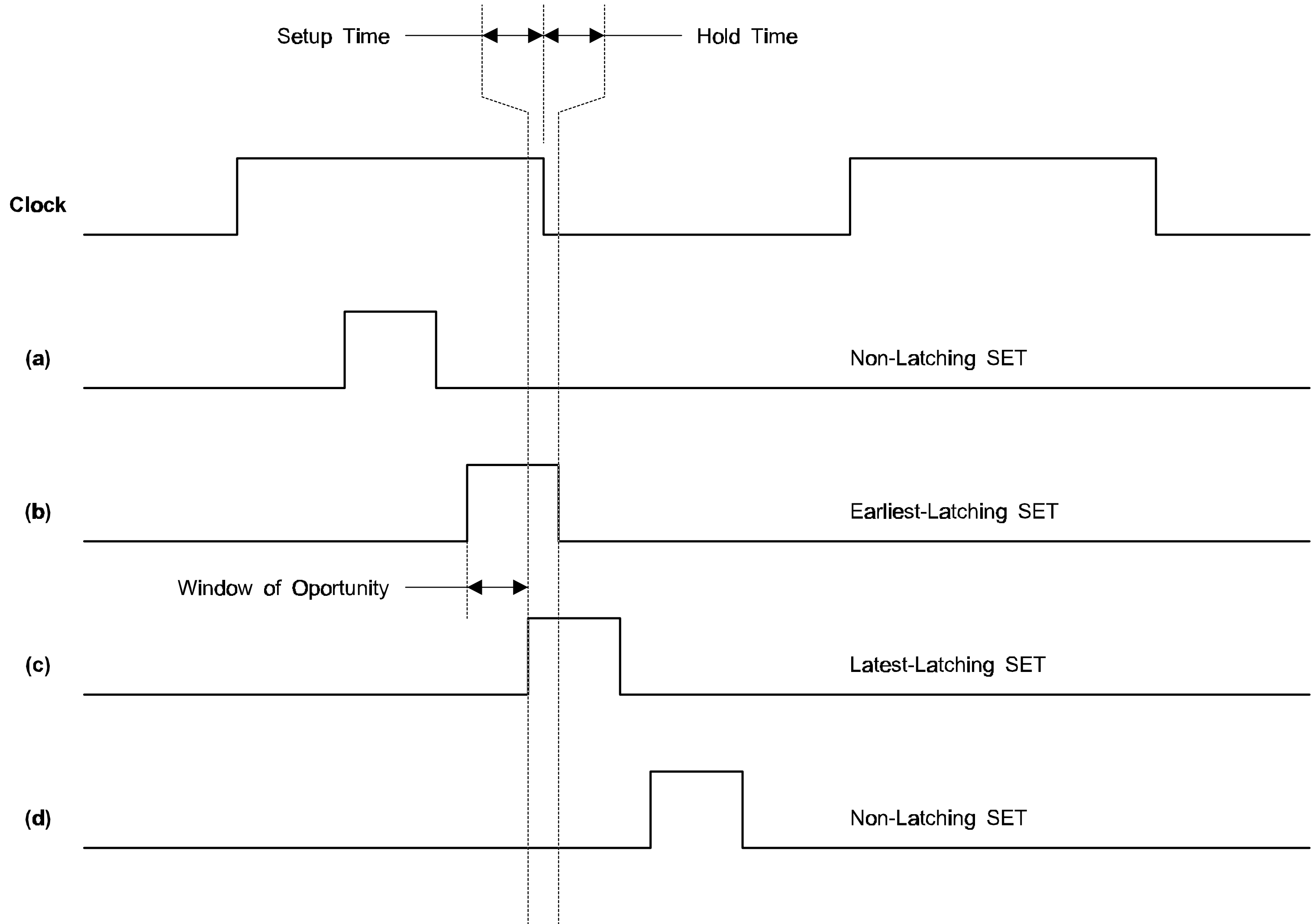

Figure 4. Temporal Relationship for Latching a Data SET as an Error.

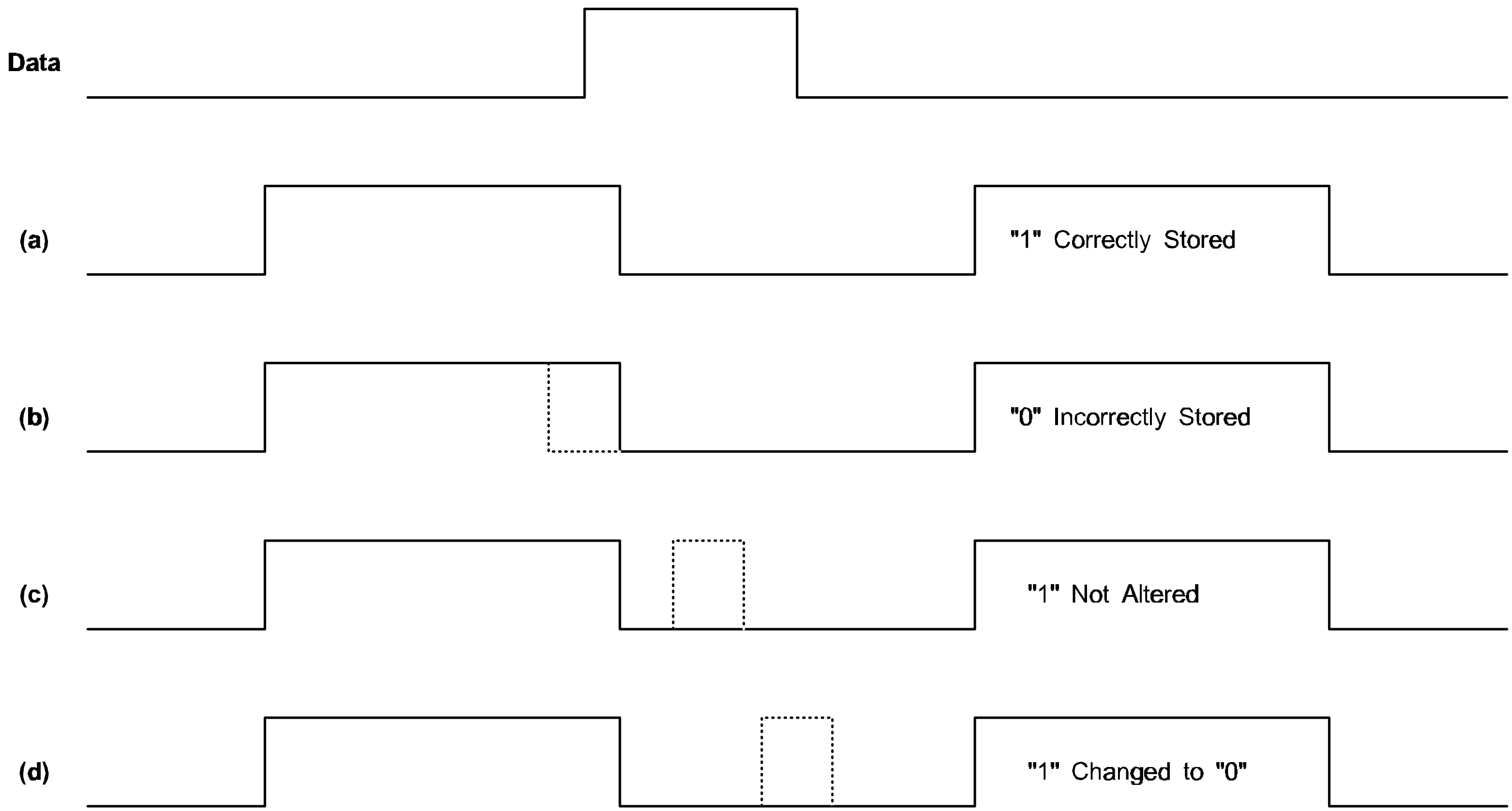

Figure 5. Temporal Relationship for a Clock SET to Cause an Error.

of clock frequency while the combinatorial logic SET error rate is directly proportional to clock frequency. These error rate relations have actually been demonstrated experimentally [12] using pulsed laser illumination of test circuits while measuring the various error rates as a function of clock frequency.

These error rate relations actually compound the SET problem as IC technology feature sizes shrink since smaller feature sizes result in smaller gate delays that permit circuits to be operated at higher clock frequencies. Not only will each combinatorial gate in a circuit contribute transient errors (because transients will no longer be attenuated), but the probability of storing any given error will also increase (because of the higher clock frequencies).

To date, efforts in the area of SETs have been limited to characterizing the mechanisms, simulating the propagation process, and developing analytical tools to estimate error rates in future designs. The focus of our work is to develop circuit techniques to solve this SET problem as well as to solve the conventional static latch SEU problem.

IV. CONVENTIONAL HARDENING TO SETS

Several obvious hardening approaches can be used to help mitigate transient pulses in combinatorial logic and clock lines [13]. The most straightforward at the IC design level is to use high drive transistors with increased node capacitance. High drive transistors dissipate the transient charge more quickly and high node capacitance reduces the voltage excursions resulting from the transient charge. This necessarily results in physically larger circuits (for the high drive devices) with longer propagation times (from the capacitance needed to attenuate SETs). But reducing IC size and increasing speed are exactly the reasons for using smaller feature size technologies in the first place.

Some hardening measures can also be taken at the system level. Redundant computation, either using multiple chips or multiple calculations on a single chip, can be used to detect errors. The latency of an error becomes an issue in these cases because it may be many clock cycles before an error manifests itself at the circuit outputs. Should an error be detected, rollback to a previously known good state would have to occur. These techniques place heavy burdens on the system engineers and result in overly complex systems that must include periodic storage of known good state variables so resets can be performed. As device feature sizes decrease, error rates might even increase to such an extent that these techniques are no longer even feasible. Rollbacks might become so frequent that no appreciable error free computational time remains.

V. ASIC DESIGN SYNTHESIS

ASIC designs have become so large in the past few years that automated design synthesis and layout tools are an absolute necessity if one hopes to achieve a reasonable time to market design cycle. Even in the area of radiation hardened microelectronics, present 0.8 micron features sizes easily permit 500,000 to 1,000,000 transistor circuits on a single IC. For present day commercial technologies, and future radiation hardened technologies, 20,000,000 transistor ICs are typical. Manually sizing transistors and tailoring node capacitances in ASIC designs of this size is not a viable option because of the large amounts of manual design, simulation, and layout time that would be required.

Automated design synthesis tools, unfortunately, have not been developed with even the simplest of radiation hardening design methods in mind. The "Design Compiler" software from Synopsys [14], for example, requires that each latch and flip-flop in the library contain only a single global clock input. The tools will not accept latches that have, as inputs, both a clock (CLK) and its complement (-CLK). In SEU hardened designs, both CLK and -CLK are best treated as global signals, each routed over the chip using high drive buffers and high capacitance lines. In synthesized designs, -CLK is generated locally at each latch which introduces lightly driven low capacitance nodes that have a low LET threshold for upsetting the latch.

This is just an example of how existing tools are unable to handle even the simplest of upset mechanisms. Computer algorithms for synthesizing, from conventional logic libraries, designs hardening against combinatorial SET induced errors have not even been investigated. Software tools to analyze ASIC designs and predict error rates [11] are in their infancy.

It is unlikely that design tools will ever be developed for synthesizing SEU hardened designs. This will not be done by the current commercial software vendors since the spaceborne IC market is too small. Government funding for the development of such software is not practical since, without a large market, the Government would be forced to continuously subsidize the vendor for the long term maintenance of what would be an expensive tool set.

VI. TEMPORAL SAMPLING LATCH

We have developed a new and novel circuit approach to eliminate cosmic ray induced upsets from sequential circuit designs. The upsets eliminated include both static latch SEUs that dominate at present day technology feature sizes as well as upsets resulting from combinatorial logic and control line SETs that will dominate in future technology generations. This new circuit is termed either the "temporal sampling latch" or the "temporally redundant latch." Its intended use is to replace conventional latches in any sequential circuit that must provide high, or total, immunity to SEU.

A. LATCH CONSTRUCTION

A simple embodiment of the temporal sampling latch is shown in Figure 6. The circuit contains nine level sensitive latches (U1 through U9), one majority gate (U10), and three inverters (U11 through U13). Each level sensitive latch is transparent (sample mode) when its clock input is high and is blocking (hold mode) when its clock input is low. When in sample mode, data appearing at the input D also appears at the output Q. When in hold mode, the data stored within the latch appears at the output Q and any data changes at the input D are blocked. Two level sensitive latches in tandem and clocked by complementary clock signals (such as U1 followed by U2) form an edge triggered D-Flip-Flop. With the clock inversions used in Figure 6, the D-Flip-Flops formed by (U1,U2), (U3,U4), and (U5,U6) are triggered on the falling edges of the clocks CLKA, CLKB, and CLKC, respectively.

The complement of each clock is formed locally by the inverters U11, U12, and U13. There is therefore no need, for hardening purposes, to route global complimentary clock signals over the chip. As we shall later see, heavy ion induced transients on the clocks will not affect the SEU immunity of the temporal sampling latch.

The three D-Flip-Flops (U1,U2), (U3,U4), and (U5,U6) operate in parallel and form the temporal sampling stage of the circuit. Each of these three D-Flip-Flops drives another level sensitive latch. These latches (U7, U8, and U9) together with a simple majority gate (U10) form the sample release stage of the circuit.

The upset immunity of the circuit in Figure 6 is a consequence of two distinct parallelisms: (1) a spatial parallelism resulting from the three parallel circuit branches and (2) a temporal parallelism resulting from the unique clocking scheme. Previous redundant systems have used only spatial parallelism to achieve SEU immunity to cosmic ray strikes in static latches (inherently spatial). Immunity to SETs in combinatorial logic and global clock lines (inherently temporal) cannot be achieved with spatial redundancy alone -- some form of temporal redundancy must be additionally included.

Why not just replicate the combinatorial logic and the clock lines to form a totally spatially redundant circuit? This is exactly what has been done for redundant computation described above and error latency becomes a problem. In our approach, the combinatorial logic is effectively replicated, not in space but in time. The same logic is really just used at three different times. The result of this (although it may not yet be obvious) is that errors are flushed

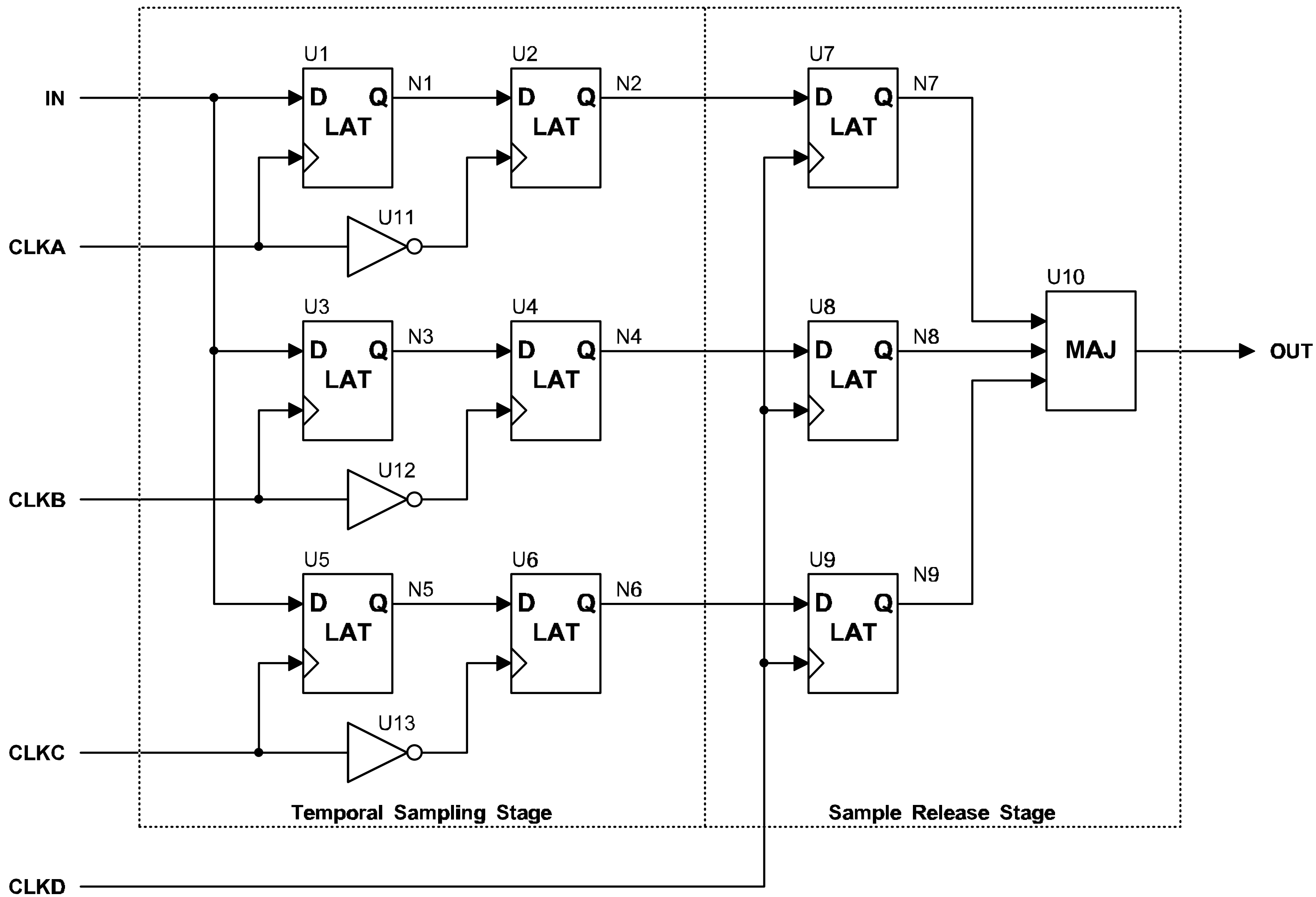

Figure 6. Temporal Sampling Latch With Sample and Release Stages.

on each clock cycle and the maximum error latency never exceeds a clock period. This has good implications for multiple bit upsets which are discussed in a later section.

Temporal redundancy of our circuit as achieved by combining a temporal sampling stage with a sample release stage where the sampling is controlled by three clocks (CLKA, CLKB, and CLKC) and the release is invoked by CLKD. The clocking scheme is therefore central to the operation of circuit and will now be discussed.

B. CLOCKING SCHEME

The clocking scheme is shown in Figure 7. The figure shows four cycles of the master clock and two cycles of the temporal sampling latch control clocks. The master clock (top curve) would generally be the clock signal brought onto the chip through an input pad. It could also be a higher frequency clock generated on chip with a clock multiplier synchronized to the input clock through a phase locked loop. The bottom four curves in Figure 7 show the four clock signals (CLKA, CLKB, CLKC, and CLKD) used in Figure 6.

Each of these four clocks operates at a 25% duty factor and each is phased to the master clock as shown in Figure 7. CLKA is high during the first half of cycle one of the master clock. CLKB is high during the second half of cycle one of the master clock. CLKC and CLKD are high during the first and second halves, respectively, of cycle two of the master clock. Thus a full cycle of the A, B, C, and D clocks occupies two cycles of the master clock. These clocks are actually quite easy to generate with simple circuitry presented in a later section. Controlling the fidelity of the four clocks is not a problem since the temporal sampling latch will operate correctly even in the presence of skew or overlaps.

C. CIRCUIT OPERATION

The operation of the circuit of Figure 6 with the clocking sequence of Figure 7 is most easily explained if we start at the beginning of a computational cycle. To keep the explanations simple, we will refer to all events relative to clock edges without regard to setup and hold times. When we state that a signal must arrive somewhere before a clock edge, we assume the reader understands that it must really arrive a setup time earlier than the clock edge. When we say that a signal appears at an output after a clock edge, we assume the reader understands that it will appear after a time equal to the clock-to-output time.

The computational cycle begins at the rising edge of CLKD. At this time the sample release latches (U7,U8,U9) pass their input data to the majority gate (U10) where it subsequently appears at the output node (OUT). CLKD subsequently goes low, the release latches (U7,U8,U9) enter a hold state, and this original data remains asserted on the output for the remainder of the computational cycle.

This output data is then processed by intervening combinatorial logic before it appears at the input to the next temporal sampling latch stage. (This is just the typical sequential circuit topology shown previously in Figure 3.)

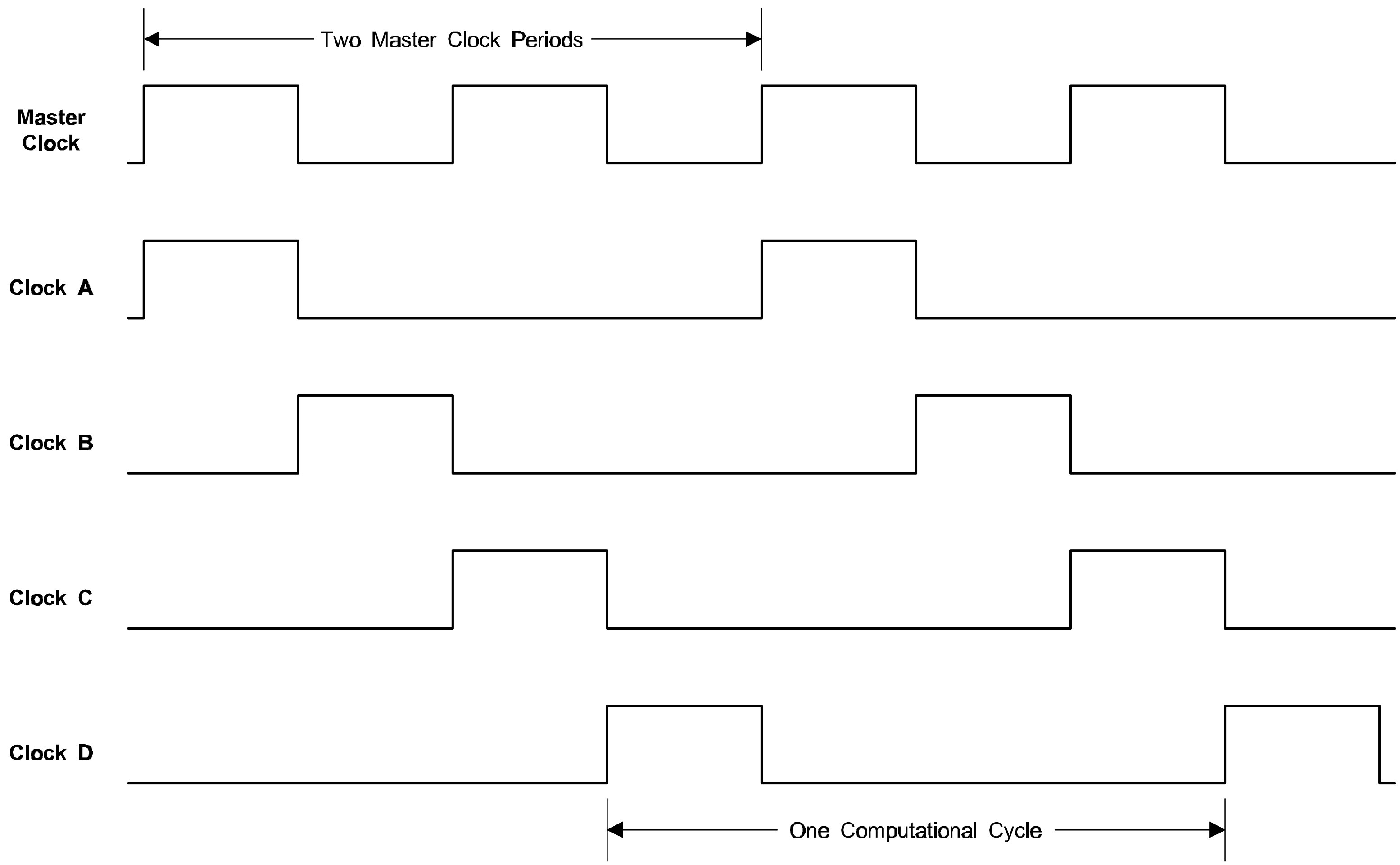

Figure 7. Temporal Latch Control Clocks Derived from Master Clock.

The data then arrives at the input to the next stage before the falling edge of CLKA at which time the data is stored in the a D-Flip-Flop formed by latches (U1,U2). CLKB then goes high to sample the input. Whatever data is at the input when CLKB goes back low is then stored in the D-Flip-Flop formed by latches (U3,U4). Finally, CLKC toggles high and low to sample and hold the input data in the final D-Flip-Flop formed by latches (U5,U6).

At this time another computational cycle begins. The input data to each temporal sampling latch has been asserted on the three inputs to the sample release stage. When this next computational cycle begins, CLKD again goes high and the data appears at the output of the majority gate.

Figure 8 illustrates the voltage values on each node in the circuit of Figure 6 for a complete computational cycle. It shows how each node voltage is correlated to the clock signals for a temporal sampling latch whose input is high at the start of a computational cycle and goes low before the falling edge of CLKA.

D. ELIMINATION OF UPSETS

Upsets of the temporal sampling latch are avoided as a result of the spatial parallelism provided by the three circuit branches and the temporal parallelism provided by the sampling and release architecture of the design. It is simplest to describe the upset immunity of the design in terms of four distinct upset mechanisms: (1) static latch SEU, (2) data SET, (3) sampling clocks SET, and (4) release clock SET. The first of these, static latch SEU, is the upset mechanism of primary concern in present day spaceborne microelectronics systems fabricated in 0.8 micron to 0.7 micron feature sizes. The last three mechanisms will be of concern in future systems fabricated in 0.35 micron and smaller feature sizes.

Case (1): Static latch SEU occurs when a cosmic ray flips the data state of a latch whose clock is low and is in a blocking state (hold mode). Any such single upset in any of the nine latches in Figure 6 (U1 through U9) will only affect one of the three parallel data paths through the circuit. When data release occurs, one of the three nodes N7, N8, or N9 will be in error while the other two will be correct. The majority gate will then ensure that the correct data value is asserted on the output node. Such a data flip can occur at any time within the computational cycle and not affect the output value.

Case (2): Data input SETs occur when a cosmic ray strikes a node in the combinatorial logic preceding the temporal sampling latch and the resulting transient propagates to the input node just as a normal signal. This transient will be latched into only one of the three parallel sampling paths if it arrives on a falling edge of one of the three sampling clocks (CLKA, CLKB, or CLKC). Just as for the preceding static latch upset mechanism, only one of the three parallel data paths will be corrupted. When data release occurs, the majority gate will again ensure that the correct data appears at the output node.

Case (3): Cosmic ray strikes on nodes in the clock generation circuitry or in the clock distribution tree will produce SETs on the clock signal lines that can cause the latches to toggle data at unintended times. The three sampling clocks (CLKA, CLKB, and CLKC) are used

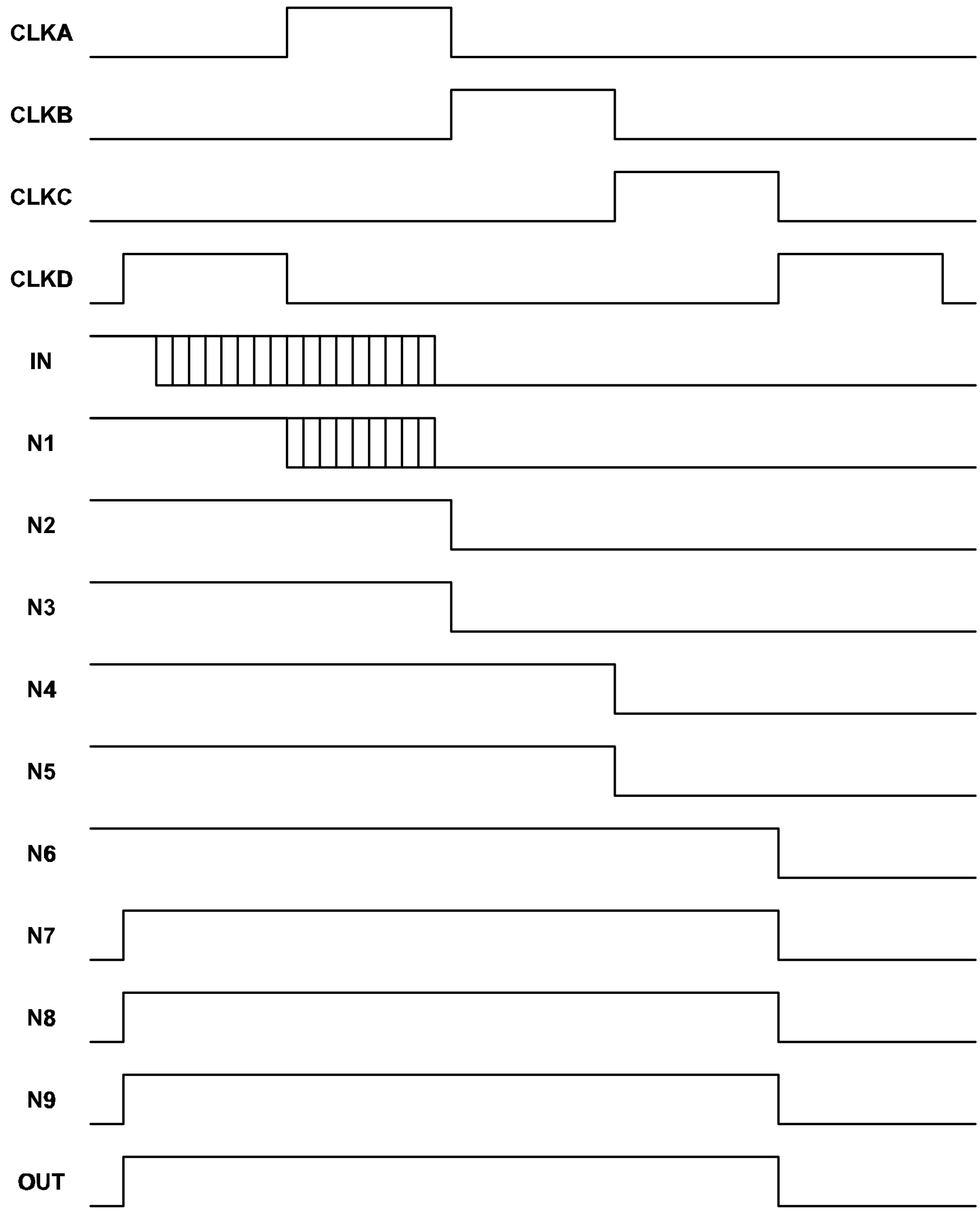

Figure 8. Sample Node Values for One Computation Cycle.

symmetrically in the design and can be discussed together. Remember that the controlled latch pairs (U1,U2), (U3,U4), and (U5,U6) each form a falling edge triggered D-Flip-Flop. At falling clock edges, these D-Flip-Flops store whatever data happens to be present at their inputs. If a clock is low, an SET will result in a rising edge followed by a falling edge. If a clock is high, an SET will produce a falling edge followed by a rising edge. In either case a data store occurs.

There are two time intervals in the computational cycle that may be affected by a sampling clock SET. The first interval starts at the rising edge of CLKD (beginning of a computational cycle) and ends when the released data arrives at the input to the temporal sampling latch which will experience a sampling clock SET. The second interval starts at this data arrival time and ends when CLKD again transitions high (beginning of the next computational cycle).

If the SET induced falling edge on any of the sampling clocks occurs in the first of these intervals, old data will be stored in one of the three parallel sampling paths. The true (intended) falling edge will occur later and the correct data will be sampled. The only exception is for CLKA which may experience an SET that overlaps the true falling edge. This shifts the falling edge to an earlier time by an amount less than or equal to the SET pulse width. If this shift causes a setup time violation of the (U1,U2) D-Flip-Flop, then old (incorrect) data may be stored in the first of the three parallel sampling paths. As in the above cases, only one of the three parallel paths will be corrupted and the majority gate once again produces correct data values at the output.

If the SET induced falling edge occurs in the second of the intervals defined above, the only effect will be to store the correct data. This SET may occur before the actual clock edge (in which case the correct sampling is performed early) or it may occur after the actual clock edge (in which case correct data is re-sampled). The SET may overlap the true clock edge in which case a single correct sampling is performed slightly early.

Case (4): The effects of an SET on the release clock (CLKD) are somewhat different than those on the sampling clocks discussed above. Again, it is easiest to discuss two distinct time intervals in the computational cycle. The first interval is when CLKD is high and the second interval is when CLKD is low.

A negative transient when CLKD is high causes each of the sample release latches (U7, U8, and U9) to momentarily hold what was being sampled and then, when the clock restores, continue to sample what was being sampled in the first place. This event therefore has no effect on the operation of the circuit.

A positive transient when CLKD is low will cause each of the sample release latches (U7, U8, and U9) to first sample its input (become transparent) and pass the value to the majority gate and then store (hold) this data value for the majority gate when the transient disappears. The effect depends the current state of CLKA, CLKB, and CLKC.

If such a positive transient occurs before the falling edge of CLKA in the computational cycle, nodes N2, N4, and N6 in Figure 6 will still have their original values and the majority gate output will not change. If the event occurs between the falling edge of CLKA and the falling edge of CLKB, node N2 may have changed but nodes N4 and N6 will still have their original values and the majority gate will still produce the correct output. Finally, if the transient occurs between the falling edge of CLKB and the falling edge of CLKC, both nodes N2 and N4 may have changed (to the next cycle values) and only node N6 will have its original value. In this case the majority gate output may change. However, this is simply a premature change to the next sample release value that would have eventually occurred anyway when CLKD was scheduled to rise. This premature data change could then get latched into the CLKC branch of a downstream sampling latch if it arrives before the falling edge of CLKC.

If this transient on CLKD is local to a single sampling latch, then the majority gate of the downstream temporal sampling latch will suppress the erroneous value (just as it suppress the Case (1) and Case (2) events discussed above) and the premature data release will be confined to the single affected latch. If this transient is common to a group of sampling latches, all latches in the group will release prematurely. If the transient is global to the chip, such as would happen if the transient occurred in the clock generator, then all latches on the chip will prematurely release their data. In each case, nodes are simply assuming correct data values one quarter of a computational cycle early. All data values achieve correct synchronization at the start of the next computational cycle.

An important point that applies to each of the four upset mechanisms just described is that any erroneous data stored in any of the sampling latches gets flushed within a single computational cycle. Any premature data releases get back in phase within one quarter of a computational cycle. Thus the latency these erroneous values never exceeds one computational cycle.

Each of the discussions in this section has focused on the response of the temporal sampling latch to the effects of a single cosmic ray striking a single circuit node. In each case the circuit has proven to be immune to upset. Extensive simulations have also been performed to ensure that each of the explanations presented is correct and that the circuit truly is totally immune to upset from single node strikes.

Multiple node strikes, although having a much lower probability of occurrence, could conceivably cause an upset. These multiple strike events are discussed below in a later section. Cases are identified where multiple events could cause upsets and special circuit implementations are discussed which can make the temporal sampling latch immune to even these low probability multiple node hits.

Each of the discussions above have also assumed that the width of the SET is less than the width of any of the four clock pulses that control the latch. If the SET pulse width exceeds any of the clock pulse widths, then the temporal sampling latch will exhibit a non-zero error rate. For typical 100 ps to 200 ps SET durations, this limits the master clock frequency of Figure 5 to 2.50 GHz and limits the on-chip computational speed to 1.25 GHz.

E. CLOCK GENERATION

Generating the four temporal sampling latch control clocks (CLKA, CLKB, CLKC, and CLKD) from the master clock is straightforward. Figure 9 shows a simple circuit to do this. The master clock (CLK) is brought on chip through a pad buffer. It is used to clock a D-Flip-Flop formed from level sensitive latches U1 and U2 with the compliment of CLK formed by the inverter U3. The output of U2 is fed back to the input of U1, with an inversion provided by U4. U1 through U4 perform a divide-by-two operation on the master clock, generating a new clock signal of one half the frequency. Latches U1 and U2 are provided with power up reset circuitry (not shown) to initialize the sequence.

The master clock and the half frequency clock signals are then used as addresses for the decode U5. Address bit 0 (A0) is taken from the master clock and address bit 1 (A1) is taken from the half frequency clock. The decode will generate a high on only one of the four outputs according the address (A1,A0). As shown in Figure 9, the decode will toggle the output lines in the following address order (1,1), (1,0), (0,1), and (0,0). These output lines are selected, in this order, to provide the four control clocks shown earlier in Figure 7.

The clock generation circuitry in Figure 9 is itself susceptible to upsets. In particular, an SEU in one of the level sensitive latches would cause the on-chip control clocks to get out of phase with the master clock. We therefore prefer to use the clock generator circuit of Figure 10 which is immune to upset.

In Figure 10, the master clock is brought onto the chip through a pad driver cell that immediately breaks the signal into three independent paths through three independent buffers U1, U2, and U3. In this way there exists no single node for which a cosmic ray strike can simultaneously affect more than one master clock input of the subsequent generator circuits.

Three instances of the circuit in Figure 9 (U4, U5, and U6) are used in Figure 10. These instances contain the circuitry enclosed within the dashed box of Figure 9. (Note that in Figure 9 the dashed box breaks the wire connecting the latch output to the inverter input.) In Figure 10, each of the three latch outputs are fed to three majority gates (U7, U8, and U9) and the majority gate outputs are fed back to the three inverter inputs within the generator subcircuits.

We now have three parallel generators, each of which provides a full complement of on-chip control clocks. Four additional majority gates (U10, U11, U12, and U13) generate the final control clocks (CLKA, CLKB, CLKC, and CLKD) from the individual generator subcircuit outputs.

The resulting circuit can no longer get out of phase with the master clock. Furthermore, any internal erroneous latch values within U1, U2, or U3 are purged within two master clock cycles. A cosmic ray strike on one of the internal nodes in any of the final majority gates can produce an SET on a clock line. These SETs, as described in the previous section, will not affect the operation of the temporal sampling latches.

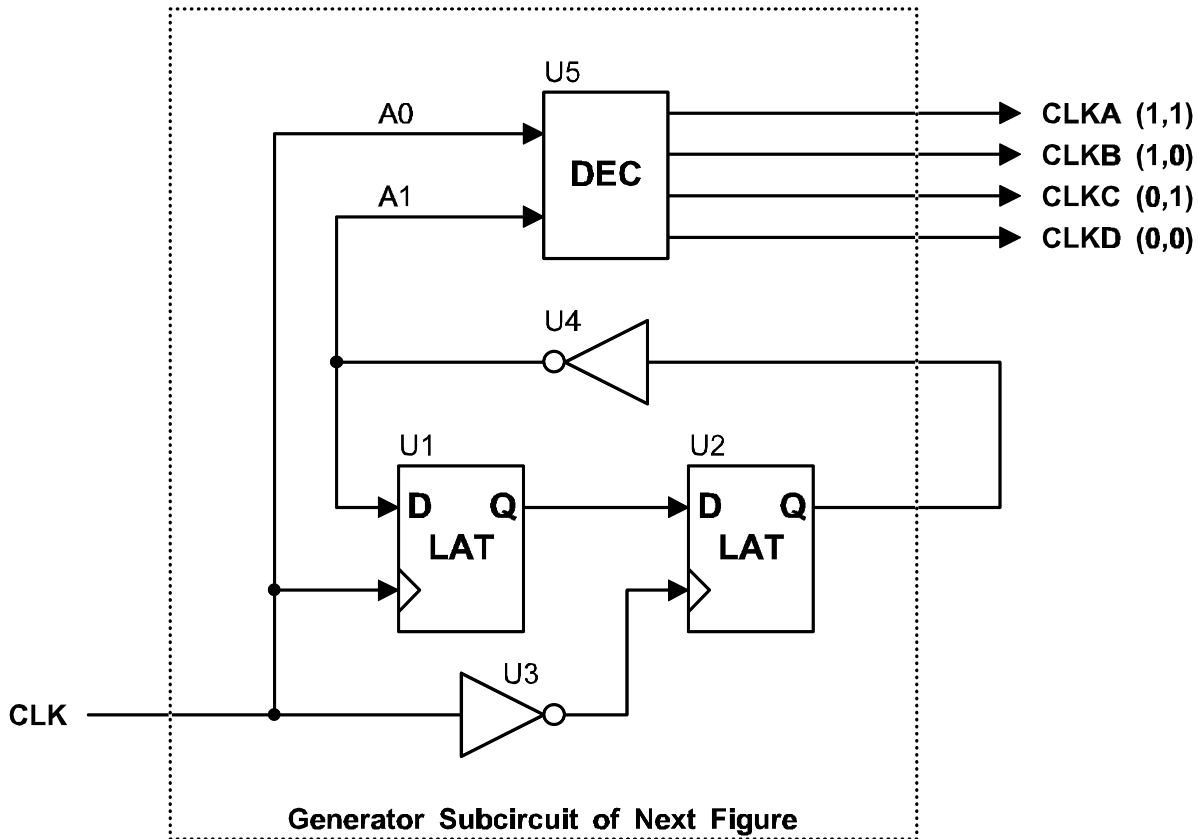

Figure 9. Simple (Non-SEU Immune) Control Clock Generator Circuit.

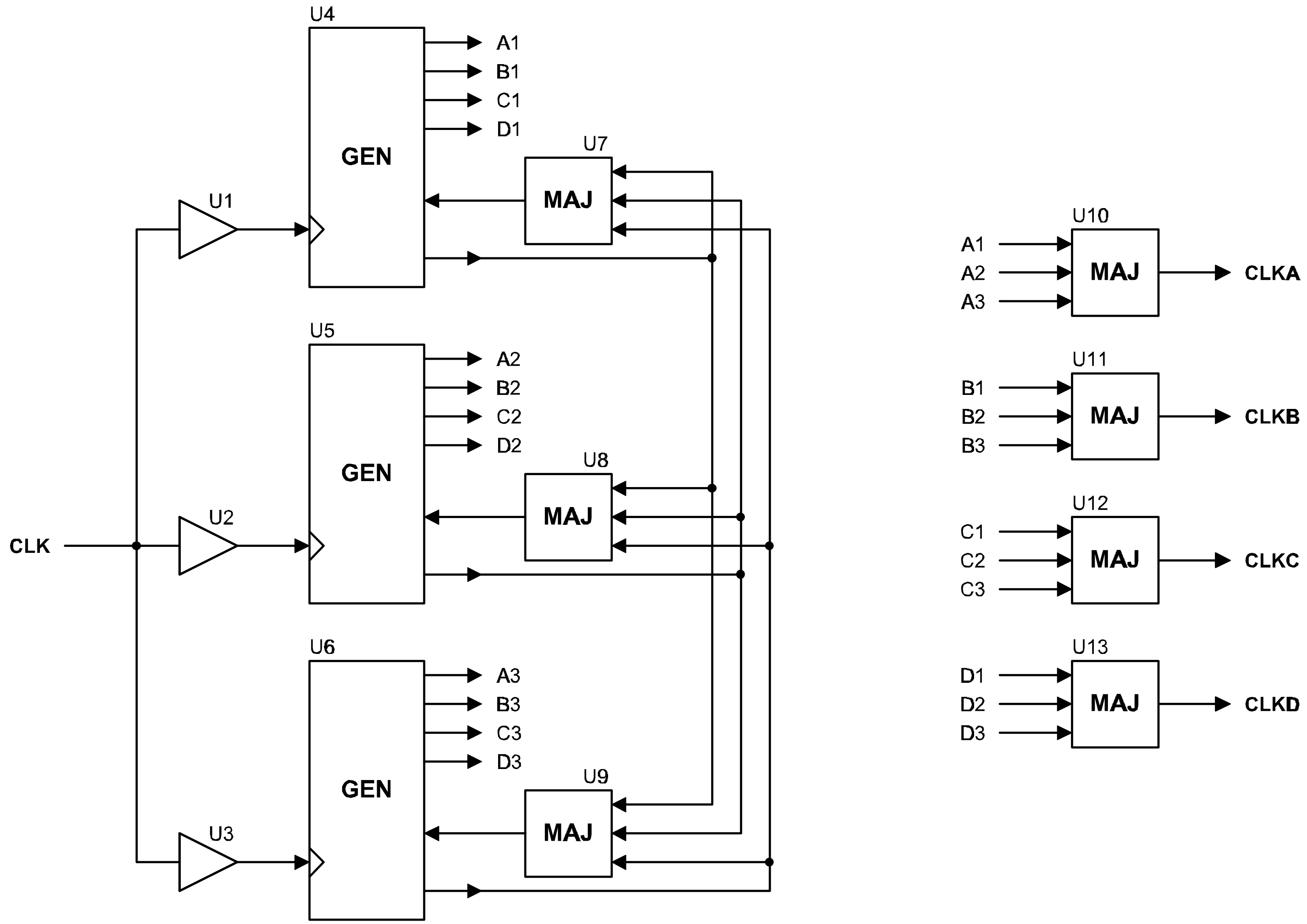

Figure 10. Final SEU Immune Control Clock Generator Circuit.

F. FAST MODE OPERATION

It is possible, using the circuitry shown in Figure 11, to select the clocking mode of operation of a chip designed with temporal sampling latches. The MODE signal is immediately split into four independent paths by the buffers U1, U2, U3, and U4 which are part of the MODE input pad driver cell. The master clock signal (CLK) feeds the clock generator circuit U5 previously shown in Figure 10. A fourth clock buffer U6 is now included in the CLK input pad driver (the other three are schematically inside of U5, but physically included with U6 in the pad driver cell). The resulting parallel paths for MODE and CLK prevent a single node strike from creating multiple clock transients when the chip is operated in the SEU immune mode using the clocking scheme of Figure 7.

The MODE signal simply specifies which input of each of the four multiplexers (U7, U8, U9, and U10) will be selected for the four clocks (CLKA, CLKB, CLKC, and CLKD). For one value of MODE, the multiplexers select the clock signals generated by U5. In this mode, the chip will operate in SEU immune mode (as per the Figure 7 clocking scheme) with one computational cycle being performed every two master clock cycles.

For the other value of mode, the second input of each multiplexer is selected. In this case, CLKD is held high so that the sample release stage of each temporal sampling latch is always transparent and the sampling clocks (CLKA, CLKB, and CLKC) are each driven by the master clock signal. In this mode, the chip operates at the master clock frequency and the only SEU immunity provided by the temporal sampling latch is an immunity to static latch SEU since we still have three D-Flip-Flops operating in parallel.

This second mode of operation can be used to speed up computations in the field by a factor of two when immunity to SETs is not a concern. It is also a very useful mode that can be used for earth based SEU testing. In these tests, an IC is placed in a beam of high energy heavy ions produced by an accelerator and error rates are measured. By operating the chip in fast mode, error rates due to SETs alone can be measured as a function of LET and master clock frequency since static latch SEUs are still suppressed. Such testing can provide important data to characterize fabrication technologies as a function of feature size.

G. SPEED TRADEOFF

A conventional (SEU susceptible) sequential circuit would use simple D-Flip-Flops (each formed from two level sensitive latches) triggered on the falling edge of the master clock. Such a circuit (Figure 3) would satisfy timing constraints such that the data delay through the intermediate combinatorial logic would be small enough that the data would reach the next D-Flip-Flop before the next falling edge of the master clock. In other words, in any conventional sequential circuit, the maximum combinatorial logic transit time would be less that the period of the master clock (minus the D-Flip-Flop setup time).

In our temporal sampling latch, data is released to the combinatorial logic on the rising edge of CLKD and must reach the next sampling latch stage before the falling edge of CLKA (minus the setup time). From Figure 7, this is just the period of the master clock minus the

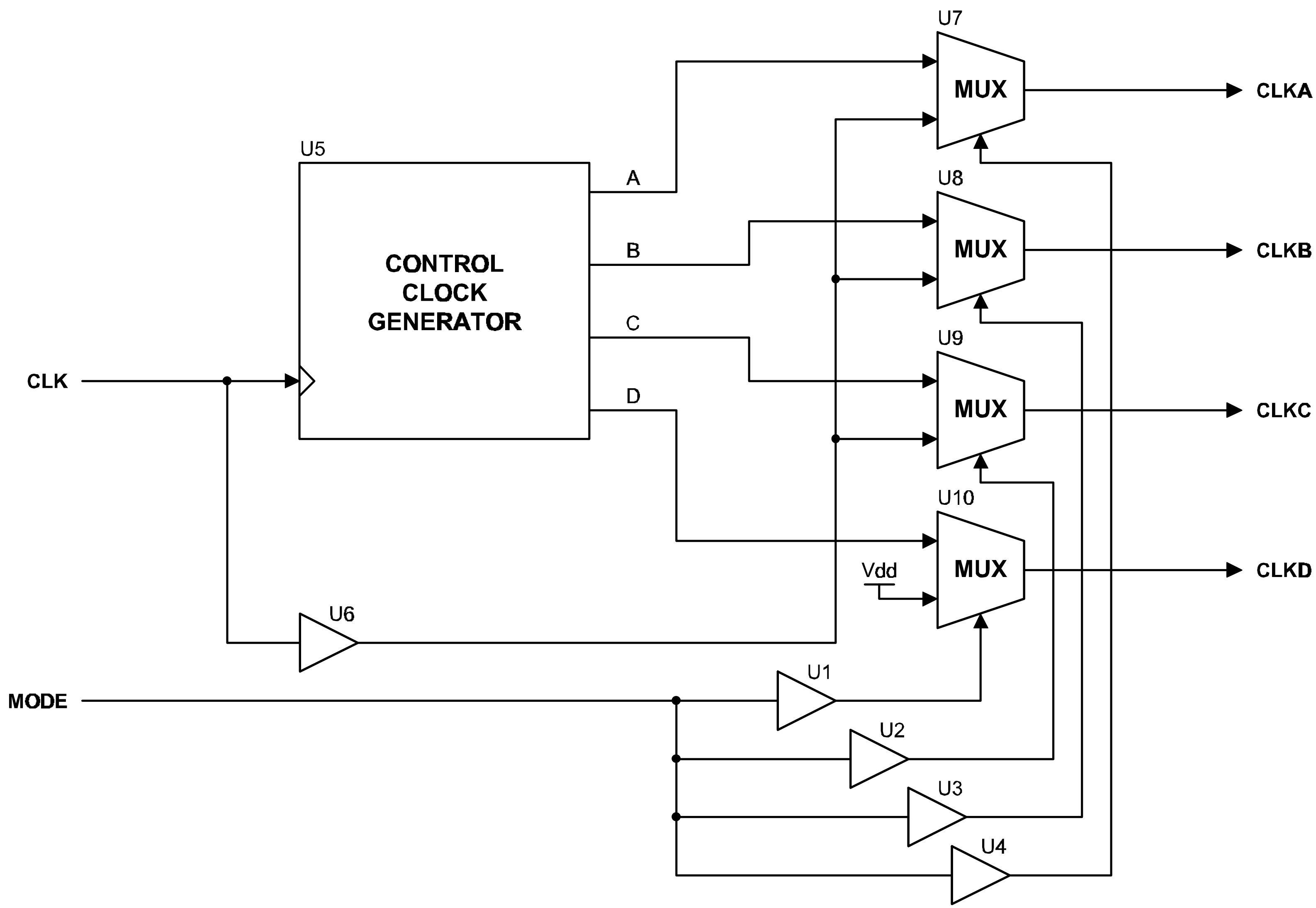

Figure 11. Circuit to Select Between SEU Immune and Fast Modes of Operation.

D-Flip-Flop setup time. Thus a conventional circuit that satisfies the timing constraints for the master clock will automatically satisfy the timing constraints of our new clocking scheme.

The insertion of the two extra clock phases (CLKB and CLKC) is needed for the additional temporal sampling. In Figure 7 we show these phases as occupying one additional master clock period. In this case the effective on-chip computational frequency is exactly one half the frequency of the master clock provided from off-chip. Therefore a factor of two speed penalty has been incurred to ensure upset immunity.

The CLKB and CLKC widths could actually be smaller than we have shown in Figure 7. Their widths need only be greater than the maximum width of any SET induced in the combinatorial logic. As an example, a system might provide a master clock signal to the IC which has a frequency of 50 MHz. CLKA and CLKD would therefore each have widths of 10 ns. CLKB and CLKC could each be as narrow as 500 ps (0.5 ns) and still reject the SETs produced in the combinatorial logic. This results in an effective on-chip clock period of 21.0 ns corresponding to a frequency of 47.6 MHz. In this case only a minor speed penalty (4.8%) would be incurred by using the temporal sampling latches. If the CLKB and CLKC widths were kept at 500 ps as the master clock frequency was increased, then the speed penalty would approach its maximum value of 2× as the master clock frequency approached 1 GHz.

We believe, however, that the clocking scheme of Figure 7 would be preferred in most designs because it is simple to generate and because an effective on-chip frequency exactly one half the master clock frequency would be easier to synchronize to other signals at the board level. Also, if the CLKB and CLKC widths are too small compared to the CLKA and CLKD widths, then second order errors, such as multiple strikes in the combinatorial logic (described later), could conceivably occur.

H. SIZE TRADEOFF

Clearly the temporal sampling latch will occupy more area on an IC than a conventional D-Flip-Flop. A conventional D-Flip-Flop can be constructed from two level sensitive latches while our temporal sampling latch is constructed from nine level sensitive latches plus one majority gate. Since a three input majority gate layout (12 transistors) is roughly the same size as a level sensitive latch (10 transistors), one might expect the temporal sampling latch to occupy about five times as much IC area as a conventional D-Flip-Flop. For any given ASIC design, however, the total chip area will never grow by a factor of five. There are three reasons for this, which are explained below.

First, only the D-Flip-Flops in the design must grow -- all of the combinatorial logic can remain unchanged. The amount that any given ASIC must grow will depend on the ratio of D-Flip-Flop area to total chip area. We have examined several latch intensive ASIC designs that we have recently completed. The first, an anti-jam filter, has 7.5% of its area devoted to D-Flip-Flops. Various blocks of this design include multipliers, adders, and subtractors for which D-Flip-Flops account for 3.7%, 15.0%, and 25%, respectively, of their total areas. Another recent design, an 8-bit ALU, contains addition, subtraction, bit shift, and bit logic blocks. The fraction of this chip devoted to D-Flip-Flops is 7.2%. The total size penalty, expressed as an area increase factor, for using temporal sampling latches in these chips would therefore be 1.30 for the filter and 1.29 for the ALU.

Secondly, the "conventional" latches being replaced may not be conventional at all. They may be latches designed to already contain some level of SEU immunity. This will not have been done without some area penalty of its own. Hardening via high drive transistors and high node capacitance (to increase the critical charge threshold for upset) makes these latches 1.5 to 2.0 times larger than the minimum sized latches used in the temporal sampling latch. Hardening via transistor decoupling (such as the cross-isolated latch [8] and the DICE latch [9]), makes these latches 2.0 to 2.5 times larger than minimum sized latches. In these cases the area penalty, per D-Flip-Flop, for using our temporal sampling latch would be no more than a factor of 2 or 3.

Finally, in some ASIC designs, total SEU immunity may only be necessary in certain blocks of sequential logic. In this case only the D-Flip-Flips of the critical blocks need to be replaced by temporal sampling latches. The percentage of chip area occupied by these critical blocks as well as the percentage of critical block area occupied by D-Flip-Flops must be considered when estimating how much a given ASIC design will grow.

We expect that the more complicated clocking scheme will have only a minor impact on total IC area. The clock generation circuit need only appear once in a design and its larger size will be insignificant in comparison to the total IC size. The additional routing needed for the extra global clocks is not a problem in the latest fabrication technologies which permit four to five levels of metal. Our clock distribution may be replacing an SEU hardened clock distribution (high drive buffers with high capacitance lines) in which case the total buffer area may actually be smaller and the power requirements less.

As feature sizes decrease and designers seek to avoid the adverse effects of SETs, conventional hardening approaches used to attenuate the propagation of transients will result in combinatorial logic that is sized larger than necessary for normal circuit operation. Converting an ASIC design that uses DICE latches along with oversized combinatorial gates to a design that uses our temporal sampling latch with minimum sized gates may not incur any area penalty at all.

I. SCAN CHAIN TESTING

Testing the temporal sampling latch, which is immune to errors, could potentially be a challenge. Fabrication defects could render one of the three parallel sampling stages inoperative. In this case the latch would function normally but could then be susceptible to upset due to a cosmic ray strike.

A redundant scan chain approach can be used to identify such faults. The scan chain redundancy must simply match the temporal latch redundancy. Such a scheme, as shown in Figure 12, allows complete latch verification in each sampling path. It also allows, by intentionally shifting in an error, verification of the majority gate. Combinatorial logic between latches is verified according to normal scan chain procedures. Clock tree multiplexers permit block by block verification over an integrated circuit.

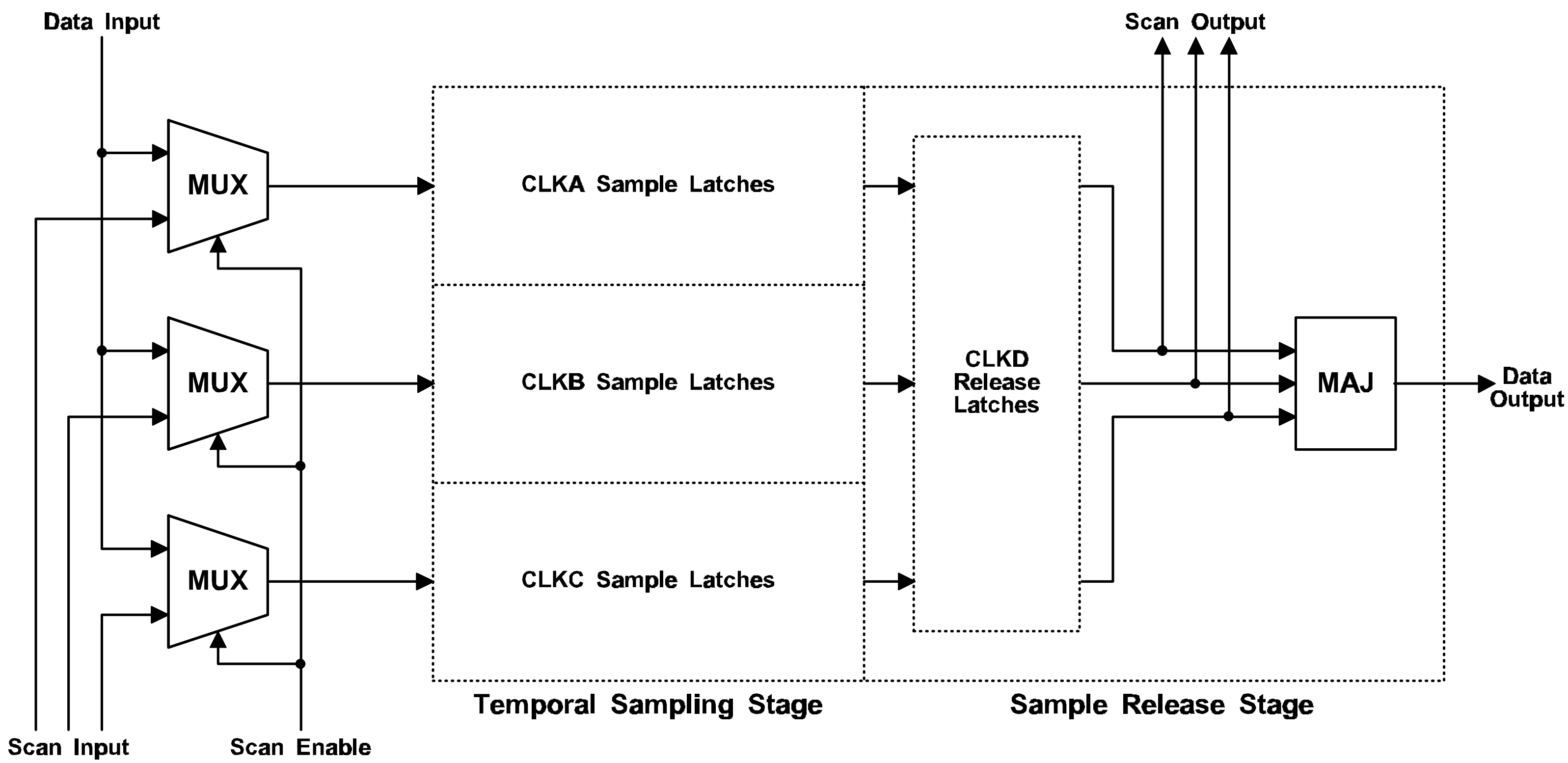

Figure 12. Scan Chain Testing Approach for the Error Immune Temporal Latch.

For synthesized designs, a straightforward replacement of a conventional scan chain by the redundant scan chain means that all of the associated test vectors can be readily used. Test vectors that intentionally load errors are constructed simply by using the test vector compliment for one of the three parallel chains.

J. STATIC DATA STORAGE

It may often be desirable to turn off the clock for long periods of time in order to conserve power. Such might be the case for deep space probes and interplanetary missions. In this case the latches on an IC would effectively become SEU integrators. To prevent this, it is necessary to periodically scrub any errors that might occur within the redundant sampling stages of the temporal latch. Figure 13 shows a scheme to do this for the simple case of a shift register. Only three shift register stages are shown in the figure. The method can obviously be applied to general sequential circuits where additional combinatorial logic would reside between the output of a latch and the input of the multiplexer associated with the next latch stage.

Under a normal clocking configuration, the "Scrub" signal in Figure 3 selects the MUX input from the previous latch and the four clocks (CLKA through CLKD) are as described earlier. When the IC master clock is turned off, a very low frequency scrubbing clock is selected using multiplexers upstream in the clock tree to provide the four clock signals and the "Scrub" signal is changed to select the MUX input coming directly from the latch output.

The scrubbing clock might easily be generated by using a Schmitt trigger input pad with an external resistor and capacitor to set the scrubbing frequency. The scrubbing frequency need not be fast. Several Hz to several kHz will reduce the error latency to between 1×10^{-5} and 1×10^{-8} days and reduce the multiple cosmic ray strike error rate to insignificant levels. (Multiple bit upsets are described in more detail in a later section.) The optimum scrubbing frequency will likely be system dependent and would be user controlled by the RC time constant provided external to the chip.

A shift register as shown in Figure 13 could also be used to store the configuration of a reprogrammable FPGA. The programming data would be toggled in at boot time and the scrubbing clock would maintain data integrity over long periods of time with little power consumption. At small feature sizes (< 0.25 microns), this approach would actually consume less area than conventional SRAMs currently used to store FPGA programmations. This is largely due to the fact that an FPGA SRAM must be highly immune to upset and high threshold LET SRAMs cannot be scaled as feature sizes decrease without compromising their SEU immunity.

K. MISCELLANEOUS CONSIDERATIONS

It is important to note that none of the circuits in Figure 6 need to have any inherent SEU immunity. The SEU hardness is a result of the temporal sampling and sample release processes, not a result of any specific circuit hardening to increase the critical LET. The temporal sampling latch will therefore be immune to upset in any technology feature size. (The only implication of

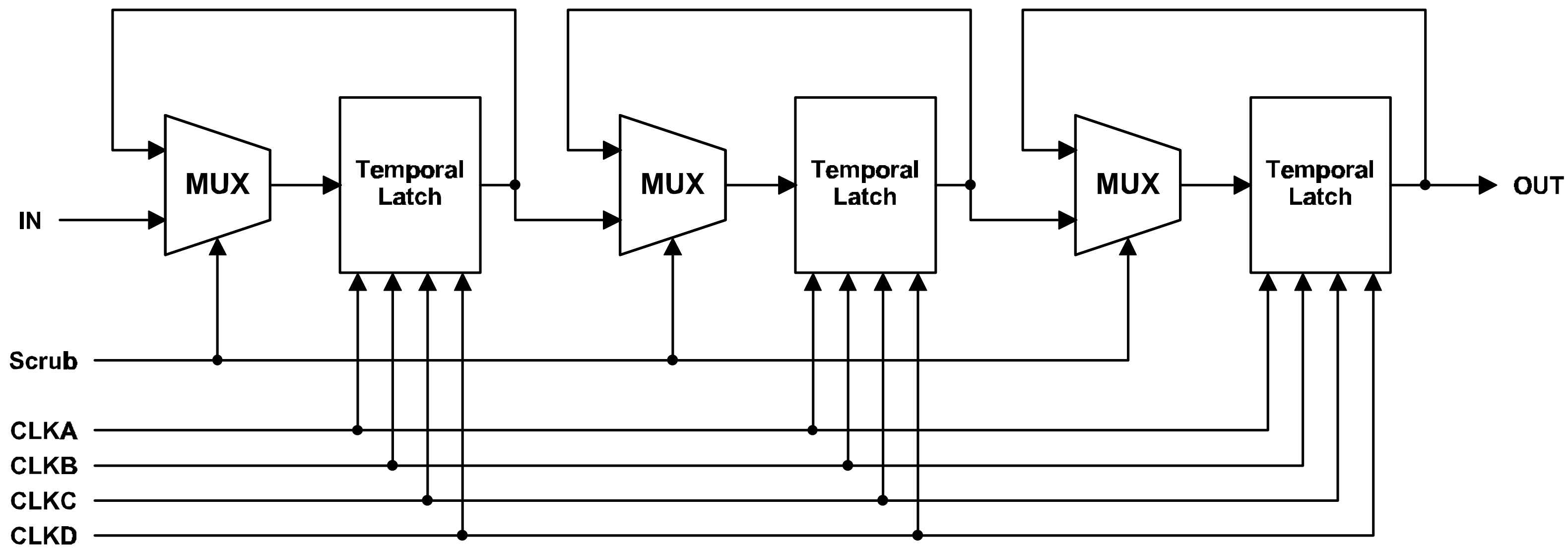

Figure 13. Shift Register Configuration to Self Scrub Errors for Static Data Storage.

using extremely "soft" circuits to construct the temporal sampling latch is for multiple bit heavy ion strikes which is discussed below.)

If the fabrication process is sufficiently hard to total dose so that the NMOS transistors do not exhibit appreciable edge leakage, it would even be possible to implement the temporal sampling latch using dynamic CMOS level sensitive latches without impacting the SEU hardness of the circuit. Since dynamic CMOS latches are small compared to static latches (4 transistors versus 10 transistors), the temporal sampling latch could be made quite small in spite of its complexity. Even if the fabrication process were not total dose hardened, edgeless (doughnut shaped) NMOS transistors could be used with only minor area impact. Dynamic latches could never be used otherwise in a cosmic ray environment because they provide no transistor restoring drive whatsoever when in the hold state.

More complex set/reset (synchronous or asynchronous) level sensitive latches could also be used to build the temporal sampling latch shown in Figure 6. In this case, three separate set/reset control lines (A, B, and C) should be applied only to the temporal sampling stage of the circuit to keep the design totally SEU immune. Whether the set/reset is applied in an asynchronous or a synchronous fashion, the temporal sampling latch output will always set or reset synchronous with CLKD which triggers the sample release.

Input and output pad timing is only slightly more complicated than for a conventional sequential circuit design. The added complication is due to the fact that two master clock cycles are needed for a single on-chip computational cycle. Data at output pads will be valid some time after the rising edge of CLKD (the falling edge of the second master clock cycle). This output data will then remain valid for at least 1.5 master clock cycles (without premature data releases due to CLKD transients, data would be valid for two master clock cycles). Data at input pads must be valid some time before the falling edge of CLKA (the falling edge of the first master clock cycle). It must remain valid for at least 1.5 master clock cycles to ensure adequate sampling time.

Many ASIC designs contain on-chip multiport memories or register files. If these memories are constructed using DICE type cells, these memories can also be made immune to normal SEU (when the cells are latched) and to SETs on the bit and word lines when read and write operations are performed. Such methods are discussed more fully in [9] and fit quite naturally into our temporal latch sampling and release architecture.

L. CONNECTION TO DESIGN SYNTHESIS

The temporal sampling latch approach requires no special custom circuit designs to achieve SEU hardness. Manual sizing of transistors, tailoring of node capacitances, and routing of complementary clock and control lines are never necessary. Successful operation of the sampling latch does not depend on using circuits with inherent immunity to SEU. Because of this, the temporal sampling latch approach is amenable to ASIC design synthesis, in its present state, without the need to develop new and specialized algorithms to handle the special needs of the spaceborne electronics community.

ASIC design synthesis of spaceborne electronics can be performed with existing commercial software tools using a library that contains a D-Flip-Flop characterized with the setup and hold times of the temporal sampling latch. The D-Flip-Flop is the only library primitive that requires modification. Synthesis then proceeds using a simple clock, namely the master clock in Figure 7.

Post-processing of the final netlist is then performed with simple parsing software to generate a final netlist. The post-processing consists of adding the special clock generator at the root of the clock tree, adding three more clock inputs to the D-Flip-Flop primitive, and adding parallel clock trees for the three additional clocks. Global set and reset lines are be similarly treated. The final modified design automatically satisfies all of the timing constraints that were input into the synthesis tool, but it operates internally at one half of the master clock frequency.

The final netlist is then input into the place and route software which generates the physical layout. The place and route tool is simply told to use the temporal sampling latch layout cell as the D-Flip-Flop cell that appears in the netlist. The final netlist can be back annotated with wire delays and timing verification simulations can be performed using models for the clock generator and for the actual temporal sampling latch controlled by all four clocks. Layout versus schematic verification is performed using the final post-processed netlist.

VII. MULTIPLE BIT HEAVY ION STRIKES

Multiple bit upsets (MBUs) can also occur in circuits under certain conditions and must be considered in any spaceborne microelectronics design to ensure that the associated second order cross sections are small enough for the particular application. Three types of such upsets are possible, with the first two caused by a single charged particle and the third caused by two separate charged particles.

A. TYPE 1

The first type of MBU is due to a cosmic ray traveling through the IC at a shallow angle, nearly parallel the surface of the die, and simultaneously striking two sensitive junctions. It is an important mechanism for upsetting multiple bits in SRAM devices and for upsetting certain specialized latch designs (such as the DICE latch) that can only change their data state if two critical nodes are simultaneously driven. The probability of this occurring is largely geometrical with the cross section being proportional to the sensitive areas of the junctions that is normal to the incident cosmic ray and to the solid angle subtended between the these sensitive areas. This geometrical probability decreases as the square of the feature size as devices become smaller. The ratio between MBUs and SEUs, however, remains constant as devices become smaller since the SEU cross section also decreases as the square of the feature size.

Multiple node hits can occur in the temporal sampling latch itself or on the clock tree buffers. A multiple upset in two of the three parallel latch paths in the sampling latch will produce an error at the latch output. Similarly, multiple SETs on two of the tree sampling clocks (CLKA, CLKB, and CLKC) while CLKD is high could cause latch feedthrough for certain fast circuits, such as shift registers.

The probability of this type of MBU can be minimized in a circuit design by taking care in the physical layout so as to separate critical node junctions by large distances and to align such junctions so that the area of each, as viewed from the other, is minimized. For minimum sized junctions, properly aligned and separated (placed in adjacent rows) in a standard cell design, the ratio of MBUs to SEUs can usually be kept smaller than 1×10^{-4}.

In typical 0.8 micron technologies, standard cell latches have exhibited LET upset thresholds on the order of 20 MeV-cm^2/mg and SEU rates on the order of 1×10^{-8} errors/bit-day. This means that MBUs, for 0.8 micron designs, exhibit rates of only 1×10^{-12} errors/bit-day. For a worst case scenario as feature sizes decrease to 0.15 microns, the MBU geometrical cross section will decrease by a factor of 28 (as the square of the feature size), the critical LET could become as small as 1 MeV-cm^2/mg, and the integral cosmic ray fluency above the threshold LET will increase by a factor of 1000 (from 0.001 to 1.0 ions/m^2/sr/s for a geosynchronous orbit [3]). The result of this would be an increase of the MBU rate from 1×10^{-12} errors/bit-day to 4×10^{-11} errors/bit-day. For low earth circular orbits with inclinations less that 40 degrees, the fluency is much less at all LETs because of the geomagnetic cutoff. The MBU rate for 0.15 micron technologies remains under 1×10^{-12} errors/bit-day for these orbits which may be acceptable for most applications.

If the MBU rate is too high for any particular circuit application, a simple solution (albeit with an additional layout area penalty) is to implement our temporal sampling flip-flop using DICE latches, each of which can only be upset if two critical nodes are simultaneously struck by a heavy ion. The temporal flip-flop will then upset only if four critical nodes are simultaneously struck, which can be easily avoided by placing the DICE latches within the layout so that no four critical nodes lie on any straight line. The DICE latches can also be designed to each use two independent clock (and also set/reset) signals of which both must transition to latch in data. This would mean that four clock buffers in the clock tree must be simultaneously struck by a cosmic ray for the temporal flip-flop to experience a double clock SET. Again, it is easy to avoid lining up four critical clock nodes in the layout. In this way, our temporal sampling scheme can be made totally immune to not only SEUs, but also to MBUs.

While the preceding discussions focused on multiple strikes within the temporal sampling latch circuit itself, multiple strikes can also occur in the combinatorial logic that generates the input signal to the sampling latch. Such a multiple strike could produce two distinct transients that would arrive at the latch input at different times. The time interval separating these transients will depend on where in the combinatorial logic the two strikes occurred. An error would be stored if the first transient coincided with the falling edge of CLKA and the second coincided with the falling edge of CLKB. Alternatively, the first and second transients could coincide with the falling edges of CLKB and CLKC, respectively. If the widths of CLKB and CLKC are less than the widths of CLKA and CLKD, then an error can also be stored on the falling edges of CLKA and CLKC. (A CLKA and CLKC alternative is not possible for the clocks shown in Figure 7 since true circuit data could not get through the combinatorial logic from the rising edge of CLKD to the falling edge of CLKA and still meet the setup time requirements).

The probability of this happening will be third order at best. The geometrical cross section will be appreciable only for gates located near one another. A multiple node strike in adjacent gates will produce transients separated in time by an amount small compared to the clock widths (assuming the clocking scheme of Figure 7) and an error will not be stored. A long time interval between two such transients implies gates separated by large distances which means the geometrical cross section is extremely small.

Pathological layouts are always possible, however. Such a layout would be one in which (1) the early gates in the combinatorial logic were physically placed near the late gates (so that the geometrical cross section were large) and (2) the propagation time between these gates nearly matched the time interval between clock falling edges. Some sort of layout screening may be necessary to identify such situations and estimate the magnitude of the resulting error rate.

If the error rate of MBUs of this type are determined to be too large (either by analysis, by experiment, or by observation in the field), it is still possible to totally eliminate them in a temporal sampling latch design. Simply use the clocking scheme of Figure 7 and decrease the master clock frequency until the width of the each internal clock signal is larger than the longest propagation time through any group of combinatorial logic. It will then be impossible for two correlated transients to fall on two separate falling clock edges. (Note that (1) this frequency tradeoff will decrease the operational speed of the IC by at most an additional factor of two and that (2) the maximum factor of two will only be realized if the circuit were operating with zero margin on the clock in the first place.)

B. TYPE 2

In the second type of MBU, the heavy ion strikes the IC at an angle nearly normal to the surface of the die. In this case multiple nodes can collect charge and experience voltage transients if sufficient charge is deposited and if the collecting junctions are sufficiently near each other in the layout. Since the strike is near vertical, at least one of junctions must collect its charge via the diffusion component of the charge collection process. This falls off rapidly with distance from the strike and therefore this MBU mechanism is really of concern only in extremely dense layouts, such as SRAMs or DRAMs (dynamic random access memories). In ASIC standard cell designs, critical node separations can easily be maintained at safe values.

C. TYPE 3

In the third type of MBU, two distinct heavy ions strike two critical nodes nearly simultaneously. The window of opportunity for this type of MBU is simply the latency of the initial error. This type of MBU is really of importance only in devices such as DRAMs where the error latency can be long if the refresh rate is low. For our approach, the latency of any given error will never exceed one computational cycle. This type of MBU will, therefore, never have any significant probability of occurring. For example, even at a relatively slow computational clock frequency of 20 MHz (master clock frequency of 40 MHz), the error latency will never exceed 50 nanoseconds (5×10^{-13} days). For even a large SEU rate of 10^{-5} errors/bit-day, this latency will result in a MBU rate of only 5×10^{-18} errors/bit-day, which is totally insignificant (such a multiple bit error would be likely only every 2×10^{17} years).

VIII. SUMMARY

We have described a new and innovative temporal sampling latch design approach which can be easily applied to any sequential circuit. The design approach achieves total upset immunity to any single node cosmic ray strike occurring anywhere in the circuit and at any time within a clock cycle. Since the approach itself is inherently immune to these effects, spaceborne microelectronics can be designed with conventional (non-SEU hardened) standard cell libraries using conventional (non-SEU cognizant) design synthesis tools. Speed (2×) and area (30%) tradeoffs of the approach are minor considering that total SEU immunity is achieved.

Not only are the usual static latch SEUs eliminated, but upsets due to SETs in the combinatorial logic, global clock, and global control signals are also eliminated. Designs using the temporal sampling latch are therefore immune at any technology features size, both present and future.

The temporal sampling latch can also be implemented with special latches and operated at slower clock speeds to additionally achieve immunity to multiple node cosmic ray strikes. Since multiple node strike cross sections are small, these special techniques may be necessary for only a limited number of spaceborne and high-altitude microelectronics applications (such as life-critical systems).

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