

# Diagnosis of Multiple Faults Using $I_{DDQ}$ Techniques

Richard B. Katz  
NASA/Goddard Space Flight Center  
Code 738  
Greenbelt, MD 20771  
Tel: (301) 286-9705  
Fax: (301) 286-1751  
richard\_katz@ccmail.gsfc.nasa.gov

Gary M. Swift  
Jet Propulsion Laboratory  
California Institute of Technology  
4800 Oak Grove Drive, MS: 303-220  
Pasadena, CA 91109

## ABSTRACT

A procedure for diagnosing faults using  $I_{DDQ}$  techniques can identify leakage paths to power and ground as well as bridging faults. This diagnostic has been successfully applied to gate arrays with radiation-induced multiple faults. The feasibility of automating the procedure has been demonstrated and the underlying concepts appear compatible with certain design-for-test techniques.

## I. INTRODUCTION

Field programmable gate arrays (FPGAs) are becoming increasingly popular in both commercial and aerospace applications. These devices consist of a matrix of initially unconnected logic blocks and associated programmable routing resources. The logic blocks in the Actel FPGAs used here are interconnected with dielectric anti-fuses that are high resistance (effectively open) until selectively shorted to join segments.

Irradiation with heavy ions (to simulate cosmic rays in space) revealed a new, unexpected radiation effect [1]: permanent damage manifested by an increase in supply current and intermittent functional failures. Key goals were to identify the failed device structure and to quantify the probability of fault occurrence, which required a statistically significant number of faults. This paper documents the  $I_{DDQ}$ -based techniques for determination of failure cause, accurate fault enumeration, and identification of fault type and location. Occurrence probabilities and mechanism details will be reported elsewhere [2, 3].

## II. TEST DEVICE

The Actel A1280 FPGA containing ~8000 gates is the DUT, with similar results obtained with A1020s. The DUT was programmed as seven varying size shift registers that could be linked to make a 282 element shift register. Most of the elements were in a triple module redundant (TMR) configuration which had the benefit of preserving functionality in the presence of hard errors.

## III. FAULT DESCRIPTION

Unprogrammed (~700,000) anti-fuses are extremely thin (~85Å oxide-equivalent) and a failure would cause the observed symptoms of shorts to rails and bridging faults. Therefore, suspicions were that the radiation-induced faults were partially conducting unprogrammed anti-fuses (although other possibilities were evaluated). Results from the  $I_{DDQ}$  testing in combination with emission microscopy proved this. The major effect of the failures is to reduce noise margins, which explained the intermittent functional failures.

## IV. APPLICATION OF $I_{DDQ}$ TECHNIQUES

Several diagnostic techniques were considered or attempted before the successful  $I_{DDQ}$ -based analyses were developed. The FPGAs built-in probe function is only useful for hard failures. The “net-short” test utility provided with Actel’s programmer succeeded in detecting a single fault but test’s applied voltage exacerbated the damage. Also, the Sentry S50 VLSI tester showed no parametric degradation other than  $I_{DD}$ .

First, “coarse  $I_{DDQ}$ s” (all 0’s, all 1’s, checkerboard) demonstrated that the anomalous currents were a function of state. Walking 1’s data (see Figure) localized failure sites and showed that the current could be reliably controlled. Next, the test apparatus was programmed to selectively turn on/off individual faults, enabling emission microscopy techniques to pinpoint the failure sites (data to be presented in the full paper). The existence of bridging faults was proven by the tedious process of showing identical failure sites for multiple vectors. This was confirmed by interactively running pairs tests showing a difference of state between flip-flops was necessary for the anomalous currents.

Automated techniques for classifying faults as either a short to a rail or a bridging fault were necessary to make the determination of accurate fault counts and mission reliability failure rates tractable. Exhaustively running all possible pairs tests is of order  $n^2$ . An optimized shift algorithm was developed which required approximately 10 hours. The next improvement was to run pairs tests on all “ $I_{DDQ}$  spikes,” states that showed deltas from the baseline (see Figure), which is still quite time consuming for heavily damaged devices.



FIGURE.  $I_{DDQ}$  Results for A1280A s/n:004.

(Note: vector index 0 corresponds to all ones for walking zero and all zeros for walking one.)

The final algorithm exploited the relationship between the walking 1's and the walking 0's data. By analyzing conditions that can cause  $I_{DDQ}$  spikes, it is seen that an 'exclusive OR' of the curves provides the distinction between shorts to rails and bridging faults.

Corresponding (same vector index) spikes of the same polarity indicate that a change in that flip-flop's state relative to all the other flip-flops in the shift register cause the change in current. Corresponding spikes of opposite polarity indicates that the state of that individual flip-flop controls the anomalous current for that part of the DUT. This algorithm is easily automated and is efficient, needing only  $2N+2$  measurements.

Lastly, pairs of vectors involved in the same bridging fault are identified by running exhaustive pairs tests on the minimal set of vectors known to be involved in bridging faults. The paper presents a detailed example making this vector selection and pair identification process clear.

## V. IMPLEMENTATION

Initial  $I_{DDQ}$  work used the S-50 which proved cumbersome, expensive, and non-portable. The remaining work was implemented with an inexpensive, portable, and moderate-speed apparatus: a PC controlling a DVM and microcontroller. The DVM measures across a current-sense resistor and the microcontroller shifts in vectors and reports DUT outputs. This apparatus is used to conduct functional tests, coarse  $I_{DDQ}$ s, and walking 1's and 0's at the irradiation facility. Later, vectors which energize individual faults are interactively applied to the DUT for emission microscopy. Other functions extract vectors causing  $I_{DDQ}$  spikes, determine fault types, and run pairs tests on bridging faults. The final matrix analysis is computed in a spreadsheet. It is feasible to automate the entire procedure by integrating the various operations.

One complication was that significantly damaged devices dissipated  $\sim 1W$ , versus nominal dissipation of  $650 \mu W$  (for A1280As). Thermal stabilization of the device is critical to obtain data which does not drift, as the increased temperature affects leakage currents and the device's transistors' drive into faults. Before reaching thermal equilibrium, the magnitude of the change in baseline current often exceeded the magnitude of current deltas from damage sites, making automation difficult.

## VI. CONCLUSION

Diagnosis of failed, functional VLSI devices with multiple faults is difficult. The procedures described here efficiently solve the problems of failure analysis, fault enumeration, and diagnosis.  $N$  vectors provide information for stimulus patterns to use in conjunction with diagnostic instruments such as emission microscopes.  $2N+2$  vectors are needed for fault enumeration which allowed us to make an accurate prediction of mission failure rates. Diagnosing the faults (type and matching vectors involved in bridging pairs) is done with a vastly reduced set of vectors tested pairwise, which initially was a combinatorially large problem. These techniques lend themselves to automation and have been implemented using only standard, inexpensive laboratory instrumentation. Lastly, design-for-testability techniques incorporated into VLSI devices and circuit boards can take advantage of these methods.

## VII. REFERENCES

- [1] R. Katz et al., "SEU Hardening of FPGA for Space Applications and Device Characterization," IEEE Trans. Nucl. Sci., Dec., 1994.
- [2] G. Swift and R. Katz, "An Experimental Survey of Heavy Ion Induced Dielectric Rupture in Actel FPGAs," submitted to RADECS '95.
- [3] R. Katz and G. Swift, "Anti-fuse/FPGA Reliability in the Heavy Ion Environment," . accepted IEEE NSREC 1995 Data Workshop.
- [4] N. Jarwala and C. Yau, "A New Framework for Analyzing Test Generation and Diagnosis Algorithms for Wiring Interconnects," IEEE Proceedings 1989 ITC.