

An Experimental Survey of Heavy Ion Induced Dielectric Rupture in Actel Field Programmable Gate Arrays (FPGAs)

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Abstract

Irradiations and subsequent failure analyses were performed to investigate single event dielectric rupture (SEDR) in Actel FPGAs as a function of ion LET (linear energy transfer), angle, bias, temperature, feature size, and device type. The small cross sections imply acceptably low risk for most spacecraft uses.

they are accompanied by a variety of radiation issues. Incorporating a patented dielectric "antifuse" technology, they may also present special problems. Indeed, in the course of routine SEE testing with heavy ions, a new failure mode was encountered [1] which ultimately was identified as ion-induced rupture of antifuses [2]. This has been named single event dielectric rupture (SEDR) for its similarity to gate rupture (SEGR) seen in power MOSFETs [e.g., 3 and 4].

I. INTRODUCTION

Actel FPGAs are very attractive to spacecraft designers and indeed are included on many planned missions. However, as highly-scaled non-radiation-hardened devices,

This paper relates the approach taken and the results obtained during a series of follow-up heavy ion tests to quantify SEDR susceptibility. The experimental approach allows the collection of a statistically significant number of events on a given test part for this destructive mechanism. For all three Actel families of devices, SEDR cross sections were obtained as eight parameters were varied: normal LET, angle, lot, feature size, bias, temperature, operating frequency, and data pattern, as illustrated in Figure 1 for a set of irradiations of ACT 2 (A1280-family) devices.

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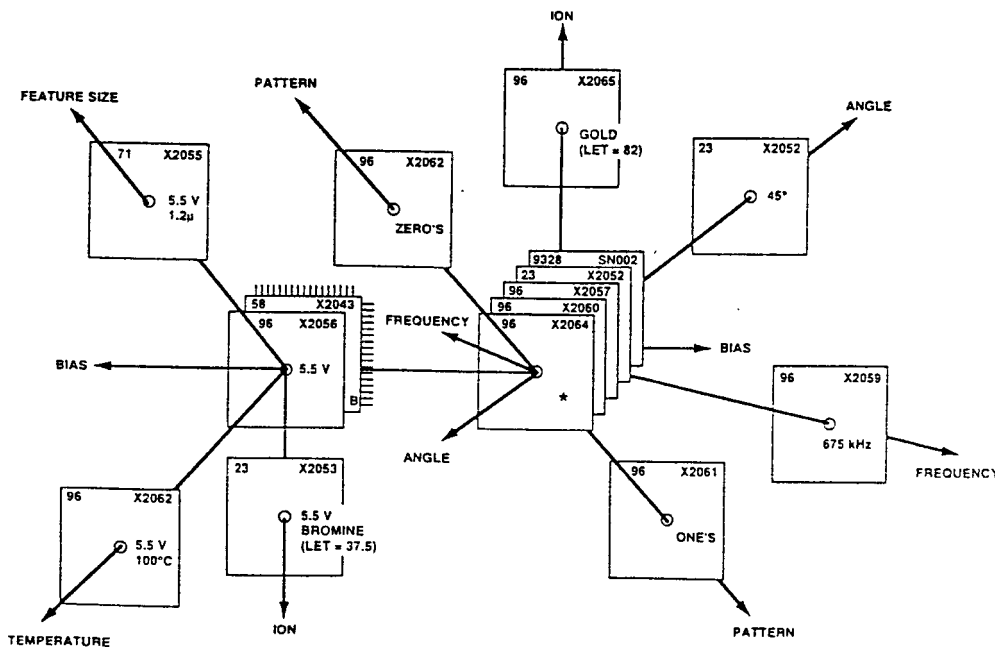


Figure 1. A1280-family SEDR test matrix from test at Brookhaven, 8/2/94

Note the asterisk indicates the matrix "center" of: bias=5V, size=1.0 micron, pattern=alternating, ion=iodine (LET=60 MeV per mg/sq.cm, angle=normal, frequency=2.5 MHz, temperature=room.

II. ACTEL ANTIFUSE STRUCTURE

The Actel FPGAs' silicon real estate is about half devoted to logic modules and half to an interconnection matrix (ignoring peripheral circuitry for programming and control functions). The matrix consists of horizontal and vertical conductors with antifuses at intersections. The antifuse dielectric is a thin sandwich of oxide-nitride-oxide (ONO) measuring ~ 80 to 90 \AA oxide-equivalent thickness. At maximum, an FPGA design will have a few per cent of these connected via electrically induced dielectric breakdown (or rupture), followed by pulses to achieve the desired resistance. An unprogrammed antifuse will be biased when the logic levels on the two crossing conductors differ - which obviously depends on the duty cycle and phase of the two signals. There are many unprogrammed antifuses: $\sim 175,000$ for 1020's (ACT 1), $\sim 650,000$ for 1280's (ACT 2), and $\sim 550,000$ for 1460's (ACT 3).

Operating within the 5.5VDC specification limit, the electric field on the insulating ONO of a biased antifuse is about 6 MV/cm in magnitude, either positive or negative. An undesired partial connection is made when a rupture occurs following a heavy ion strike on a biased antifuse. The symptoms of such a connection can be a) a small current increase only (with possible increased failure rate) or b) an intermittent due to reduced timing and voltage margins or c) a hard fault. Obviously, the seriousness of a particular SEDR depends on circuit considerations surrounding the ruptured antifuse.

III. EXPERIMENTAL APPROACH

To measure cross sections for a destructive phenomenon like SEDR, it is important to establish a test method that allows collecting and counting a statistically significant number of events. This is particularly problematic in SEGR testing of power MOSFETs where the test device is destroyed. The two most interesting aspects of the approach of this investigation are the test device program and the methods for counting SEDR events. Since multiple events were accumulated on individual test devices, care was taken to ensure that the cross section lowering caused by the previous events was not too large. Susceptibility reduction is due mainly to reducing the number of strongly biased antifuses near each SEDR site. A long irradiation was conducted to observe the reduction which became evident after approximately 100 events. Prudence then dictated limiting the SEDR events on a given device to fewer than a third of this number.

The test FPGAs were programmed as shift registers with (mostly) triple modular redundancy (TMR) as described in Ref. 1. Each TMR shift element need only have two of three flip/flops functioning for the test device to continue working,

and single flip/flop failures would not change the biasing on the substantial majority of the antifuses. Some details of the TMR design can be found in Ref. 1. During irradiations, a pattern (all ones, all zeros, or alternations) was clocked through the shift registers while single event upsets (SEUs) were counted and segment failures were noted. A crude count of SEDR events could be made from the strip charts, like Figure 2, of the dynamic current during irradiation.

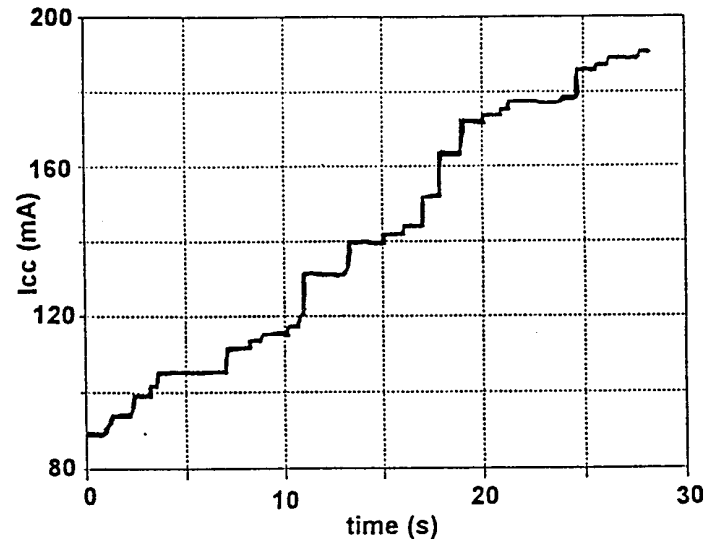


Figure 2. Operating current during irradiation of A1280A device (s/n:350) to a fluence of $2.5 \cdot 10^5$ per cm^2 of iodine ($\text{LET}=60 \text{ MeV per mg/cm}^2$). Other parameters: 5.5V, room temperature, 1.0 micron, 2.5 MHz, alternating pattern.

Additionally, two other SEDR counting methods have been employed. First, emission microscopy techniques (EMMI) were employed to identify high current nodes. Those noted at antifuse locations correspond to damage sites. These high current nodes could be turned on and off with appropriate vectors in the TMR shift registers. Second, an I_{DDQ} diagnostic technique was developed consisting of walking a one (and, later, a zero) through each shift element against a background of the opposite state in all the other elements. A representative example is shown in Figure 3. It was found that this was very revealing, yielding, the most exact number and type of ion-induced connections. Vectors with opposite polarities are stuck to a supply rail, like the first one in Figure 3 which is a fault to ground. Vectors having the same polarity for both "walks" and a magnitude equal to another vector are identifiable as bridging faults. More details of this I_{DDQ} technique are given in Ref. 5.

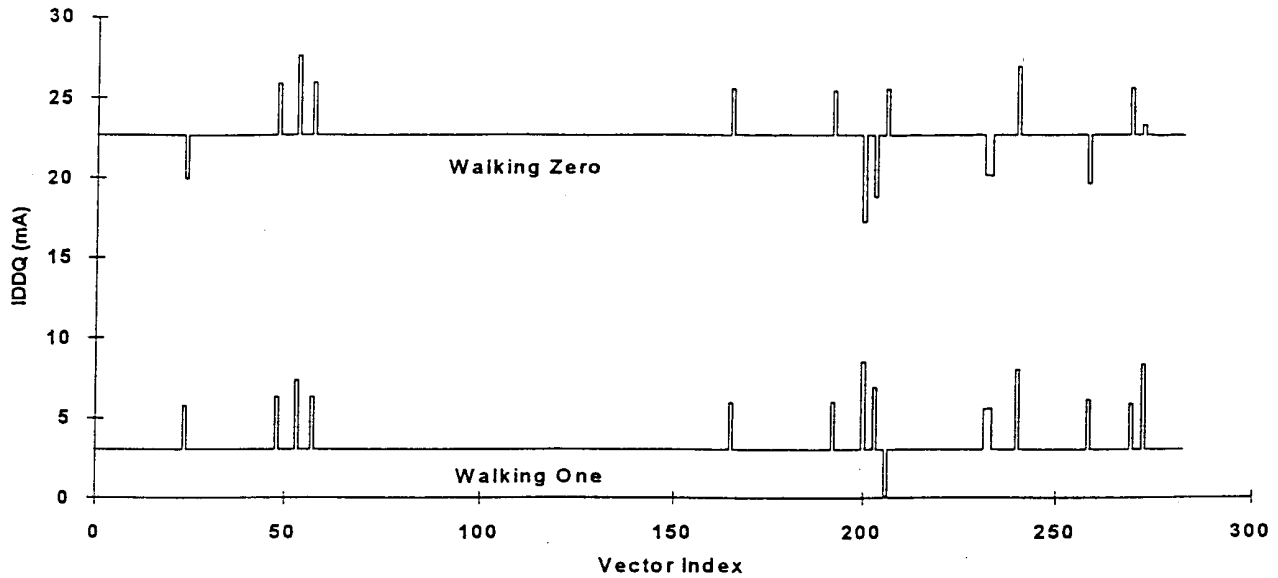


Figure 3. I_{DDQ} technique applied to an A1280A, s/n: 004.

(Note: vector index 0 corresponds to all ones for walking zero and all zeros for walking one.)

IV. RESULTS

Results for the A1280-family of devices are summarized in Table I and charted in Figures 4, 5, and 6. The A1020 devices generally agreed with these results, but scaled by the ratio of numbers of antifuses (roughly four). The cross sections are based on the 95%-confidence-level worst-case values (similar to mean plus three standard deviations) for the expected number of SEDR sites from the observed number. This Poisson treatment is necessary because of the small size of the actual numbers, between zero and 30. Note that these are device cross sections for this particular FPGA test design.

The parameter dependencies can be extracted from Table I. SEDR susceptibility appears to be unaffected by temperature between room temperature and 100° C. Lot-to-lot variation appears to be less than a factor of two while part-to-part variation within a given lot is less than 35%. The effect of feature size is unclear with this data set, and frequency does not affect the cross section. The all-zeros pattern is clearly less susceptible to SEDR, as explained later.

The most interesting dependencies are on normal LET, angle, and bias, and these are plotted in the next three figures. The LET dependent shape is not consistent with that usually observed for SEU or single event latchup (SEL). The threshold for SEDR appears to be very near an LET of 37 MeV per mg/cm² for these antifuses biased at 5.5V, and the cross section should roll off as it approaches the area of the biased antifuses, although there is little indication of that in

the data. The angle dependence is much like that of SEGR, i.e. cross section falls with increasing angle, although this appears somewhat faster than is normally seen in power MOSFET SEGR. Note that ion range limitations should not be a problem, because the antifuse ONO is grown on top surface of the silicon crystal. A channel directly underneath

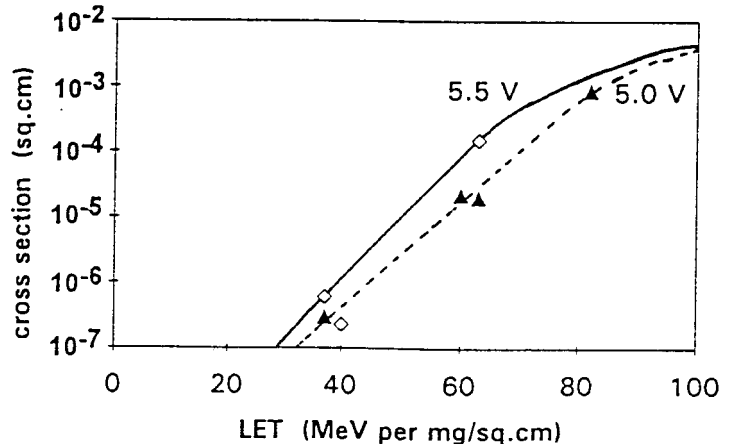


Figure 4. The measured dependence of SEDR susceptibility to normal-incidence LET.

TABLE I. SEDR cross section variations for eight parameters on the Actel A1280-family

		95% Worst Case Device Cross Sections (cm ²)				
Parameter:		# tested	Mean	Min	Max.	Note
Ion:	Au (LET=82)	1	8.7E- 4			5V
	Xe (LET=63)	1	2.0E- 5			5V
	I (LET=60)	5	2.2E- 5	1.1E- 5	4.5E- 5	5V
	Br (LET=37)	1	3.0E- 7			5V
	Xe (LET=63)	9	1.5E- 4	1.1E- 4	1.9E- 4	
	Kr (LET=40)	2	2.3E- 7	1.8E- 7	2.8E- 7	
	Br (LET=37)	2	6.0E- 7	1.9E- 7	1.0E- 6	
Angle:	0 degrees	5	2.2E- 5	1.1E- 5	4.5E- 5	5V, LET=60
	45 degrees	1	4.9E- 6			5V, LET=60
Lot:	U1H96	1	1.3E- 4			LET=60
	U1H58	1	1.2E- 4			LET=60
	U1H58	1	1.6E- 4			
	U1H80	3	1.7E- 4	1.5E- 4	1.9E- 4	
	U1H82	2	1.5E- 4	1.4E- 4	1.5E- 4	
	U1H83	2	1.4E- 4	1.1E- 4	1.6E- 4	
Size:	1.0 micron	1	2.0E- 5			5V
	1.0 micron	5	2.2E- 5	1.1E- 5	4.5E- 5	5V, LET=60
	1.2 micron	1	8.5E- 5			5V, LET=60
	1.0 micron	9	1.5E- 4	1.1E- 4	1.9E- 4	
	1.2 micron	1	1.2E- 4			
Bias:	5.5 V	9	1.5E- 4	1.1E- 4	1.9E- 4	
	5.0 V	1	2.0E- 5			
	4.5 V	1	4.0E- 7			
	5.0 V	5	2.2E- 5	1.1E- 5	4.5E- 5	LET=60
Temperature:	30 degrees	9	1.5E- 4	1.1E- 4	1.9E- 4	
	100 degrees	1	1.4E- 4			
Frequency:	2.5 MHz	5	2.2E- 5	1.1E- 5	4.5E- 5	5V, LET=60
	0.675 MHz	1	1.8E- 5			5V, LET=60
Pattern:	alternating	5	2.2E- 5	1.1E- 5	4.5E- 5	5V, LET=60
	all zeros	1	7.4E- 6			5V, LET=60
	all ones	1	1.6E- 5			5V, LET=60

Except where specifically noted in the "Parameter" or "Note" columns, the parameters are:
 Ion=Xe (LET=63), Angle=0 degrees, Lot=various, Size=1.0 micron, Bias=5.5V,
 Temperature= 30 degrees C., Frequency=2.5MHz, Pattern=alternating.
 Note: LET units are MeV per mg/cm².

is heavily doped so that all the applied field is already across the dielectric before the ion strike, in contrast to case of the MOSFET gate oxide.

Finally the bias dependence, shown in Figure 6, is remarkably strong, larger than that might be predicted based on Wrobel's work on measuring and modeling ion induced rupture in capacitor dielectrics [6]. The figures do not show sharply defined threshold conditions for either LET or bias as his model implies, but instead shows a probabilistic region where a given ion that hits a given biased antifuse may or may not cause SEDR. It is not due to the dynamics of exercising the part because similar probabilistic SEDR occurrence as a function of bias was seen in static investigations [2].

The sharp dropoff with lower bias seen in Figure 6 suggests that there would be no SEDR at 3.3 V, and this has been confirmed for gold with an LET of 80 MeV per mg/cm² to a fluence of greater than 10⁷ ions per cm². At large bias, there should be an asymptotic limit to the cross section when every ion that hits a biased antifuse causes a rupture so the cross section should approach the total area (in a time averaged sense) of biased antifuses. If the curve is rolling off at less than 10⁻³ cm² and given that each antifuse is about one square micron for the A1280A, the total number of biased antifuses can be estimated to be fewer than about 100,000 for the TMR test design, a reasonable fraction of the over 700,000 unprogrammed antifuses.

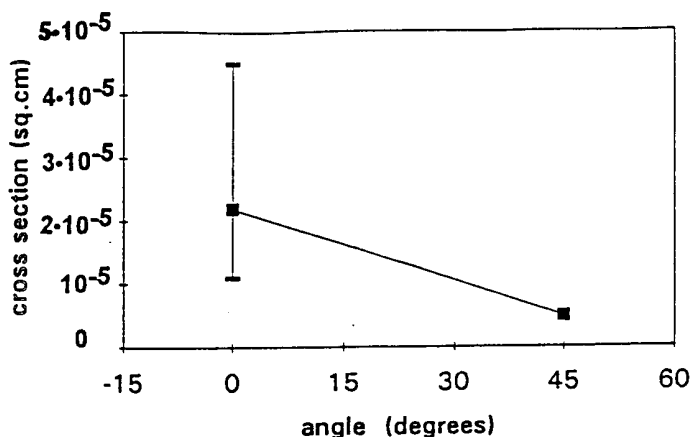


Figure 5 Angle dependence of SEDR susceptibility.

Also, the pattern dependence is explained, at least qualitatively, by the bias dependence. The alternating pattern biases the most unprogrammed antifuses and has the largest cross section. The fact that the all-ones pattern has almost the same cross section, while the all-zeros is significantly lower has a clear explanation: the ACT 2 routing algorithm used here preferentially grounds all routing segments with no programmed antifuses.

V. ALTERNATE EXPERIMENTAL APPROACHES

The present approach works reasonably well, taking advantage of the TMR design to maintain functionality even with several ruptured antifuses. However, better statistics and more accuracy in the counts of biased antifuses are desirable goals. One attempt at achieving those goals using A1280A (1.0 micron) devices turned on particular pass transistors so that essentially all the antifuses were biased with an external source applied to the Vpp pin. Unfortunately, in this mode, large susceptibilities to SEL and other (undiagnosed)

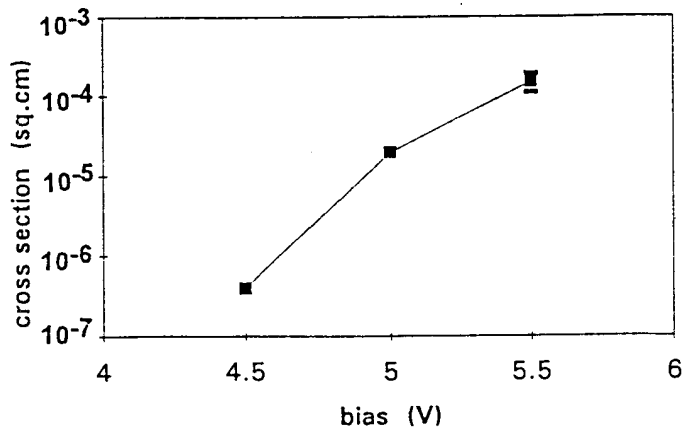


Figure 6. Bias dependence of SEDR susceptibility

problems interfered, making collection of SEDR data unreliable. (Note that SEL has not been observed during extensive irradiations for the A1280A in normal operation, implying that the susceptible area is only used during programming and debugging.) Biasing most of the antifuses by directly tying routing segments to rails has proven more successful, yielding results [2] consistent with those discussed here. Though this method requires the use of either the EMMI or current strip chart techniques to count the rupture sites, it is the preferred choice for future testing.

VI. CONCLUSIONS

Of the parameters investigated, only bias, normal LET, and angle exhibited strong enough effects to be considered significant, given the inherent statistical uncertainties. Susceptibility to SEDR increases rapidly with an ion's normally incident LET and with applied voltage. For a given ion and energy, susceptibility falls as incident angle deviates from perpendicular to the silicon surface. Other dependencies, if any, are more subtle.

Folding these dependencies into a calculation of the rate of SEDR in the 10% worst case GCR environment yields very low numbers: less than 3×10^{-5} per device-year for A1280-family devices and 7×10^{-6} for the A1020-family, assuming operation at or below 5.5V. Note two additional assumptions: that a fielded design has no more than 5 times the average number of biased antifuses relative to the test design and that the heaviest fractions of the GCR environment are known to within a factor of three [7]. Thus, one can conclude that, although the existence of this new heavy ion induced failure mechanism is somewhat disturbing, the increment in mission risk from SEDR is small. For example, the eight month Mars Pathfinder primary mission, which incorporates seventeen flight-critical A1280As in single-string mission-critical circuits, has a 99.96% chance of not experiencing a SEDR. Even this risk is probably overstated since the calculation assumes that any SEDR is fatal. However, the residual risk could be reduced significantly if it were deemed necessary, by lowering the operating voltage only 5-10%, although this would slightly increase the susceptibility to SEUs.

Evidence of SEDR was recently obtained for the A1460A, an Act 3-family device. Thus, these results apply to all feature sizes of all families of currently available, non-radiation hardened Actel devices, consistent with only small differences in the antifuse area. Interest in using these FPGAs in radiation environments is quite high. Thus, Phillips Laboratory has contracted with Loral to produce them using their radiation-hardened process. However, SEDR susceptibility would be essentially unchanged unless special steps (such as thickening the antifuse) are taken. As a consequence of this work, Actel and Loral have adopted strategies for SEDR hardening, and the reported oxide equivalent thickness of their first product is up to about 99 Å.

VII. REFERENCES

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