Nonvolatile and SDRAM Ferroelectric Memories for Space Applications

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***Abstract*--**A shunted ferroelectric memory cell has been designed for use in memories that are hardened to total ionizing dose and single event upset using hardened-by-design techniques. This approach eliminates the need for a radiation hardened CMOS process and allows for fabrication of the memories at a commercial ferroelectric semiconductor vendor. The memory cell is being used in two prototype designs, a 1-kbit nonvolatile ferroelectric memory prototype and a 4-Mbit synchronous DRAM prototype. Nonvolatile and DRAM behavior of the memory cell are controlled by using different internal programming voltages. Lower programming voltages allow the SDRAM to have higher endurance levels in trade for shorter retention times as compared to the nonvolatile ferroelectric memory. The ferroelectric memory capacitor in each memory cell is intrinsically resistant to radiation exposure. The success of hardening the CMOS circuitry by design techniques will be evaluated by investigating both memory types for performance and radiation hardness.

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1. INTRODUCTION

The availability of radiation hardened memories for space applications can be improved if the CMOS circuitry is hardened to radiation by design techniques as opposed to using specialty radiation hardened CMOS semiconductor processes. When CMOS circuitry hardened-by-design techniques[1,2] are used in combination with inherently radiation hardened ferroelectric storage capacitors,[3,4] semiconductor memories using ferroelectric storage capacitors can be designed as both nonvolatile memories and DRAM-type memories. These hardened-by-design memories are resistant to ionizing radiation as well as SEU and SEL events.

Hardened-by-design techniques have been used in the design of a prototype 4-Mbit synchronous DRAM (SDRAM) and a prototype 1-kbit nonvolatile FeRAM. Lower programming voltages on the SDRAM give higher endurance at the expense of shorter retention.[5] The SDRAM retention using the ferroelectric storage capacitor is expected to be orders of magnitude longer than a typical DRAM retention or refresh.

A shunted ferroelectric memory cell is used for both designs.[6] The shunted memory cell reduces the susceptibility to disturb and SEU and allows reduced programming voltages on the SDRAM because the plates of the ferroelectric memory storage capacitors are fixed at half the power supply voltage.

The intent of this program is to demonstrate the technology and design methodologies at lower cost on prototypes prior to designing and producing production radiation hardened memories. Both prototype products are targeted for broad space applications, including the JPL X2000 program.

Radiation hardened volatile and nonvolatile ferroelectric memories are well suited for space applications because the radiation hardness can be orders of magnitude better than Flash memory with no need for heavy shielding. In addition to superior radiation hardness, the ferroelectric memory provides very fast programming times, very high

endurance, and low power operation ideal for space applications.

2. SHUNTED MEMORY CELL

A shunted ferroelectric memory cell was selected for use in both the nonvolatile and SDRAM radiation hardened memories. A node internal to the memory cell and common to the pass transistor and the ferroelectric capacitor is connected to a local line via a shunt transistor (Figure 1). This local line periodically connects to the global plate line biased at the half-supply level. No additional area is consumed by the shunt transistor because it is formed under the ferroelectric capacitor (Figure 2).

The memory cell is destructively read by first turning off the shunt transistor (Figure 3). The pass transistor is then turned on, connecting the common internal node to a bit line. The precharge level of the bit line then biases the node, causing a voltage to develop across the electrodes of the ferroelectric capacitor. This voltage causes the capacitor to either switch to the opposite polarization state or stay in the same polarization state. The switched or non-switched charge is transferred through the pass transistor to the bit line, changing its voltage level. A sense amplifier drives the voltage of the bit line to the opposite logic level when switched charge is sensed, restoring the original state of the capacitor. Optionally, writing of a new logic state can occur at this point in the cycle.

In the SDRAM design, the half-supply voltage developed across the capacitor during restore or write increases endurance and reduces imprint, enabling the SDRAM architecture to serve higher endurance applications at a lower retention specification. In the nonvolatile design, higher retention with lower endurance is achieved by driving the plate line to the supply rails during restore and write in order to develop a full supply voltage level across the ferroelectric capacitor.

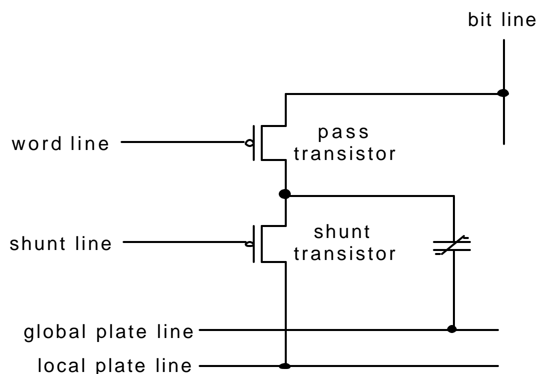

Figure 1. Circuit Schematic of Shunted Ferroelectric Memory Cell.

When deselected, the shunted memory cell holds the voltage across the ferroelectric capacitor near zero volts in the presence of noise coupling to the capacitor plates. Thus, susceptibility to disturb is reduced.

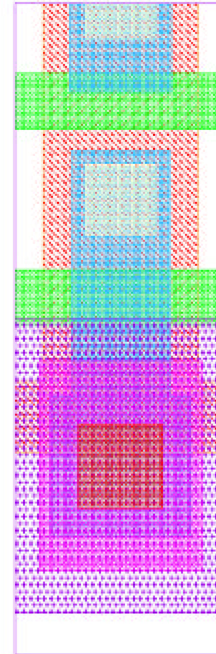

Figure 2. Layout of Shunted Ferroelectric Memory Cell.

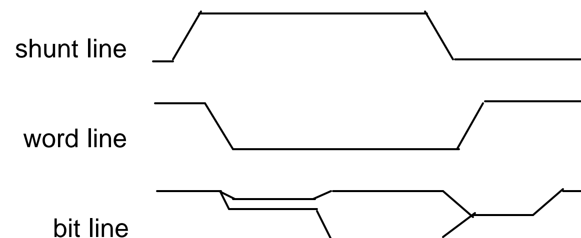

Figure 3. Read/Write Cycle Timing for Shunted Ferroelectric Memory Cell.

3. HARDENED FeRAM

A 1-kbit ferroelectric memory prototype has been designed to provide a test vehicle for evaluating radiation hardened nonvolatile ferroelectric memories for radiation tolerance and reliability. Read/write speed is comparable to that of a DRAM with the added feature that the

FeRAM provides nonvolatility. The test vehicle design provides flexibility for varying the operation of the memory array and for enhanced testability (Figure 4).

Commercial FeRAMs are being developed that use one transistor, one capacitor memory cells similar to those used in DRAMs. However, for space applications, a more rugged memory array architecture using a pair of memory cells with both true and complement bit lines is recommended. A radiation hardened sense circuitry design is used to avoid single event upset and latch-up.

FeRAMs designed for space applications are projected to have fast programming times of a few hundred nanoseconds. These fast programming times apply for the extended low temperature required for space applications (-55 °C). Lower power operation for FeRAMs is obtained because of the lower programming voltages and faster programming times, as compared to Flash memory.

Applications for FeRAMs hardened by design include system monitoring for recovery from safe modes, nonvolatile memory requiring faster programming times or higher endurance than provided by EEPROM or Flash memory, higher radiation tolerance than provided by Flash memory even with shielding, and where weight reduction by elimination of shielding of commercial parts is desired.

Completion of the radiation testing of the radiation hardened FeRAM prototype is expected in the first half of 2003. Pending successful testing, design of a multi-Mbit radiation hardened FeRAM is planned.

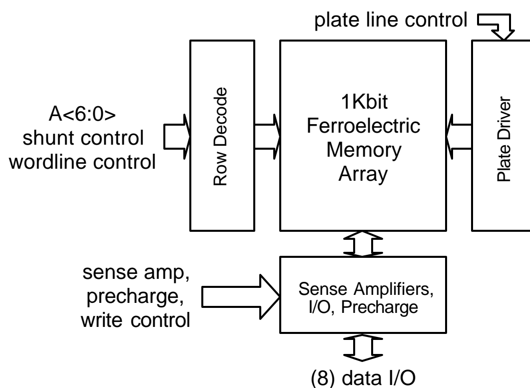

Figure 4. Nonvolatile FeRAM Architecture.

4. HARDENED SDRAM

A 4-Mbit synchronous DRAM (SDRAM) ferroelectric memory has been designed to provide an intermediate solution for both nonvolatile and volatile RAMs (Figure 5). By operating the ferroelectric memory at lower programming voltages than those used for nonvolatile ferroelectric memories, retention can be traded off against endurance providing high levels of endurance. Retention is anticipated to be at least one day and endurance is expected to be at least 10^{13}.

Ferroelectric SDRAMs hardened by design can provide COTS components to replace existing volatile memory in space systems where heavy shielding is currently required. Radiation and reliability testing of the 4-Mbit SDRAM prototype are expected to be completed in 2003.

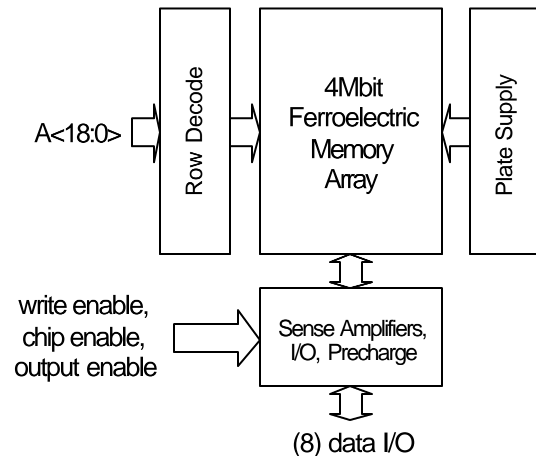

Figure 5. SDRAM Architecture.

5. SILICON FABRICATION

Hardened-by-design memories allow wafer fabrication in commercial silicon foundries, avoiding the expense and supply issues of obtaining radiation hardened memories using specialty radiation hardened semiconductor processing. The use of COTS components can become a reality.

Fujitsu, a semiconductor company that is supplying commercial products incorporating ferroelectric memory, is performing the wafer fabrication for the nonvolatile and SDRAM ferroelectric memories at 0.35 micron design rules. Development and production of these FeRAMs for space applications is expected to leverage off the commercial FeRAM activities. Both PZT (lead zirconium titanate) and SBT (strontium bismuth tantalate) can be used for the ferroelectric material, depending on the product specifications. Fujitsu uses PZT in its ferroelectric process.

6. RADIATION HARDNESS

Ferroelectric capacitors for use in ferroelectric memories, such as the nonvolatile and SDRAM memories being developed, are resistant to ionizing radiation.[3,4] Previous work has shown ferroelectric memories are resistant to SEU events[7] and proton irradiation[8] under unbiased conditions. The current program allows both the nonvolatile and SDRAM memories to be tested for SEU events and proton irradiation under biased operational conditions because the CMOS circuitry is hardened by design techniques.

7. CONCLUSIONS

A prototype ferroelectric 1-kbit FeRAM has been designed to show feasibility of combining radiation resistant ferroelectric memory storage with hardened-by-design CMOS to provide a COTS solution for nonvolatile memories for space applications. A 4-Mbit ferroelectric SDRAM has been designed to provide an intermediate COTS solution for volatile memory for space applications. Both memories use a shunted ferroelectric memory cell. The different modes of operation of the cell are attained by using different bias conditions for programming the memory cell. Both products can eliminate heavy shielding required for conventional memories.

First silicon is expected during the first quarter of 2003. Radiation testing is expected to be completed during the first half of 2003 and reliability testing of the SDRAM is expected to be completed in 2003.

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8. REFERENCES

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