

# High Density NDRO Ferroelectric Memory

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**Abstract**—Very high density ferroelectric memories using ferroelectric transistors for the memory storage devices are being developed. Memory cell sizes as small as  $4 F^2$  to  $10 F^2$ , where  $F$  is the minimum design rule feature size, are possible with this new technology. A ferroelectric material with a low dielectric permittivity allows appropriate programming voltages to be applied to the non-volatile ferroelectric transistor and provides for longer retention. A simple process flow using a fully encapsulated ferroelectric layer enables the memories to be manufactured on a CMOS process with aggressive design rules. By leap-frogging technology generations, FeRAMs of 128-Mbit and 256-Mbit densities may be possible within the next few years. By using a transistor for the memory storage device, non-destructive read-out (NDRO) is achieved. By combining the dense ferroelectric technology with hardened-by-design CMOS peripheral circuitry, very dense radiation hardened FeRAMs for space applications can become a reality.

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## 1. INTRODUCTION

Commercial ferroelectric memories are already in the marketplace. Their density is limited by the size of the ferroelectric memory cells obtainable with a select transistor in series with a ferroelectric capacitor. The size of

the ferroelectric capacitor and contacts to the ferroelectric capacitor limit the scaling of the memory cell and the achievable density of the memory.

Use of ferroelectric transistors instead of ferroelectric capacitors for the memory storage devices can provide much higher densities and non-destructive read out (NDRO) operation. However, development of a ferroelectric transistor that has a low programming voltage and sufficient retention has been elusive. Previously, ferroelectric switching currents for a ferroelectric material with a low dielectric permittivity were presented.<sup>1</sup> By using a low dielectric permittivity ferroelectric material, ferroelectric transistors can be fabricated with conventional dielectrics below the ferroelectric layer and still maintain sufficiently low programming voltages to polarize the ferroelectric layer during write operations. These conventional dielectrics also serve to increase the retention time.

Memory cell architectures and integrated process flows have been defined that give memory cell areas as small as  $4 F^2$  to  $10 F^2$ , where  $F$  is the minimum design rule feature size. A test chip containing the various architectures has been designed to evaluate the new technology.

Metal-ferroelectric-dielectric-silicon capacitors have been fabricated. C-V measurements on these devices indicate that the programming voltage goal of under 3 volts can be attained. Preliminary retention measurements indicate that retention may be orders of magnitude better than that observed in most other investigations.

## 2. FERROELECTRIC TRANSISTOR MEMORY CELLS

Several ferroelectric transistor memory cell architectures have been defined and are included on the test chip. Table I lists the estimated memory cell areas using buried bit line and conventional bit line architectures. The single

gate transistor memory cell consists of a single ferroelectric transistor. The dual-gate cell has a select transistor in series with the ferroelectric transistor on the source side, and the tri-gate cell has select transistors in series with the ferroelectric transistor on both the source and drain sides. The NAND cell has a series architecture similar to a NAND Flash memory. The dual bit line cell has true and complement bit lines for each memory cell, and is the easiest memory cell to operate electrically. The shared bit line cell is similar to the dual bit line cell except two adjacent columns share one bit line. All of the memory cell types can be fabricated with conventional implanted source/drains or with buried bit lines.

Table 1. Memory Cell Sizes by Architecture

Cell	Buried BL (F <sup>2</sup> )	Conventional BL (F <sup>2</sup> )
Single Gate	4	6
Dual Gate	16	8
Tri Gate	24	10
NAND	12	5
Dual Bit Line	8	8
Shared Bit Line	6	9

The smallest memory cell is obtained for the single gate device using buried bit lines that eliminate contact windows in the memory array. This is also the highest risk memory cell for electrical operation under write, write deselect, read and read deselect conditions. The larger memory cell architectures are lower risk with respect to electrical operation.

### 3. MEMORY ARRAY ARCHITECTURE

In the case of the single gate ferroelectric transistor memory cell, to obtain the smallest memory cell size, bit lines must be shared between adjacent memory cells and buried bit lines must be used. This requires that a bit line be used as the sense line during the read operation and the other shared bit line be used as a virtual ground.

The dual-gate and tri-gate structures allow the ferroelectric transistor to be isolated from one or both bit lines, respectively. This simplifies the electrical operation of the memory cell but adds area. The dual bit line architecture allows independent operation of all bit lines during the read operation.

The read operation is random access. Any bit in the memory array can be read with the appropriate deselect operation along the selected bit line and word line. Alternatively, an entire word line can be read into the sense amplifiers in parallel, providing the opportunity to quickly read multiple bytes of information. NAND read access is partially serial, similar to that of Flash memory.

Table 2 gives the programming sequence. All array architectures require all the bits in a row to be erased. This erase is not as restricted as the page or sector erase used for Flash memories. First, the data in a row are stored in latches connected to each bit line. Then the memory cells in the row are erased. The contents of the data in the latches are then updated as needed, and the contents of the latches for the entire row are programmed back into the row.

Except when programming, the potentials across the gate dielectric stacks of the ferroelectric transistors are near zero. A small voltage less than the coercive voltage is applied during the read operation and no voltage is applied otherwise.

Table 2. Programming Sequence

1. Store row contents in bit line latches
2. Erase row
3. Update data in bit line latches
4. Write bit line latch data into row

### 4. C-V CHARACTERIZATION

Prior to fabricating transistors, C-V analysis of MOS-type structures can be used to optimize the vertical gate stack for programming voltage and retention, and to estimate the threshold adjust implant required for fabricating transistors. Figure 1 shows the MOS type structure used for the testing.

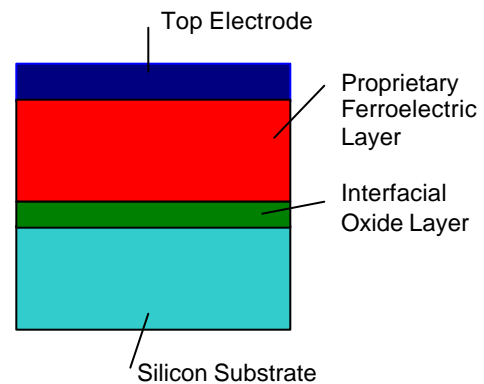


Figure 1. Cross Section of a ferroelectric capacitor used for the C-V measurements.

The C-V curves are generally reproducible for successive measurements. Figure 2 shows the reproducibility. Figure 3 shows C-V curves for different programming voltages. Using data similar to those shown in Figure 3 for different stack layer thicknesses, the memory window width versus programming voltage can be calculated, as

shown in Figure 4. It can be seen that the memory window width scales approximately linear with the dielectric stack thickness. To obtain programming voltages less than 5 V, a stack thickness under 50 nm is required. For samples with ferroelectric thicknesses around 35 nm and interfacial oxide thickness around 20 nm, breakdown voltage exceeds 20 V. This means that the dielectric stack may be scaled further.

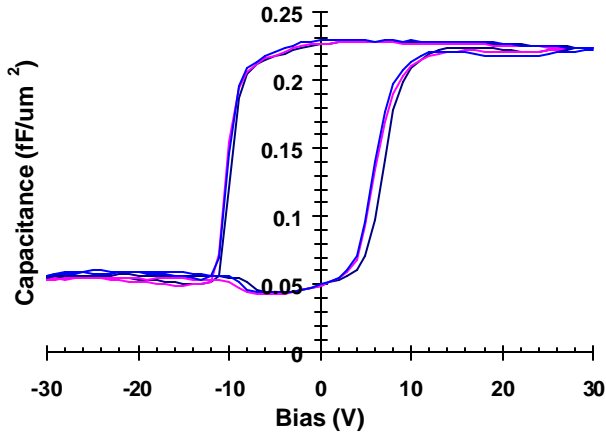


Figure 2. Reproducibility of C-V Curves. The curves were taken on successive voltage sweeps approximately 5 minutes apart.

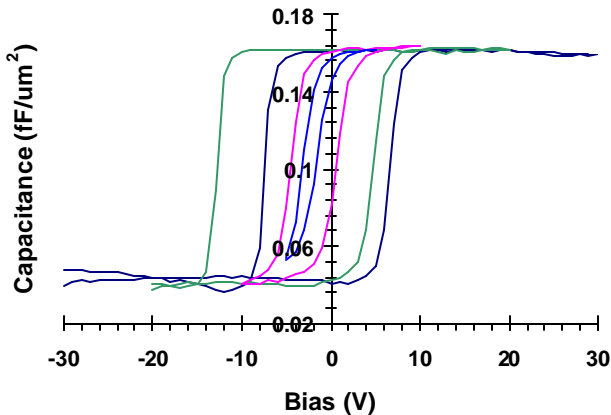


Figure 3. C-V Curves for 5, 10, 20, and 30V Programming Voltages.

The capacitor test structures have been characterized for room temperature retention. With the exception of one study,<sup>2</sup> most other investigations have shown ferroelectric transistors to have short room temperature retention, of the order of only a few hours. Preliminary data on the capacitor test structures of this study show that if the ferroelectric devices are not programmed to saturation, the retention time is short with decay of the memory window width in minutes or hours. However, if the ferroelectric devices are programmed to saturation, with the

exception of rapid depolarization to the remnant polarization common to all ferroelectric devices, no further decay in window width was observed at room temperature for over 72 hours. However, the memory window center was not observed to be absolutely stable. Measurements on ferroelectric transistors will be required to accurately assess the retention. No measurements have yet been performed with respect to endurance.

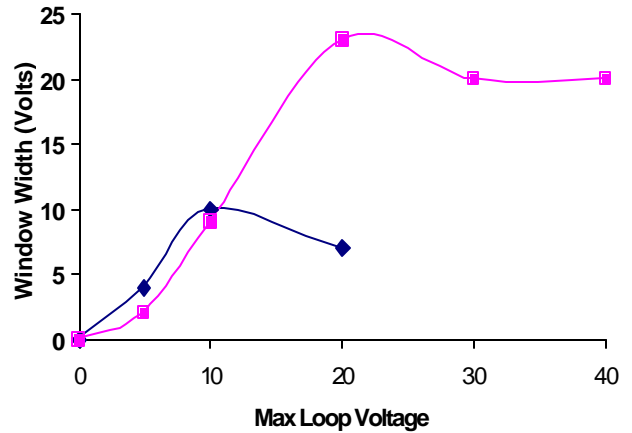


Figure 4. Memory Window Width versus Programming Voltage for Ferroelectric Capacitors of Different Thicknesses.

## 5. TEST CHIP and PROTOTYPE MEMORY

A test chip has been designed for demonstration of the technology. The test chip contains discrete test devices, process control structures, and small memory arrays for the various memory cell architectures. Table 3 lists the primary devices on the test chip. Fabrication of the test chip is planned to commence in the first calendar quarter of 2003.

Work has begun on the architecture for a 16-kbit prototype memory. Completion of this design is planned for the end of the third calendar quarter of 2003, with fabrication and characterization thereafter.

Table 3. Test Chip Devices

Discrete memory cells as listed in Table 1
Test ferroelectric capacitors
Large single plates
Arrays of small capacitors in parallel
8 x 8 memory arrays of memory cells as listed in Table 1
Ferroelectric process control structures
CMOS TEG
Variations in W/L for test chip devices
Control devices for comparison to ferroelectric devices

## 6. FABRICATION

An MOCVD deposition system has been developed for deposition of the low dielectric permittivity ferroelectric material and interfacial layers. The deposition uses flash evaporation of liquid chemical precursors. The deposition system is capable of depositions up to 800 °C on six-inch wafers. Typical deposition temperatures for the low dielectric permittivity ferroelectric materials are considerably lower. However, the high temperature capability of the deposition system allows in situ anneals of the ferroelectric layer. The ferroelectric layer forms the correct ferroelectric phase using a thermal anneal without the requirement for a rapid thermal anneal.

Thickness uniformity of the deposited ferroelectric layer has been demonstrated typically to be around 5% on the thinnest films, as shown in Figure 3. The average variation in thickness is approximately 3.4 nm independent of the film thickness, suggesting that the variation observed may be due in part to measurement inaccuracy.

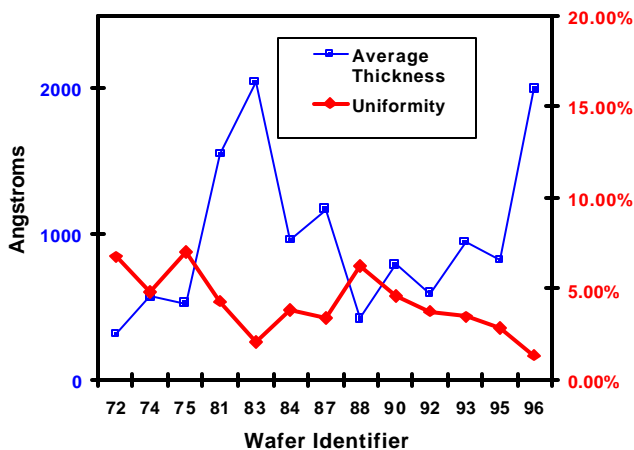


Figure 5. Thickness Uniformity of Dielectric Stack across Wafer.

Several process flows have been defined for the various memory cell architectures. These process flows provide full 100% encapsulation of the ferroelectric devices to eliminate contamination of the CMOS wafer processing facility. The encapsulation also is a hydrogen barrier to prevent degradation of the ferroelectric characteristics due to hydrogen exposure during subsequent processing steps. Some memory cell architectures use conventional sources and drains and others use buried bit lines. The architectures using buried bit lines have the advantage of reducing the etch requirements for the ferroelectric layer.

Unlike requirements for ferroelectric capacitor processes commonly used in today's ferroelectric memories, the buried bit line process flows for the ferroelectric transistors allow the ferroelectric memories to be processed at

aggressive design rules because the ferroelectric deposition and etch requirements do not limit the memory cell scaling, and contamination of the CMOS facility is not an issue with the full encapsulation. This provides the opportunity to fabricate very high density ferroelectric memories at design rules reserved for advanced DRAM and Flash memories. Initial commercialization of memories based on this technology is targeted for 128-256 Mbit. When combined with radiation hardened CMOS circuitry, very dense NDRO nonvolatile memories are possible.

## 7. CONCLUSIONS

Low dielectric permittivity ferroelectric materials in combination with new memory cell designs and integrated process flows are making dense NDRO nonvolatile semiconductor memories possible. Measurements on capacitor structures show that low programming voltages of the ferroelectric transistor storage devices are possible. Preliminary retention measurements show retention is not limited to just a few hours at room temperature. High endurance typical of ferroelectric layers is expected.

A MOCVD deposition system that gives good thickness uniformity across the wafer has been developed for the ferroelectric materials. Full encapsulation of the ferroelectric devices prevents contamination of CMOS wafer fabrication facilities and should allow the memories to be produced at leading edge design rules and densities.

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## 8. REFERENCES

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