

Tunneling Phenomenon in SuperFlash[®] Cell

A.Kotov, A.Levi, Yu.Tkachev, and V.Markov

Silicon Storage Technology Inc., 1171 Sonora Court, Sunnyvale, CA 94086, Tel. (408) 522-7350, akotov@sst.com

Abstract—An extensive investigation of interpoly oxide conduction (erase) mechanism for SuperFlash cell is presented. Single electron tunneling events have been detected, using regular flash memory cell. A physical model based on cylindrical approximation for the Fowler-Nordheim equation has been developed which shows good agreement with experimental data. The model includes two fitting parameters: SiO₂/poly-Si barrier height and average radius of curvature of the FG (Floating Gate) tunnel injector edge. Erase voltage distribution appears to be better described by modification of the SiO₂/poly-Si barrier rather than by process-related variations of the FG injector radius. In this paper the authors also present an accurate single cell technique for measuring coupling ratio (CR) concurrently with forward and reverse tunneling voltages between control and floating gates of the SuperFlash cell. As opposed to conventional techniques for the CR characterization, a new technique does not require a reference cell with contacted floating gate for CR measurement

developed approach of coupling ratio and tunneling *I-V* characteristic measurements directly on cell, without using non-floating gate test structures. By using new technique, we have studied *I-V* tunneling characteristics for the cells with different erase speed, which in turn allowed us to better understand the key parameters responsible for the erase distribution such as FG injector radius and barrier height. In this paper we have presented and verified tunnel model for the FG injector based on Fowler-Nordheim equation in cylindrical approximation.

2. EXPERIMENTAL AND RESULTS

2.1. Coupling ratio measurement

The SuperFlash memory cell is a split gate cell (Fig.1) which uses Fowler-Nordheim (F-N) Electron Injection from field-enhancing FG-injector through tunneling oxide during ERASE and Source-Side Channel Hot Electron Injection during PROGRAM [2,3].

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1. INTRODUCTION

As memory cell dimension is scaled down, new characterization techniques are required to make sure that individual cell characteristics are accessed and their degradation is negligible during measurement itself. Commonly used CR experimental methods are based on comparison between actual memory cell and dummy cell with contacted floating gate, assuming the same characteristics and dimensions for both cells [1]. The usage of the dummy cell can be a source of the errors because non-floating gate structure may not fully represent cell layout, and process-related cell-to-cell variations may further increase errors. We therefore

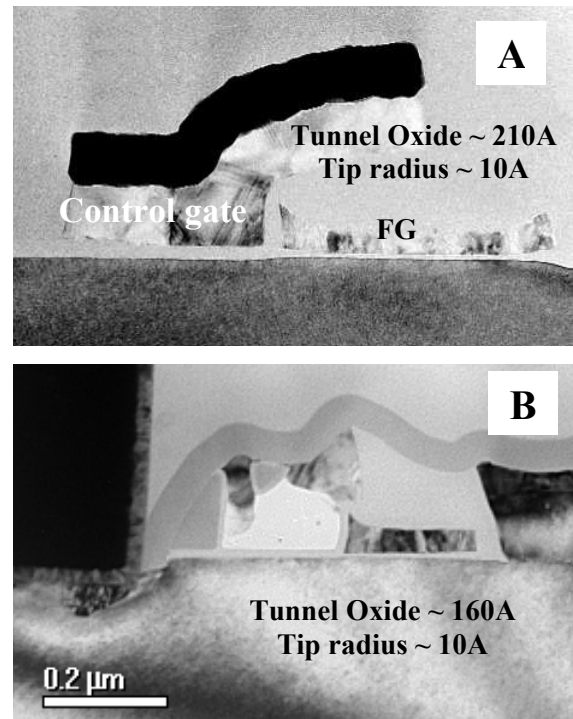


Fig.1. A: Split-gate 0.33µm SuperFlash memory cell. Cell area ~ 1.7µm². B: Self-aligned 0.25µm SuperFlash cell. Cell area 0.59µm².

The presented technique employs triangular voltage pulses applied to the control gate followed by measurements of threshold voltage as a function of stress voltage amplitude $V_t(V_e)$. The technique is based on the self-stabilization of the FG tunnel current when triangular or trapezoidal pulses are used for erase [4,5]. According to the capacitance-equivalent model of the cell, the interpoly voltage, V_{12} , during erase is given by

$$V_{12} = V_e - V_{FG} = (1 - CR) \cdot V_e(t) - Q_{FG}(t) / C_{tot}, \quad (1)$$

where CR is the coupling ratio between control and floating gates; $V_e = V_0 + \alpha t$ is the erase ramp voltage; Q_{FG} is the FG charge; and C_{tot} is the total FG capacitance.

As one can see from (1), the interpoly voltage increases proportionally to erase voltage till the onset of electron tunneling injection from FG. When tunneling conditions are reached, a corresponding positive change of the FG charge begins to slow down the interpoly voltage increase. If the amplitude of V_e is high enough, a steady state is reached in which the interpoly tunnel voltage and current remain constant till the end of ramp voltage pulse. Taking the derivation of both sides of Eq. 1, one can find the stabilized FG tunneling current

$$dV_{12}/dt = (1 - CR) \cdot \alpha - I_{FG}(t) / C_{tot} \rightarrow 0 \quad (2)$$

$$I_{FG} \rightarrow I_{FG}^{sat} = \alpha \cdot C_{tot} \cdot (1 - CR) \quad (3)$$

As can be seen from (3), the stabilized tunneling current is proportional to the ramp rate of erase pulse and, therefore, can be easily controlled externally.

Similar to the common (stacked-gate) cell the threshold voltage, V_t , is determined by FG charge as follows

$$V_t = V_{t0} - Q_{FG} / C_{12} = V_{t0} - Q_{FG} / (C_{tot} \cdot CR), \quad (4)$$

where V_{t0} is cell's threshold voltage with FG in the neutral state; C_{12} is interpoly capacitance. Note that formula (4) is not applicable for split gate cell in deep erase state, since threshold voltage for erased cell is governed by control gate rather than by the charge state of the FG.

So, FG current can be also derived from (4) taking derivation of both sides

$$I_{FG} = -C_{tot} \cdot CR \cdot dV_t/dt \quad (5)$$

Combining (3) and (5) yields

$$CR = \alpha / (\alpha - dV_t/dt) = 1 / (1 - dV_t/dV_e) \quad (6)$$

Note that formula (6) is valid when the tunneling current reaches its saturation value, see (3). From that moment V_t vs. V_e data should be in linear relationship. However, V_t vs. V_e curve for split gate cell deviates from straight line for higher V_e (when $V_t < V_{t0}$), and finally saturates at threshold voltage of the control gate. For correct calculation of CR it is necessary to extract the maximum slope of the V_t - V_e data, as shown in Fig.2.

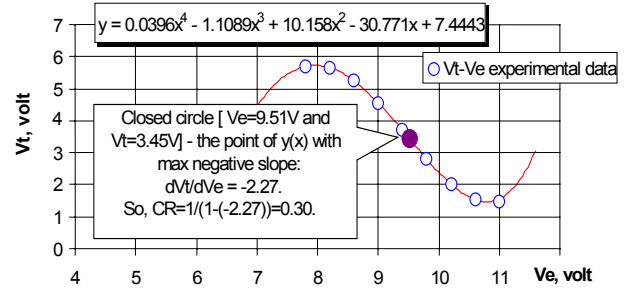


Fig.2. V_t - V_e data are approximated by 4-th order polynomial trendline for CR extraction. Erase ramp rate 1MV/s.

2.2. Forward tunneling

According to the analysis presented in the section 2.1 the interpoly tunnel current, I_{FG} , tends to saturate under the conditions of measurement. The saturated value of I_{FG} is given by (3). The value of total FG capacitance found from TEM and simulation data equals $C_{tot} = 1.2 \pm 0.1$ fF for 0.33 μm cell. The interpoly voltage, which corresponds to saturation value of I_{FG} , is extracted using V_t^* and V_e^* values, which correspond to the maximum slope point on the $V_t(V_e)$ polynomial trendline, and CR . Combining (1) and (4) results in:

$$V_{12} = (1 - CR) \cdot V_e^* + CR \cdot (V_t^* - V_{t0}) \quad (7)$$

To verify the capability of the method to cover broad range of CR and V_{12} parameters, 27 cells with intentionally different dimensions from 9 different wafers were taken for the measurements. The results of three consecutive measurement runs are presented in Fig.3.

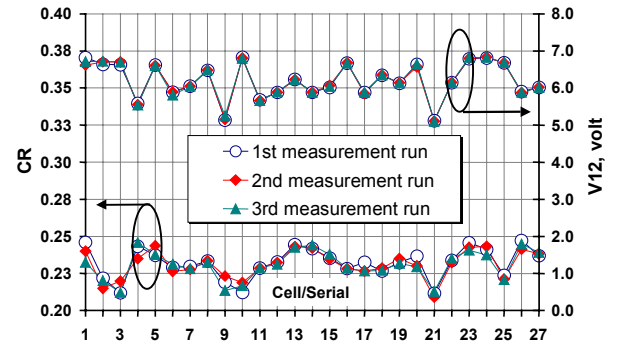


Fig.3. Reproducibility of CR and V_{12} data measured in three consecutive runs for 27 cells.

The CR and V_{12} data obtained using this technique show very good reproducibility. The closeness of agreement between successive measurements also means that no noticeable cell degradation is produced by the method itself. This allows one to extract tunneling I - V data in a wide range of current. Fig.4 shows tunnel I - V characteristics measured on fresh and cycled cell in a

wide range of current ($2 \cdot 10^{-18}$ – $2.5 \cdot 10^{-12}$ A) by changing erase ramp rate from 2.3mV/s to 3kV/s.

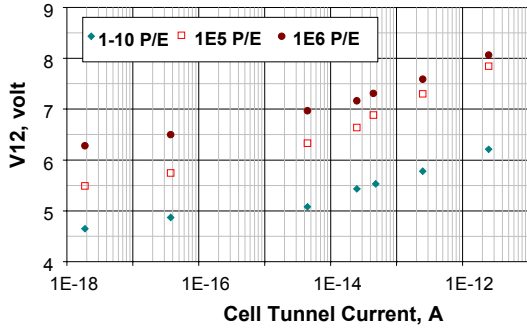


Fig.4. I - V characteristics of tunnel injector before and after program/erase (P/E) cycling.

The lower limit of measurable current is determined by external voltage ramp rate (that is, by researcher's patience) rather than by the technique itself. One can see that cell tunneling I - V characteristics are shifted in almost parallel manner towards higher voltage after million P/E cycles, showing no indication of stress-induced low field leakage current. The lower average oxide field (~ 4 MV/cm) and significantly shorter time used for erase in SuperFlash cell as compared to stacked-gate cells, reduce the endurance-related data retention failure rate. In fact, we have never observed charge loss through tunneling oxide caused by erase cycling.

2.3. Reverse tunneling

In order to meet stringent reliability and program disturb requirements imposed by tunneling oxide scaling it is very important to optimize reverse tunneling characteristics in line with forward tunneling ones. Reverse tunneling voltage can be found on similar way as presented in sections 2.1 and 2.2, by using negative ramp voltage pulses applied to the control gate. If gate voltage amplitude is high enough then floating gate gains negative charge via interpoly dielectric conductance.

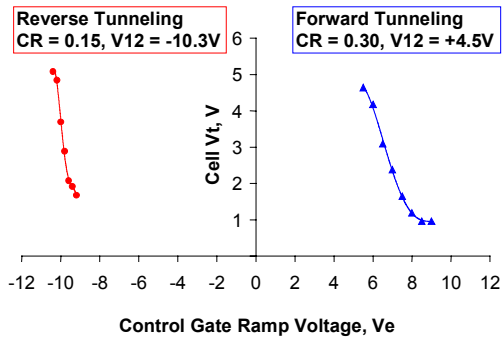


Fig.5. Reverse and Forward V_t - V_e characteristics. $0.25 \mu\text{m}$ self-aligned cell.

Figure 5 shows bipolar $V_t(V_e)$ characteristics measured for $0.25 \mu\text{m}$ self-aligned cell with 160\AA tunneling oxide. Calculated reverse tunneling voltage (-10.3V) significantly exceeds forward tunneling voltage (4.5V), delivering a striking example of the tunneling enhancement by FG-tip over planar injector. The coupling ratio also demonstrates asymmetrical behavior, being essentially lower in reverse mode under negative gate voltage compared to that one during forward measurement mode. The difference is probably due to FG depletion induced at the FG bottom under positive gate voltage.

2.4. Tunneling Model for FG injector

To simulate tunneling I - V characteristics of the FG injector we used a cylindrical geometry approximation for cathode (floating gate injector) and anode (control gate). For poly-Si/SiO₂ barrier the one-dimensional (1-D) F-N current (in Amperes) is given by:

$$I_{FN} = S_i \cdot A \cdot \left(\frac{3.2}{\Phi_B} \right) \cdot E_C^2 \cdot \exp \left[\frac{-B}{E_C} \cdot \left(\frac{\Phi_B}{3.2} \right)^{3/2} \right], \quad (8)$$

where S_i is a cathode injecting area (cm^2), $A=1.15 \cdot 10^{-6} \text{ A/V}^2$ and $B=2.54 \cdot 10^8 \text{ V/cm}$ at room temperature; E_C is electric field at the cathode surface (V/cm); Φ_B is the energy barrier at poly-Si/SiO₂ interface (eV).

According to the analysis given in [1, p.163], the 1-D F-N formula (8) can be adapted for the cylindrical coordinates (emission from an edge) if the cathode field is substituted by the following effective field:

$$E_{EFF} = \frac{V_{12} - [0.34 \cdot \Phi_B \cdot \ln(1 + T_{OX}/R_C)]}{R_C \cdot \ln(1 + T_{OX}/R_C)}, \quad (9)$$

where V_{12} is the interpoly tunneling voltage; T_{OX} is the interpoly oxide thickness, and R_C is the average radius of FG-injector curvature. The injecting area in this case equals $S_i \approx \pi/2 \cdot R_C \cdot L_C$, where L_C is the FG injector length.

I - V Model (8,9) contains two main process-sensitive physical parameters: barrier height Φ_B and injector radius R_C . It is known [1, 7] that FG doping, grain size and orientation along the FG-injector as well as a means of interpoly oxide formation can strongly affect the FG-injector barrier height.

First let us consider a role of radius R_C in simulating the tunneling I - V characteristics for cells with quite different erase voltage. Fixing Φ_B at different levels in reasonable range (2.4-3.6 eV) [1, pp.122-126], we used R_C as the only fitting parameter. Figure 6 shows an unsuccessful example of this kind of simulation at $\Phi_B=3.0\text{eV}$. For any other fixed Φ_B the model was also failed to adequately interpret the tunneling characteristics of these cells.

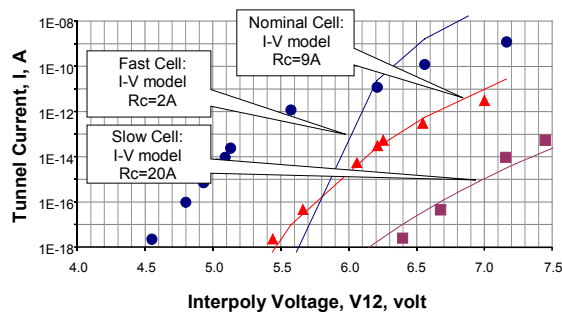


Fig.6. Experimental I-V characteristics of tunnel injector for fast, nominal, and slow-erased cells and simulation results at fixed FG-tip barrier 3.0eV: one fitting parameter – tip radius.

In our opinion, the dispersion of tunneling characteristics can hardly be associated with R_C variations for very small injector radius. We believe that in this case quantum effects should be taken into account. Indeed, the physical tip curvature achieved in SuperFlash cell ($<10 \text{ \AA}$, see Fig.8) is well below electron's de Broglie wavelength in silicon, which is in the range of 50-100 \AA at room temperature. In this case one should expect that accumulation layer, which is the actual injecting surface formed in FG during erase, is quantized and its centroid is located some distance away from the tip surface (see [6] for example). The accurate quantum-mechanical modeling of accumulation layer in FG injector is beyond the framework of the present paper. Here we merely hold to the idea that the quantization increases the effective R_C value and smoothes out the injector curvature non-uniformities. Thus, cell-to-cell variations of R_C become not so critical for V_e distribution and barrier height begins to play a dominant role.

We actually managed to obtain good agreement with experimental data using Φ_B as a fitting parameter while keeping R_C at a constant value 14.5 \AA (see Fig.7).

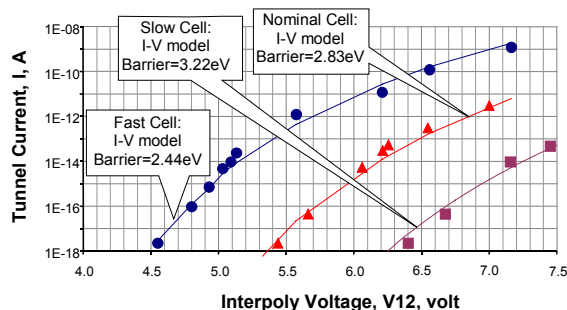


Fig.7. Experimental I-V characteristics of tunnel injector for fast, nominal, and slow-erased cells and simulation results at fixed tip radius $R_C=14.5\text{\AA}$: one fitting parameter – FG-tip barrier height.

We also found that simple cylindrical tunneling model, based on the barrier height variation at the FG tip from 2.4eV to 3.3eV, can successfully describe the whole V_e -distribution measured on 4Mb devices.

Since we believe that the fundamental limit for R_C is already achieved (see Fig.8), then only two parameters (T_{OX} and Φ_B) can be used for further erase voltage scaling.

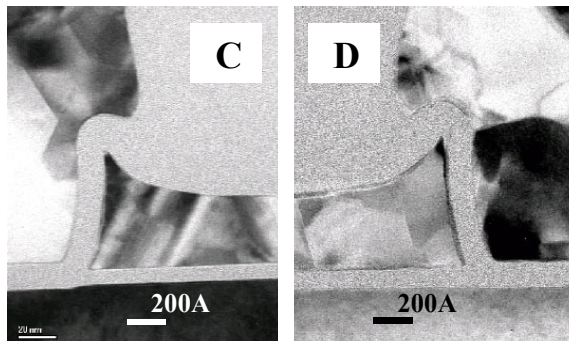


Fig.8. Actual FG-injector radius appears to be below 10 \AA for both C and D cells with and without extra FG implant accordingly.

To demonstrate the possibility of V_e decrease due to barrier modification, the cells with different FG doping were fabricated and characterized. Figure 9 shows drastic reduction of the forward tunneling voltage by about 1.5V (25%) for the cell with extra FG implant as compared to the cell without additional FG implant, while tip sharpness looks pretty much the same (compare C and D cells in Fig.8). Reverse tunneling characteristics for both cells show no noticeable difference, thus pointing out to the same interpoly oxide thickness.

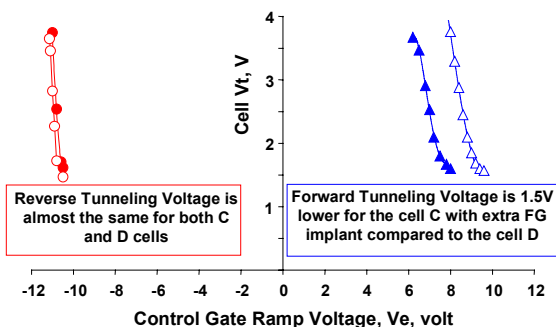


Fig.9. Reverse and forward tunneling characteristics for C and D cells with different FG doping.

2.5. Single Electron Event

We have recently found out that single electron tunneling events can be detected in SuperFlash split gate cell, when the cell is being erased and read simultaneously. This is realized by monitoring subthreshold current of a programmed cell using increased control gate voltage, V_{cg} , which is high enough (4-6V) to give rise to FG

charge change driven by extremely low tunneling current ($<10^{-19}$ A). Drain voltage is kept at ~ 0.1 V.

The typical behavior of cell current with time is shown in Fig.10. Note the "staircase" pattern of current change, where each step corresponds to single electron tunneling event. It can be shown that the magnitude of a current step, induced by single electron change of FG charge can be expressed as

$$\Delta I_d = \frac{eS}{C_{12}}, \quad (10)$$

where S is the slope of I_d-V_{cg} curve at the point, corresponding to the initial cell current; e is elementary charge. From ΔI_d and S values one can find interpoly capacitance C_{12} . For $0.25 \mu\text{m}$ cell the C_{12} value obtained with single electron event technique was found to be about $1.1 \cdot 10^{-16}$ F, which is in a good agreement with simulation data.

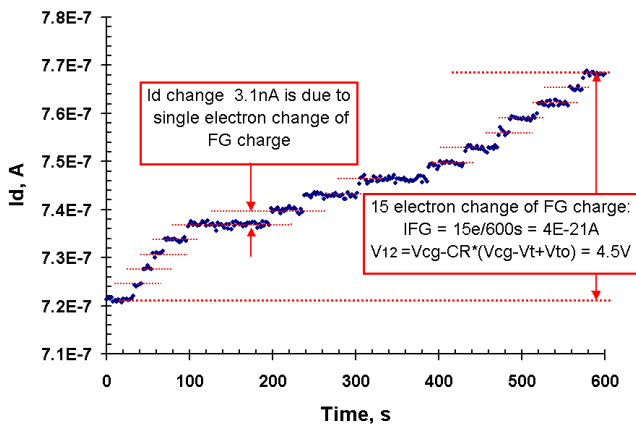


Fig.10. Typical behavior of cell current vs. time demonstrating single electron tunneling events. Measurement conditions: $V_{cg}=5.3$ V; $V_d=0.1$ V. Sampling interval – 2s.

Using this single electron technique we managed to achieve the record sensitivity in injector tunneling current measurements – 1 electron in several hours, which corresponds to the tunneling current level of about 10^{-23} A. The details of measurement technique and experimental results will be published soon.

3. CONCLUSIONS

An accurate technique for measuring coupling ratio along with forward and reverse tunneling voltages between control and floating gates of the SuperFlash cell has been developed. Using this new technique I-V tunneling characteristics for FG injector has been measured on fresh cells and cells subjected to 1million program/erase cycles. No indication of stress-induced low field leakage current has been found for the tunneling oxide. The field enhancing tunneling injector cell uses relatively thick charge transfer tunneling oxides, compared with other

E^2 PROM or flash EEPROM cells; therefore, intrinsic data retention is robust.

We also demonstrated that erase voltage distribution could be explained by cell-to-cell variation of the $\text{SiO}_2/\text{poly-Si}$ barrier at the FG-tip. A physical model based on cylindrical approximation for the FG injector and F-N equation has been developed which shows a good agreement with experimental data. Erase speed improvement for heavily doped FG-tip via reduced forward tunneling voltage has been demonstrated.

Single electron tunneling events were detected in SuperFlash cells using combined read-erase technique. This method can be used for determination of interpoly capacitance, extraction of tunneling injector I-V characteristics in extremely low current range (down to $\text{sub-}10^{-23}$ A) and for read-disturb analysis.

4. ACKNOWLEDGEMENTS

We would like to thank Dr. Ken Su for the TEM analysis, Dr. Sohrab Kianian, and Dr. Yuniarto Widjaja for many valuable inputs.

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Alexander Kotov received the M. S. degree in semiconductor physics from Moscow Institute of Physics and Technology in 1981.

In 1981 he joined Kiev Institute of Micro Devices, Ukraine, where he engaged in advanced CCD, EEPROM, CMOS technology development. From 1995 to 1997 he was a member of the technical staff at the Angstrom, Co., Moscow, Russia. He contributed in the area of 1.2- and 0.8- μm FLOTOX embedded memory technology. He is presently Reliability Physics Manager at the Silicon Storage Technology, Inc., Sunnyvale, California, working on advanced SuperFlash technology.



Viktor Markov received the M. S. degree in electronics from the Moscow Institute of Physics and Technology in 1981. From 1981 to 1999, he worked as process integration and research engineer in the area of CMOS NV memory at the institute of Micro Devices, Kiev, Ukraine.

In 2000, he joined SST as a member of Reliability Physics Group working on reliability analysis and reliability prediction methodology for SuperFlash memory devices. His current research interests include retention, endurance and performance stability of flash memory.



Amitay Levi received his Master's degree in Physics in 1979 and his Ph.D. in Material Science in 1985, both from the Hebrew University of Jerusalem. In 1985 he joined Xicor, Inc. and worked on process integration of EEPROM technology. In 1990 he joined Silicon Storage Technology, Inc. He has since been responsible for the development

of a few generations of the SuperFlash technology. Currently he is serving as the Vice President for Advanced Development.



Yuri Tkachev received the M.S. degree in electrical engineering from Moscow Institute of Electronic Engineering, Moscow, Russia, in 1983.

From 1983 to 1987 he worked as Research Engineer at the Institute of Micro Devices, Kiev, Ukraine, developing CMOS and MNOS

EEPROM technology.

From 1987 to 1994 he was with the Institute of Semiconductor Physics, National Academy of Sciences, Kiev, Ukraine, where he was engaged in research on radiation effects in MOS devices.

During 1994-2001 he was Researcher and Principal Engineer at Kvazar-IPAN R&D Company, Kiev, Ukraine, where he worked on ZMR SOI technology and silicon charged-particle detectors.

He joined SST, Sunnyvale, CA in 2001 as a Staff Engineer and is currently involved with the electrical characterization and reliability analysis of SuperFlash memory cells.