Reliability and Endurance of FRAM: A case study

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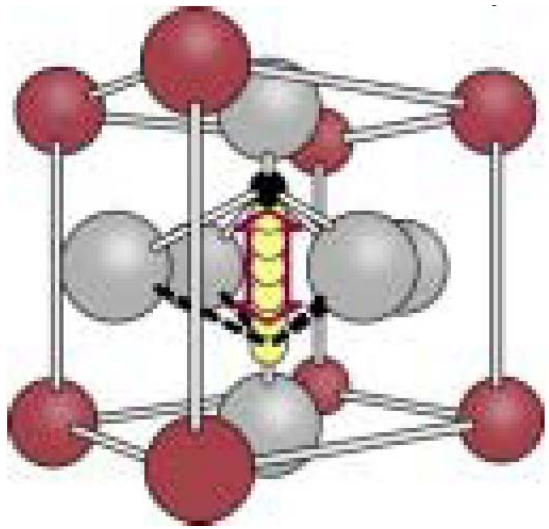
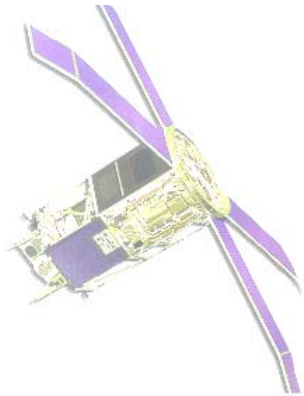


Outline

1. Motivation
2. FRAM Refresher
3. Reliability/Testing Issues
4. Test-bed Implementation
5. Test Methodology
6. Test Procedures and Current Results
7. Concluding Remarks

Motivation

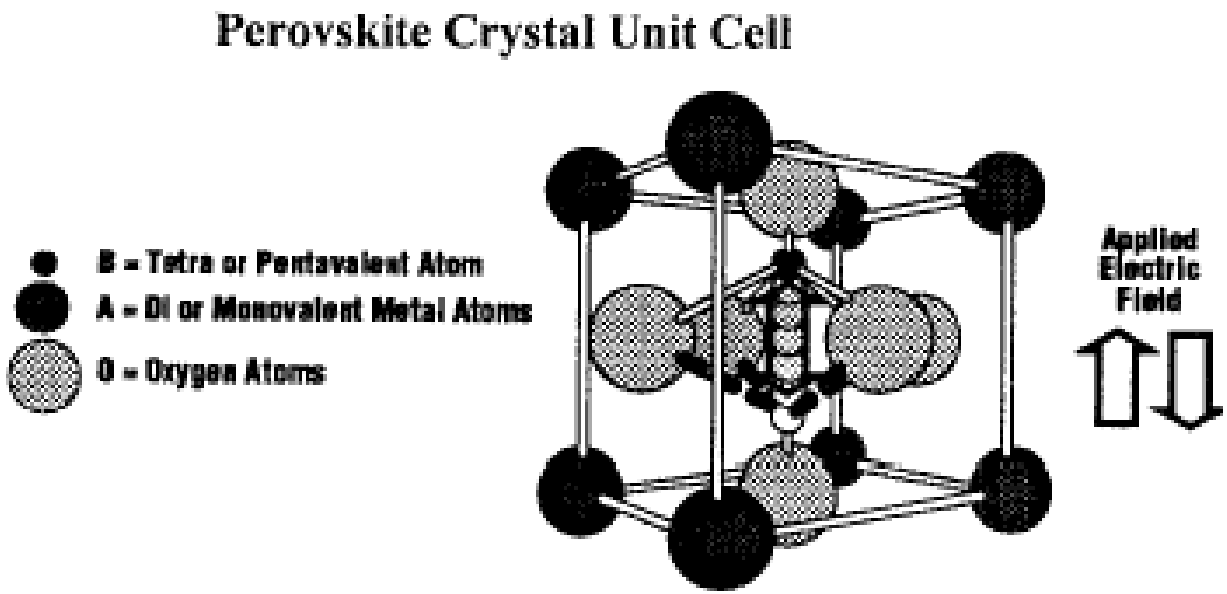


- NASA/JPL space missions exhibit needs for:
  - Fast read and write times (e.g. high computing performance)
  - High endurance and reliability (e.g. long-term missions)
  - High resistance to extreme temperature conditions
  - High resistance to radiation (e.g. deep space missions)
- FRAM Characteristics
  - Fast read and write times (~SRAM speeds)
  - High endurance and reliability ratings
  - High resistance to extreme temperature conditions
  - High resistance to radiation
- Existing endurance and reliability testing is costly

FRAM Refresher

Ferroelectric Random Access Memory (FRAM)

- Ferroelectric effect used as storage mechanism (vs. floating-gate found in EEPROM)
- SRAM-speed writes and reads
- Non-volatile storage with high endurance and reliability ratings



Ramtron Products

Ramtron FRAM Parallel Product Family

Product	Density/ Organization	Access Time	Read/Write Endurance	Operating Temp	Pkg
FM1208	4K(512x8)	200ns	10^{10}	-40 to +85°C	24 pin Dip/ SOIC
FM1218	4K(512x8) + ROM Addressing	200ns	10^{10}	-40 to +85°C	24 pin Dip/ SOIC
FM1608	64K(8192x8)	250ns	10^{10}	-40 to +85°C	28 pin Dip/ SOIC

Ramtron FRAM Serial Product

Product	Density/ Organization	Bus	Freq- uency	Read/ Write Endur	Oper Temp	Pkg
FM24C04	4K(512x8)	I^2C	400KHz	10^{10}	-40 to +85°C	8 pin Mini Dip/ SOIC

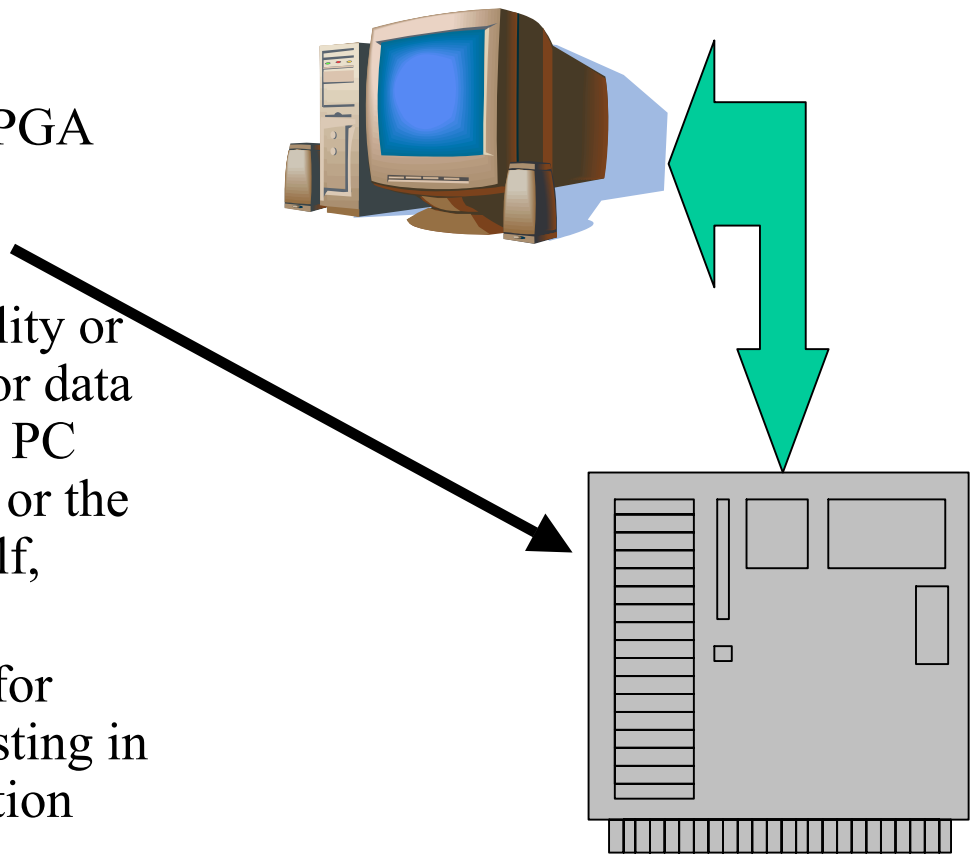
Reliability/Testing Issues of FRAM

Non-fabrication related issues of FRAM reliability

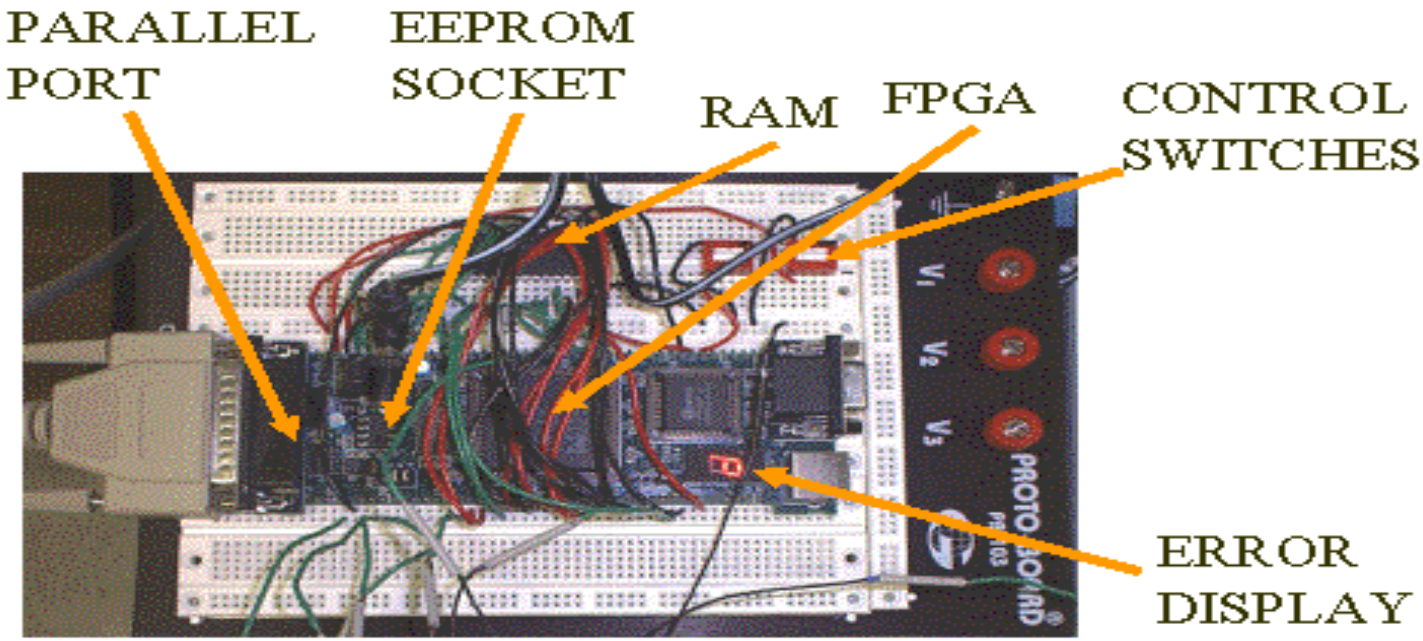
- Data retention endurance
- Fatigue
- Aging
- Imprint
- Radiation (TID) on underlying electronics (CMOS)

Test Bench Design

- Low-cost off-the-shelf FPGA evaluation board
- Low-complexity
- Useful to perform reliability or endurance tests. The error data can either be logged on a PC through the parallel port, or the tester can be used by itself, independent of a PC.
- Highly portable/flexible for extreme environments testing in cryo-chambers and radiation testing



Test Bench Details



RAM - Tested FRAM (FM24C04 or FM1808)

FPGA - XILINX XC4010E 10,000 gate, 5/3.3 V FPGA

Parallel port - For optional tandem PC error logging operations

EEPROM - For independent PC operation

Reliability and Endurance Tests

- MATS+ test used to test reliability and endurance
- Brief example using Van de Goor's memory test notation:

UP(W10101010; R; W01010101)

– *UP* = Perform the entire set of operations in parentheses from the first memory address to the last

– *W10101010* = Write the data pattern '10101010'

– *R* = Read back the data

– *W01010101* = Write the data pattern 01010101

– (Increment address and loop)

Reliability Test

- The MATS+ reliability test can detect address decoder faults and stuck-at faults, and was programmed to cycle through all the addresses in the memory.
- This reliability test was chosen because it met the minimum test criteria while fitting into the relatively small FPGA. Again using Van de Goor's notation, the MATS+ test is described as follows:

1. *UP(W01010101)*
2. *UP(R; W10101010)*
3. *DOWN(R; W01010101)*
4. *LOOP BACK TO (2)*

Endurance Test

- For the endurance test the following method was used:

  1. *(W01010101; R; W10101010; R)*
  2. *LOOP BACK TO (1)*

- Because testing all the addresses would have been prohibitively long, only one address was tested

Current Results

Memory	Status	# R/W Cycles (Endurance)		Endurance Specification
		NVMTS 2001	NVMTS 2002	
Ramtron Serial FRAM (FM24C04)	Test bed complete: Both tests running	1.058E10	7.08E10	1E10
Ramtron Parallel FRAM (FM1808)	Test bed complete: Both tests running	N/A	9.49E10	1E10

Conclusion and Future Outlooks

- Reliability and endurance of two FRAM chips currently available has been tested
  - Results have exceeded the manufacturer's ratings
- The test bench used for this case study is low in complexity and cost
- Further testing for more FRAM chips are possible on our test bench with minimal effort
- Further tests to undergo accelerated aging by heating and high voltage testing for data retention
- Radiation testing
- Additional reliability testing using a larger FPGA