Description and Reliability of a Robust 0.18 micron Low-Voltage and Low-Power Embedded Flash Technology

Ata R. Khan, Naresh Tandan.
Philips Semiconductors, 811 E. Arques Ave. Sunnyvale, CA 94086. ata.khan@philips.com

Abstract:

Philips Semiconductors has developed a 0.18u, triple-well, embedded Flash technology. The basic technology uses a 2T cell, FN-FN program/erase, on-chip charge pumps for Program/erase voltage generation and operates over a 1.2 to 2V range (read). Design techniques, the flash cell and the process are optimized to produce a robust product with high endurance over a wide range of operating conditions. Program/Erase voltage condition of selected and un-selected cells are optimized for robustness. Extensive reliability studies have been performed and data will be presented to show performance meets expectations in such critical areas as Bit Disturb characteristics, Endurance, and Data retention. The system advantages of this approach, applications and future technology paths are briefly described.

Strategic requirements for Embedded Flash

Embedded Non-volatile memories have seen tremendous growth in the last decade, becoming ubiquitous and synonymous with Microcontrollers. As on-chip memory sizes have increased, Embedded programs have become more complex and prone to revisions to correct errors and add features; these must be done in situ because the cost of doing field upgrades is usually prohibitive. These trends have forced the Industry to move to on-chip Flash from EPROM rapidly and will cause on-chip Flash to become a standard feature in Microcontrollers.

Customer and System needs for Embedded Flash

The main driver for Embedded Flash is, as usual, Cost. But not just the Cost of acquisition, it is the total ownership Cost which includes factors such as Lifetime Reliability, Endurance in Write/Erase Cycles, Area efficiency, Programming Time, Erase Time, Power Consumption, Operating Voltage Range, Performance, Yields, etc. etc. Optimising all these is a complex problem as many of these work against one another. In general, customers want all factors optimized.

System and Technology trade-offs

Another major trade-off area is in how to integrate Embedded Flash with existing Libraries and Processes. Generally, Flash technology lags a generation or so behind state-of-the-art Digital Logic processes and, for Embedded Flash Technology, it is vital that full Library compatibility be maintained with both Digital and Mixed-Signal Blocks. Given the expense of building new libraries, this drives the addition of the Flash Process steps to an existing Logic Process; this is usually more expensive in terms of masks than adding Logic to Stand-alone Flash but the end result is a library, Process, and Design Flow compatible technology which was the route we chose. Other major decisions that were made after considerable analysis were:

a. The basic Flash Cell Design: Weighing requirements for Low power, Endurance, Reliability, and after a Risk analysis, it was decided to use a 2-T Flash cell. The rationale will be explained in some detail later. The cell consists of a Stacked gate transistor with a series Access transistor with Source side access. It is larger than a 1-T Cell but there are some mitigating factors in the reduced size of the Charge Pumps and overhead required that compensate to some extent for the area increase. We believe that the reliability and robustness advantages over a 1-T cell are vital for many Embedded Applications where the Cost of Technology failure is very high, both from a cost and a safety point of view. Another reason for choosing a 2-T cell was the possibility of adding EEPROM functionality without any process impact. This FN-FN Cell has excellent reliability characteristics, and the very low Write and Erase currents allow a great degree of parallelism in programming and erasing which results in average program and erase times as fast as CHE-FN at a System Level.

b. Redundancy, Trimming, and Error Correction: It was decided to use Row Redundancy with the information stored in Flash at Wafer Sort to maximize yields. In addition, the High Voltage outputs of the Charge Pump are also measured and trimming values stored in Flash to optimize Cell and Sense Amp Operations. Since this is a new technology, and because it was felt to be extremely important to have a Reliable and Robust Flash Cell, 8 bits of Hamming ECC are appended to 128-bit word organized memory to allow single-bit error correction.

Technology Description

With the decisions and trade-offs considered earlier, what resulted was a 0.18u, triple-well, embedded Flash technology. The basic technology uses a 2T cell, FN-FN program/erase, on-chip charge pumps for Program/erase voltage generation and operates over a 1.2 to 2V range (read). Five or Six layers of metal are used along with a Local Interconnect Layer. The cell Size is 0.78 square microns and resulting access times, which vary a lot with array size and VDD range, are typically in the 50 nanosecond range. A diagram of the cell is shown in Figure 1, and the Read, Program, and Erase Voltages are shown in Figure 2. The Charge Pumps are turned on and off under User Program Control and a Programming Interface has been defined to allow the Application to Control pre-writing to the Row Data Latches before the actual Flash Programming is invoked (an entire Row can be programmed simultaneously; as an instance this could be 4K bits), to write-protect and to un-protect Sector write status thus minimizing the possibility of erroneously executed Code causing unwanted Sector changes and to prevent Power Supply failures from altering Sector contents (other than the one being written to).

Rationale for Robustness

Several advantages result from the 2-T Cell approach :

1. Uniform channel FN Tunneling is used for Write and Erase. No biased junctions are present under floating gates thus greatly reducing hole injection into tunnel oxides, improving Retention as well as Stress Induced Leakage Current-related endurance.

2. The 2-T does not require Pre-erase programming as mainstream 1-T NOR Flash memories do. This considerably reduces overall Program/Erase times and effectively increases endurance by a factor of 2.

3. The 2-T cell does not suffer from over-erase effects which can cause bit line currents to be altered to the point where the cells can no

longer be read. The Access transistor de-selects the Read paths of the unselected bit lines.

4. The cell can be read at low voltage (1.2V) because of the large Read current provided by the Access gate. Thus the Control Gate does not have to be pumped during Reads. This is a major advantage since Reads may occur every clock cycle in an Embedded Flash used for Code memory and Charge pump noise and power are eliminated. The low Control gate voltage also means that Read Disturb of unselected cells is minimal.

Process status, Reliability Studies and Data

Endurance studies were done on a 2.7Mbit array (a typical Embedded size). Two million cycles were used to collect data. Endurance performance clearly exceeds 100K cycles, indicating a robust design that meets its goals. Data retention after cycling was evaluated by gate stress measurements to observe SILC effects. No significant difference was observed on gate stress (thus also read disturb and data retention due to SILC) after cycling.

No fails due to window closure were observed on 16 Mbit demonstrator module after 10,000 cycles. Extended intrinsic endurance cycling capability up to 100K cycles was shown on 120 16Mbit samples.

Retention testing of 279 samples after 1000 hrs. of storage at 150C showed no failures. A conservative extrapolation of bit fail level after 10 year continuous reading and 10K endurance at worst case temperature of 150C leads to a value of 7 ppm.

Read current measured is shown in Figure 3 for various Access Gate voltages (VDD). At 1.8V, Read current is nominally 30 microamps [1], dropping to 20 microamps at 1.2V. Threshold voltage measurements for different Write and Erase voltages versus durations are shown in Figure 4, showing a window of 3V for typical Write and Erase conditions. Window closure observed is very small at 100,000 cycles (Figure 5) showing that the Erase Vt is well below the Control gate Read voltage.

Embedded Applications

With a Page write time of 1 ms (a Page can be, for instance, 512 bytes in length) and a Sector erase time of 400ms, system requirements from customers are easily met. The Flash supports both self-timed as well as externally timed Reads, thus allowing power optimization by selecting the appropriate Read method depending on system cycle time (self-timed saves power at slow clock speeds; externally timed is faster at high clock speeds)

Library blocks of various sizes and configurations have been developed and used in various Embedded Controller projects within Philips. Sector sizes, Row and Word widths can be specified for optimum system performance. A memory controller has been developed which also affords a full JTAG Test capability and interfaces to the ARM7 CPU. A Boot Loader program is entered into a dedicated Sector at Wafer Sort which then allows User Programs to be loaded into Flash and updated via a Flash Programming Interface to the User Program.

Working silicon has been demonstrated and a large range of low-cost low voltage products are planned based on this technology using the ARM and various other cores. This technology is expected to become a high-volume mainstream Embedded memory process.

Future Directions

Shrink paths and future directions for this technology are being studied to allow cost reduction to finer dimensions with the minimum of re-design effort required considering the large investments in process and product developments made in this technology.

Reference

[1] Do Dormans, et al., SSDM 2001, Reliability aspects of advanced embedded floating-gate non-volatile memories with uniform channel FN tunneling for both program and erase.

Diagrams

Figure 1: Flash Cell Structure.

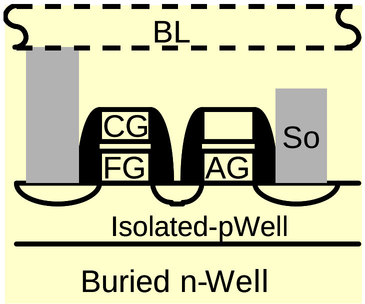
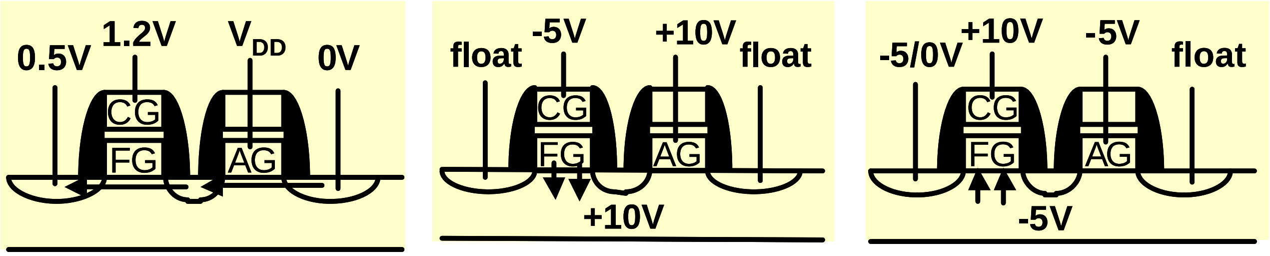


Figure 2: Read, Erase, and Program Voltages.


READ

ERASE

PROGRAM

Figure 3. Read Current:

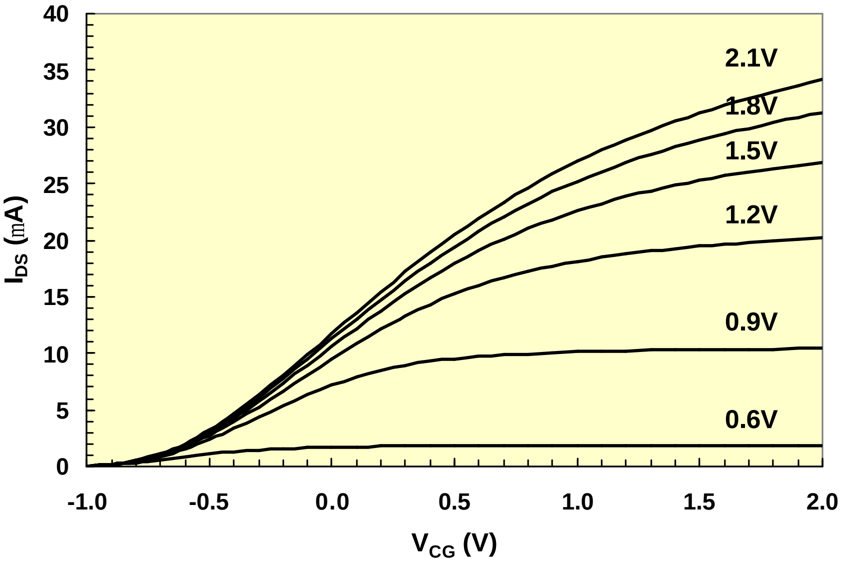


Figure 4. Write/Erase behaviour:

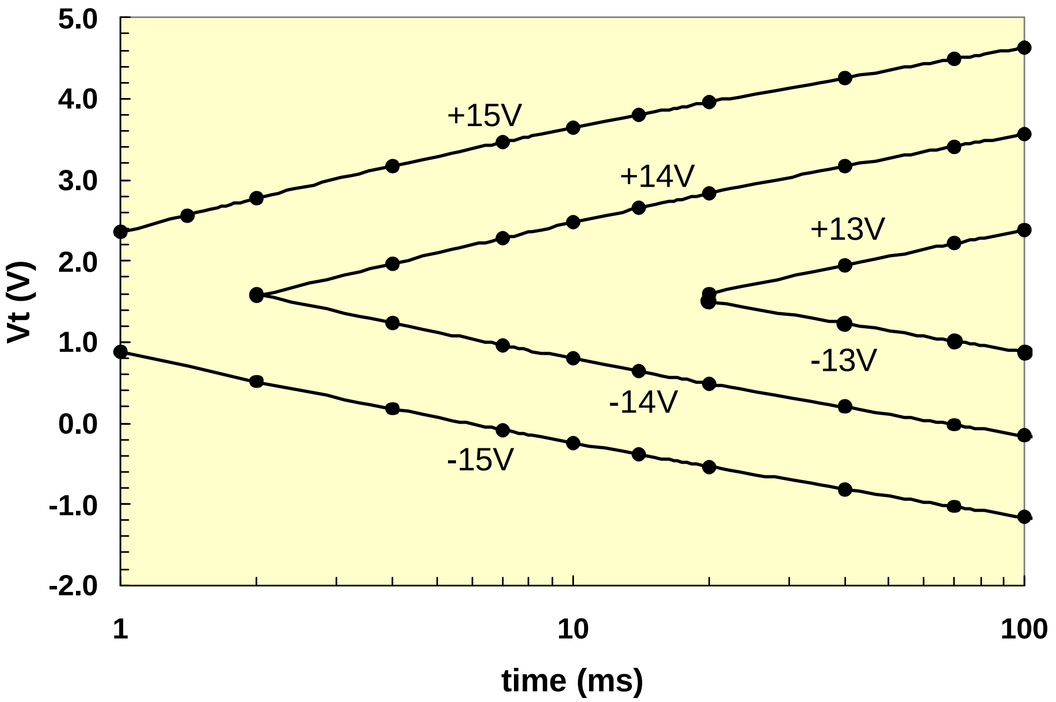


Figure 5. Window change after 100K Cycles: