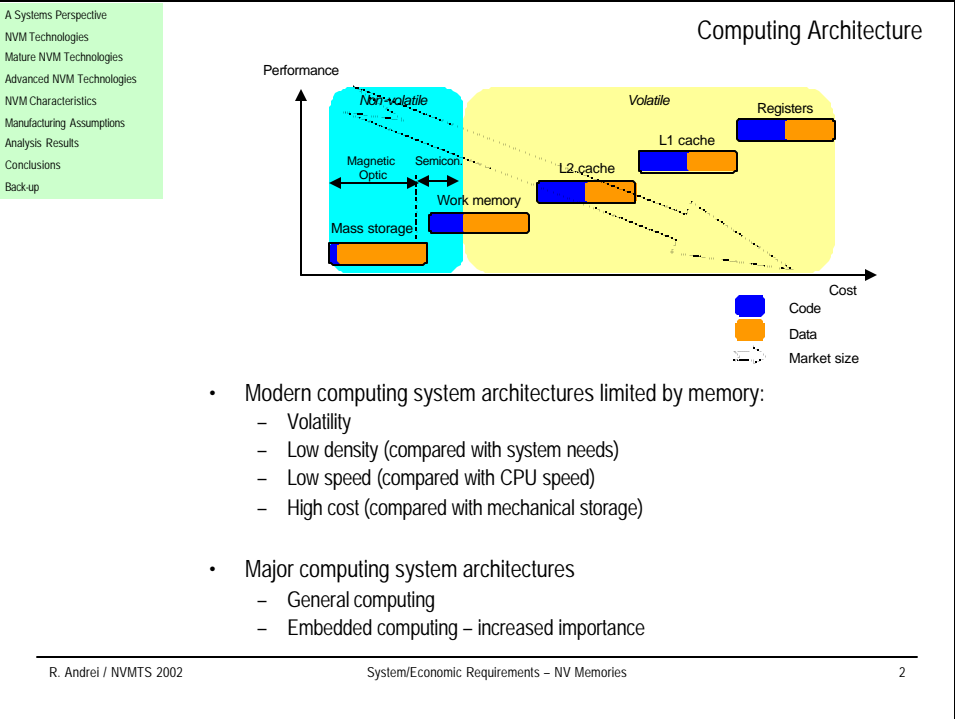


System and Economic Requirements for Advanced NV Memories

NVMTS 2002



A Systems Perspective

NVM Technologies

Mature NVM Technologies

Advanced NVM Technologies

NVM Characteristics

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Memory Layers

MEMORY LAYER
Registers
L1 cache
L2 cache
Work memory
Mass storage

TECHNOLOGY
Flip -flops
SRAM
SRAM
NVM (code)
DRAM (data)
Magnetic/optic

STORAGE PRINCIPLE
8T/cell
6T/cell
6T/cell
1T1E/cell
1T1C/cell

MEMORY LAYER
Registers
L1 cache
L2 cache
Work memory
Mass storage

TYPICAL SIZE
256 Bytes
256 kB
2 MB
256 MB
128 GB

SIZE RANGE
10 ² Bytes
10 ⁵ Bytes
10 ⁶ Bytes
10 ⁸ Bytes
10 ¹¹ Bytes

- Storage need >> memory need
 - approximately 10 orders of magnitude

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NVM – Technology Lineup

- Mature NVM technologies
 - Floating gate – NOR, DINOR, ACT
 - NAND, AND, AG-AND
 - Trapped charge – MirrorBit, NROM (inherently 2 bits/cell)
- Advanced NVM technologies
 - FRAM – ferroelectric principle
 - MRAM – magnetic polarization principle
 - CRAM – phase change principle
 - PFRAM – dipole change principle
 - Nano FG (Nanocrystal) – quantum transistor based
 - PMC – phase change principle
 - NRAM – electro-mechanical principle
- Embedded-able NVM technologies
 - HIMOS
 - SONOS
 - SuperFlash
 - GreenFlash
 - e-Flash
- "Least conventional" technologies
 - McRAM (NV/SRAM monocrystalline)
 - Millipede (micro machined)
 - SpinRAM (all metal structure)
 - NonoMem (on plastic support)
 - Resonant Interband Tunneling Device – RITD
 - Gain memories – SESO, PLEDM, STTM

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- Application / market requirements
- **System requirements**
- Manufacturing economics

Advanced Memory Objectives – A Systems Perspective

Primary system objectives for next NVM technologies:

- Enable “application agnostic” memory components
- Reduce memory hierarchy layers to a minimum
- Non-volatility
- Symmetric access
- Access speed comparable with CPU I/O speeds
 - Plus many more secondary objectives

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Mature NVM – Liabilities

- System level liabilities
 - Memory layer specificity – work or storage memory
 - Not suitable for registers, L1 cache or L2 cache
 - Technology limitations offset by on chip circuitry
 - Read-while-write
 - Garbage collection
 - Wear leveling
 - Limited write endurance
 - Incremental system overhead
 - Hardware
 - Software
 - Highly asymmetric access cycles
- Consequences
 - Increased system cost
 - Reduced system performance
 - Memory market fragmentation – higher component cost

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Mature NVM – Liabilities

- Technology and manufacturing level liabilities
 - Low normalized density – an order of magnitude less than mechanical magnetic storage
 - Normalized density enhancing technique (MLC)
 - HV manufacturing process
 - Average yields
 - Resource intensive testing
- Consequences
 - Increased manufacturing cost
 - Increased system cost

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Density Calibration 1

- Magnetic storage density history
 - 25% p.a. through 1990
 - 60% p.a. 1990 – 1998
 - 100% p.a. 1998 – present
- Magnetic storage density forecast
 - 100% – over aggressive
 - 25% – conservative
 - Gradual progression – best compromise
- Superparamagnetism limits
 - Today's predictions 20 Gb/cm² (130 Gb/sq in)
 - Limits continuously pushed out by:
 - Using perpendicular recording
 - Increasing Ku
 - Using patterned recording media

(Gb/cm ²)	2000	2007
NAND2b	1.0	3.3
AG-AND2b	1.2	4.1
NROM	1.6	5.0
FRAM	---	2.3
MRAM	---	2.3
CRAM	---	2.7
PFRAM	---	23.9
nCrystal	---	3.8
PMC	---	10.0
NRAM	---	5.0
HDD	4.1	15.0

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Advanced NVM Technologies – FRAM

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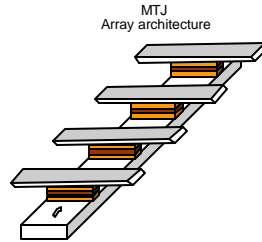
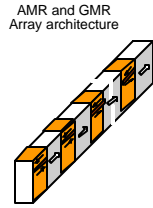
graph TD
    A[FRAM cell types] --> B[FEFET]
    A --> C[FE-capacitor]
    B --> D[Single capacitor]
    B --> E[Double capacitor]
    C --> D
    C --> E
  
```

- FE-capacitor – DRO structures
 - 2T2C configuration – obsolete
 - 1T1C configuration
- FE-FET – NDRO structure
 - 4f² (theoretical)
- Risk factors
 - Processing – high temperature, hydrogen contamination, substrate oxidation through ferroelectric material deposition
 - Switching field through half select currents
 - Broad range of time scales – high on chip circuit dynamics

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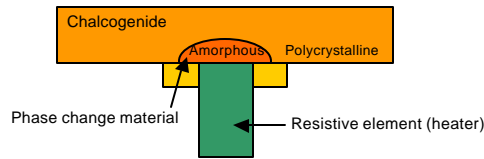
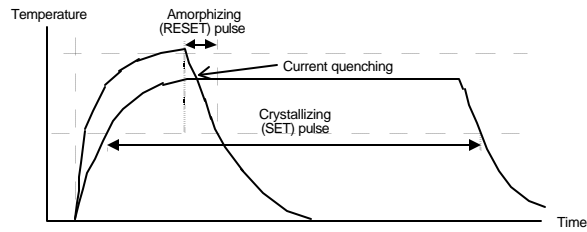
Advanced NVM Technologies – MRAM



- AMR and GMR structures
 - Sequential structures
- MTJ
 - Cross point structure
- Risk factors
 - Processing
 - Magnetic field uniformity
 - Thick layer uniformity, coercive field uniformity
 - Scalability to finer geometries
 - Switching field control through half-select currents

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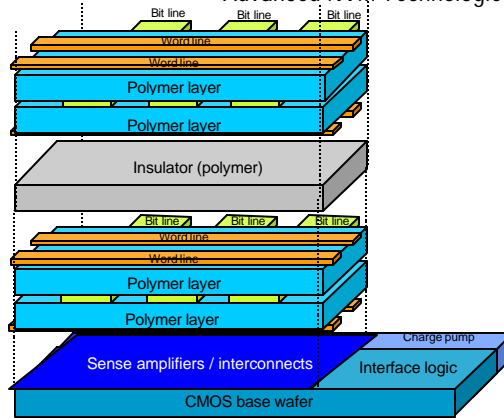
Advanced NVM Technologies – CRAM



- Risk factors
 - Standard cmos process integration – chalcogenide deposition on cmos substrate
 - Alloy optimization for heavy duty write operations
 - Operation speed
 - Power density

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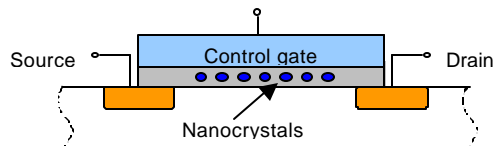
Advanced NVM Technologies – PFRAM



- Characteristics
 - Stack-able configuration, up to 8 layers
 - DRO
 - Very slow access cycles (ms range); suitable for external storage
- Risk factors
 - Materials – optimized polymer (difficult learning curve)
 - Processing – polymer deposition on cmos substrate

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Advanced NVM Technologies – Nano FG (Nanocrystal)



- Advantages
 - Direct tunneling erase / programming; no HV circuitry
 - Higher endurance (low voltages reduce oxide degradation)
 - Ultra-low power consumption
 - Faster read / write cycles (thinner oxide layers lead to higher current densities)
 - Nearly unlimited size scaling (only limit: size of the crystals)
 - Accurate multi-level cell capability (single electron charges possible)
- Risk factors
 - Basic R&D
 - Process immaturity and instability

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Advanced NVM Technologies – Programmable Metallization Cell

PMC – Programmable Metallization Cell

- Phase change type memory
- Storage principle (write)
 - Ability to increase / decrease the metal content of a solid electrolyte
 - Result – electric parameter (resistivity) change
 - MLC capability
- Read principle
 - Measure resistivity
- Physical principle
 - Solid state electrolytes (solid state ionics ; electro-chemistry)
 - Good electrolytes
 - Chalcogenide type glass with 39% Ag (Ag-Ge-Se)

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Advanced NVM Technologies – Nano-Tube RAM (NRAM)

Nanotube Device concept

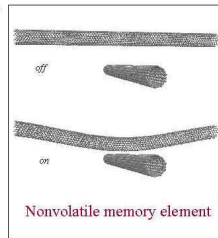
A suspended nanotube crossbar architecture is *intrinsically* bistable

OFF state: mechanical minimum

ON state: van der Waals minimum

Switching: biasing leading to electrostatic attraction or repulsion

Reading: high/low junction resistance



- Architecture
 - Cross-bar
 - Cross-point
- Carbon nano-tube (1 atom wall thickness, 1-2nm diameter) suspended over a fixed layer of nano-bars
- Structure:
 - Bistable
 - Electrostatically switchable

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NVM Endurance

(cycles)	2000	TN 2001 130	2002	2003	TN 2004 90	2005	2006	TN 2007 65	TN 2010 45	TN 2013 33	TN 2016 23
Channel Length											
DRAM	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity
SRAM	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity	infinity
NOR (1b/cell)	10 ⁶	10 ⁶	10 ⁶	10 ⁶	10 ⁶	10 ⁵	10 ⁶	10 ⁶	10 ⁶		
NOR (2b/cell)	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵		
NOR (4b/cell)											
DINOR	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	10 ⁶	10 ⁶	10 ⁶			
ACT											
NAND (1b/cell)	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵		
NAND (2b/cell)											
AND (1b/cell)	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵			
AND (2b/cell)	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵	3x10 ⁵			
AG-AND (2b/cell)											
MirrorBit (2b/cell)			10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	
NROM (2b/cell)		10 ⁴	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁵	
HIMOS (1b/cell)		10 ⁶	10 ⁶	10 ⁶	10 ⁶						
HIMOS (2b/cell)											
SONOS	10 ⁵	10 ⁵	10 ⁵	10 ⁵	10 ⁶	10 ⁶	10 ⁶	10 ⁷			
FRAM(2C)	variable	variable	variable	variable							
FRAM(1C)		variable	variable	variable	variable	variable	variable	infinity	infinity	infinity	infinity
FRAM					infinity	infinity	infinity	infinity	infinity	infinity	infinity
MRAM		infinity	infinity	infinity	infinity	infinity	infinity	10 ¹³	10 ¹³	10 ¹³	10 ¹³
CRAM								10 ¹²	10 ¹²	10 ¹²	10 ¹²
PFRAM								variable	variable	variable	variable
nCrystal								10 ⁷	10 ¹⁰	10 ¹⁰	10 ¹⁰
PMC								10 ¹³	10 ¹³	10 ¹³	10 ¹³
NRAM								10 ¹³	10 ¹³	10 ¹³	10 ¹³

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NVM Access Times

Memory Technology	Read (ns)	Erase (ns)	Program (ns)
DRAM	40	n.a.	40
SRAM	5	n.a.	5
NOR	50	200m	50i
DINOR	50	200m	50i
ACT	100	200m	40i
NAND	100	200m	50i
AND	100	200m	50i
AG-AND	80	200m	10i
MirrorBit	40	100m	7i
NROM	40	100m	7i
HIMOS	30	100m	3i
SONOS	50	100m	10i
FRAM	30	n.a.	30
MRAM	10	n.a.	10
CRAM	50	n.a.	150
PFRAM	200i	n.a.	200i
nCrystal	?	?	?
PMC	10	n.a.	10
NRAM	2	n.a.	2

- Mature NVM
 - Highly asymmetrical access times
 - Poor level of sustained transfer rates because of hidden memory cycles (Flash, trapped charge) or DRO (DRAM)
- Advanced NVM
 - Nearly perfectly symmetrical access times (exception: CRAM)
 - Sustained transfer rates close to the sum of access times (exception: PFRAM)

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NVM Cell Manipulation Energy

Memory Technology	Read (pJ)	Erase (pJ)	Program (pJ)
DRAM	17	n.a.	12
SRAM	2	n.a.	7
NOR	5	40i	100n
DINOR	5	40i	100n
ACT	4	40i	80n
NAND	10	25i	80n
AND	10	25i	80n
AG-AND	8	25i	60n
MirrorBit	10	25i	100n
NROM	10	25i	100n
HIMOS	5	20i	120n
SONOS	10	25i	140n
FRAM	20	n.a.	15
MRAM	5	n.a.	30
CRAM	1	n.a.	150i
PFRAM	200	n.a.	100
nCrystal	?	?	?
PMC	10i	n.a.	10i
NRAM	15	n.a.	15

- Power consumption increases disproportionately for higher density devices
- Mature NVM
 - Disproportionately high power consumption, due to erase cycle and HV circuitry
 - Only marginal power consumption improvements possible
- Advanced NVM
 - Very low power consumption (exception: CRAM)
 - Power consumption is a major risk factor for CRAM
 - Extremely low power consumption: Nanocrystal

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Interconnect Delay/Losses Considerations

- Component considerations
 - Component delay/losses = Cell delay/losses + Interconnect delay/losses
- Global wires (between modules)
 - Cannot be scaled in length
 - Best case - will not increase in length
- Cu much better than Al
 - However, it scales up with decreasing manufacturing geometries

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NVM System Characteristics

Memory technology	Degree of agnosticism	Number of comp. variations	System overhead	Memory layers	System cost contribution	Code exec. capability
DRAM	++++	+++	+++	-----	-	+++++
SRAM	+++	++	+++++	-----	+	+++++
NOR	-----	-----	---	++	++	+++
DINOR	-----	-----	---	++	++	+++
ACT	-----	-----	---	++	++++	+++
NAND	-----	-----	-----	++	----	-----
AND	-----	-----	-----	++	----	-----
AG-AND	-----	-----	-----	++	----	-----
MirrorBit	----	--	---	++	-	+++
NROM	----	--	---	++	-	+++
HIMOS	++	++	+++	--	++	+++
SONOS	++	++	+++	--	++	+++
FRAM	+++++	+++++	+++++	+++++	++	+++++
MRAM	+++++	+++++	+++++	+++++	+++++	+++++
CRAM	+++++	+++++	+++++	+++	+++	+++++
PFRAM	++	+++++	+++	---	-	-
nCrystal	+++++	++	+++++	-	--	+++++
PMC	+++++	+++++	+++++	+++++	+++++	+++++
NRAM	+++++	+++++	+++++	+++++	+++++	+++++

+++++ Most positive ----- Most negative

- "Favorites" ranking: MRAM, FRAM, CRAM,
- Reality check:
 - NOR, NAND & Co are available now in any quantity at a tremendously low price
 - MirrorBit and NROM are close to making a market entry

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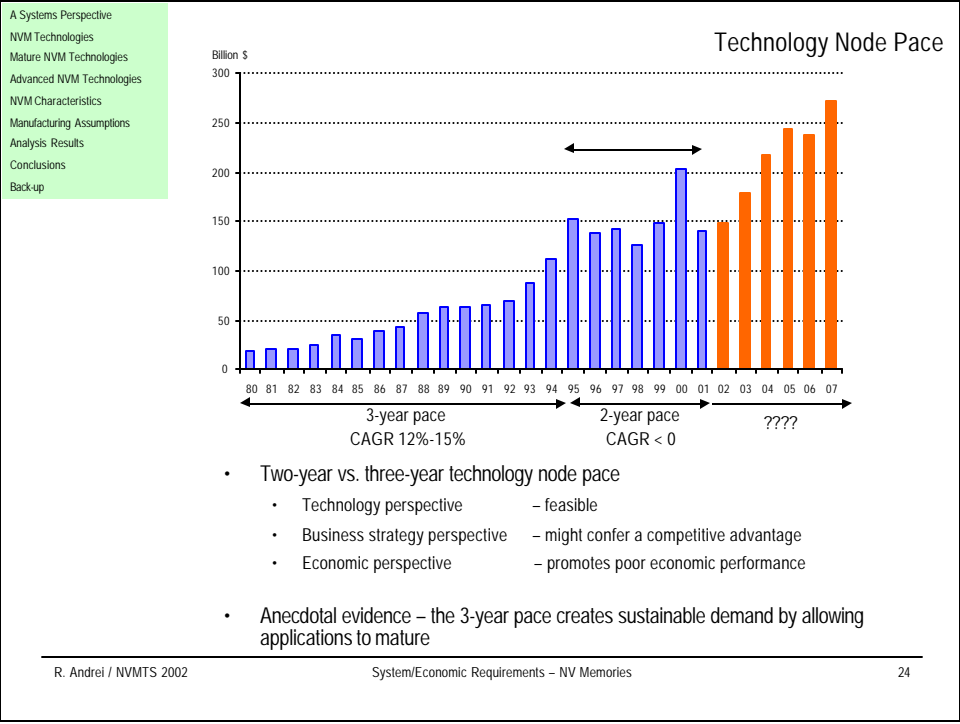
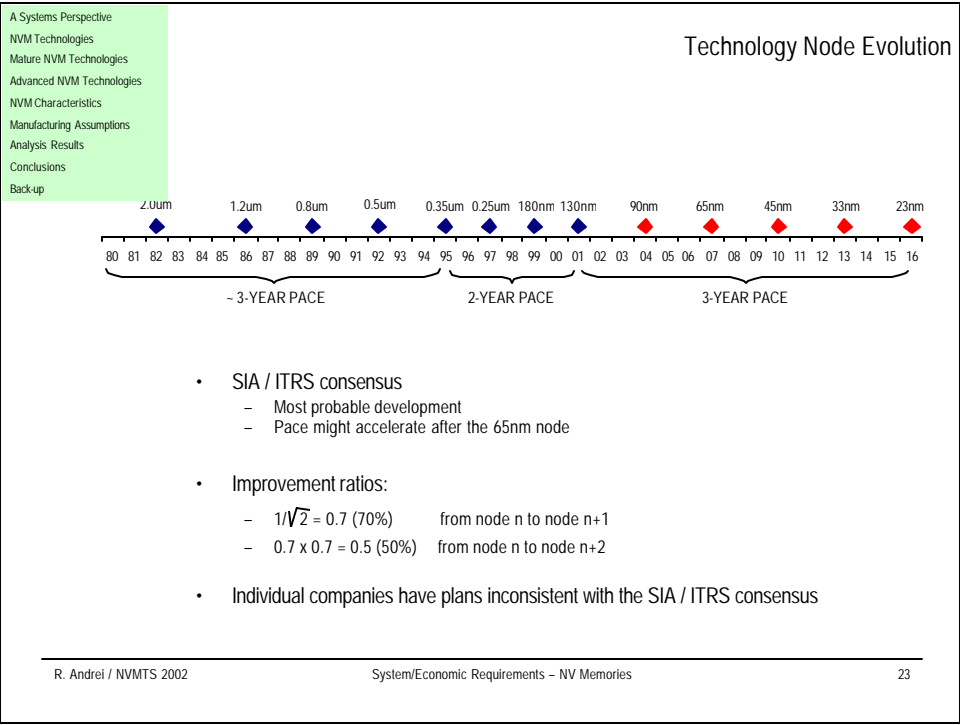
Conclusions

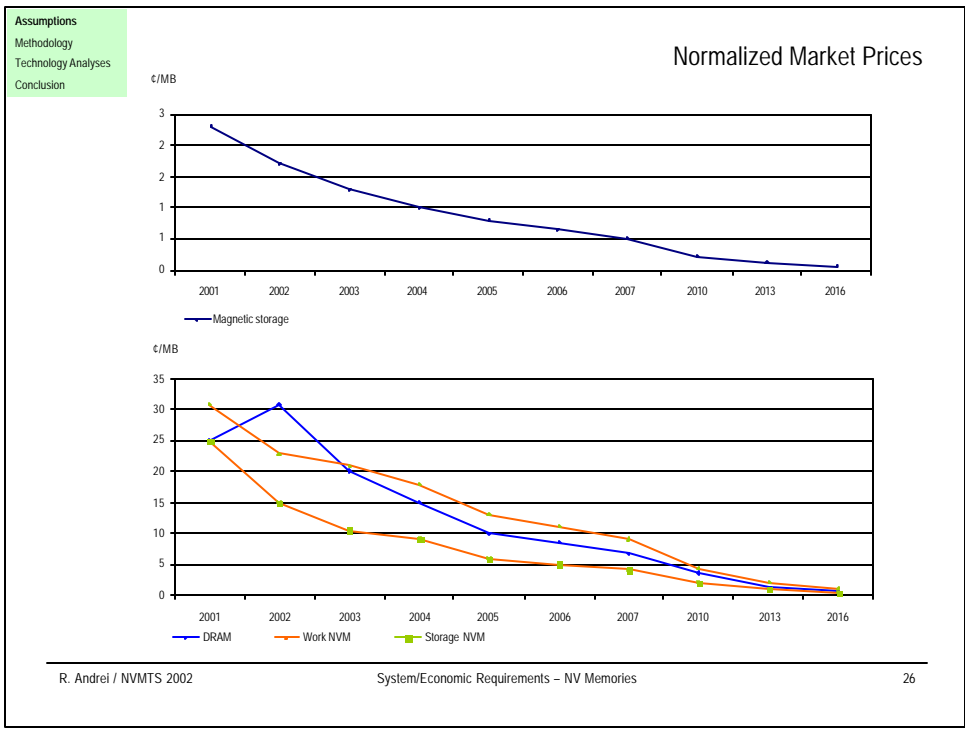
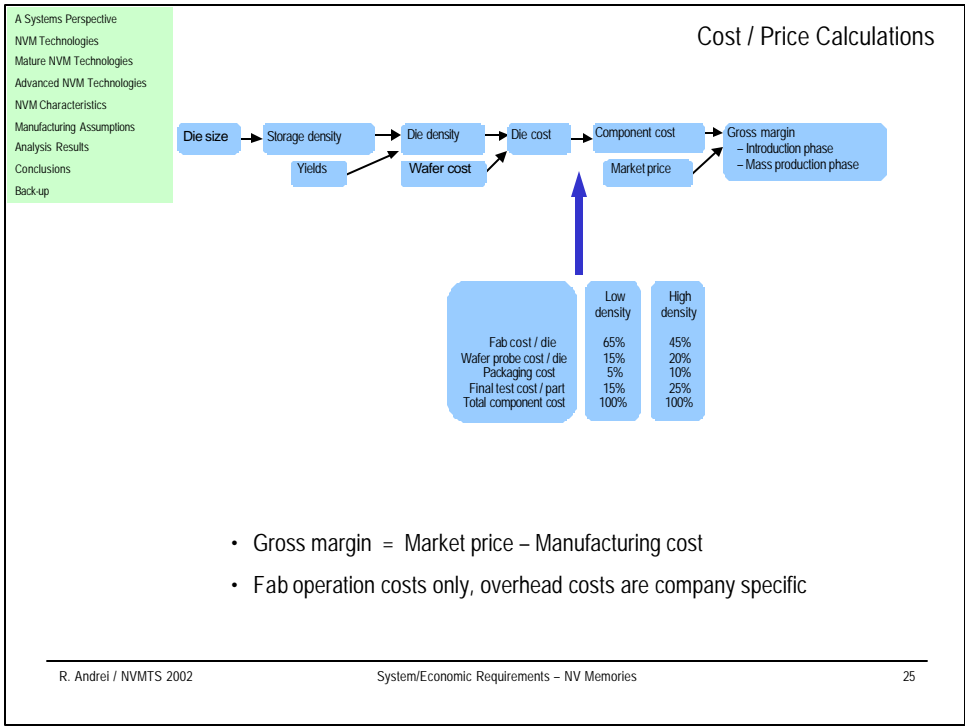
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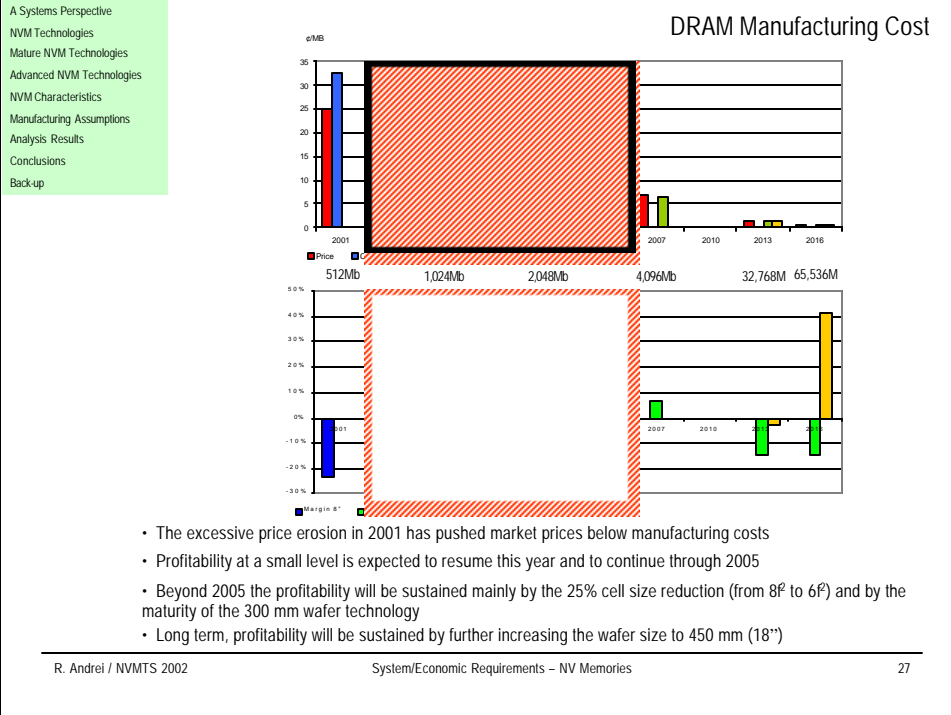
Assessment Criteria

- Application / market requirements
- System requirements
- **Manufacturing economics**

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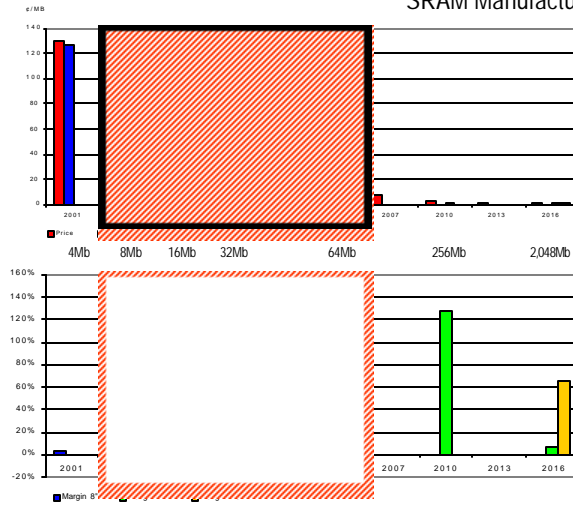
- Conclusion**
- NVM technologies and technology variations tally
 - 29 (including DRAM and SRAM) !!!! and counting
 - Market elimination criteria
 - System friendliness
 - Design and manufacturing economics
 - Manufacturing economics analysis results:
 - Cost < projected market price
 - Profitable
 - Cost ~ projected market price
 - Need for strategic considerations
 - Cost > projected market price
 - Profitability ?!
 - System requirements and manufacturing costs
 - Key assessment criteria, but not the only ones
 - Complement market criterion
- R. Andrei / NVMTS 2002 System/Economic Requirements – NV Memories 28

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Back-up Slides

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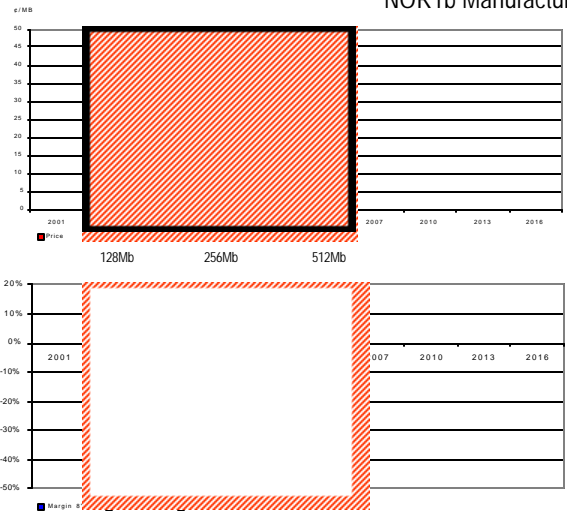
SRAM Manufacturing Cost



- The SRAM profitability is sustained mainly through creating application specific components (de-commodization track)
- 6T SRAMs will not be profitable any more beyond 32 Mb; after 2005, the 6T SRAM will be replaced by the 1T1R1M structure
- The PSRAM profitability will be sustained by the on-chip integrated logic and revived by the 450 mm wafer introduction

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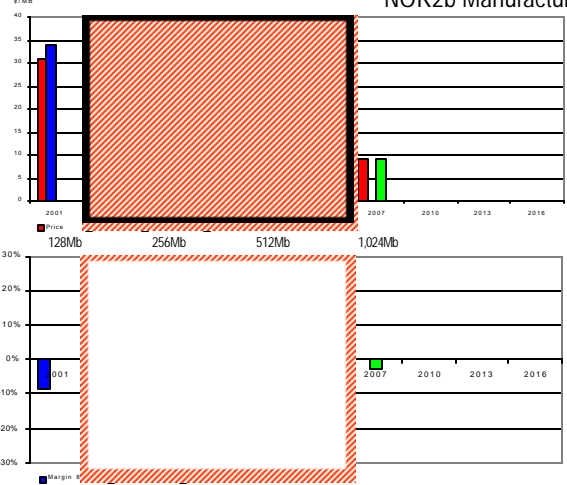
NOR1b Manufacturing Cost



- On average, 1bit/cell NOR components are expected to become uncompetitive in the work memory segment
- For the next two to three years 1bit/cell NOR components might command a higher market price, due to their monopolistic position in specific market segments
- The highest marketable 1bit/cell NOR density is predicted to be 512 Mb

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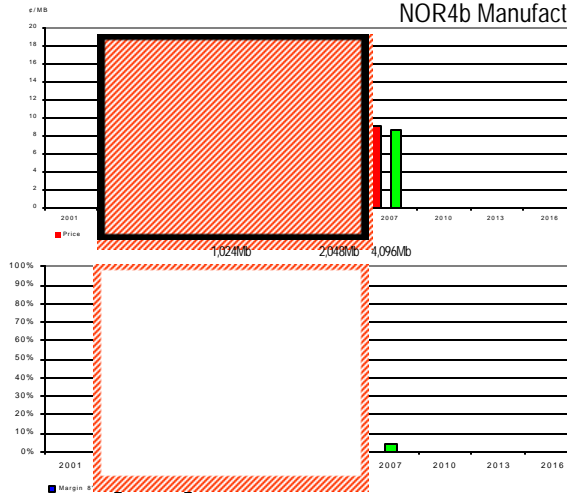
NOR2b Manufacturing Cost



- 2bits/cell NOR components are expected to remain profitable throughout the forecast period, in spite of very low manufacturing yields (currently estimated at 50% – 60%, projected to increase by approximately 20 points)
- The transition to the 300 mm wafer technology is expected to boost and sustain profitability throughout the forecast period
- For the time being, 2bits/cell NOR is the most popular non volatile work memory variation, which will command a premium on the market
- 2bits/cell NOR components that fail the final test might be sold as 1bit/cell NOR components

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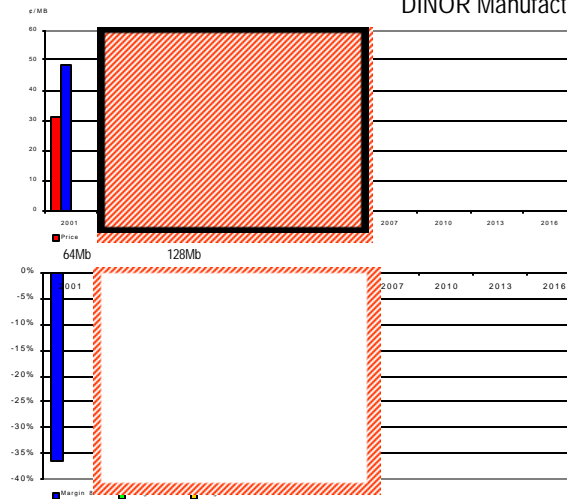
NOR4b Manufacturing Cost



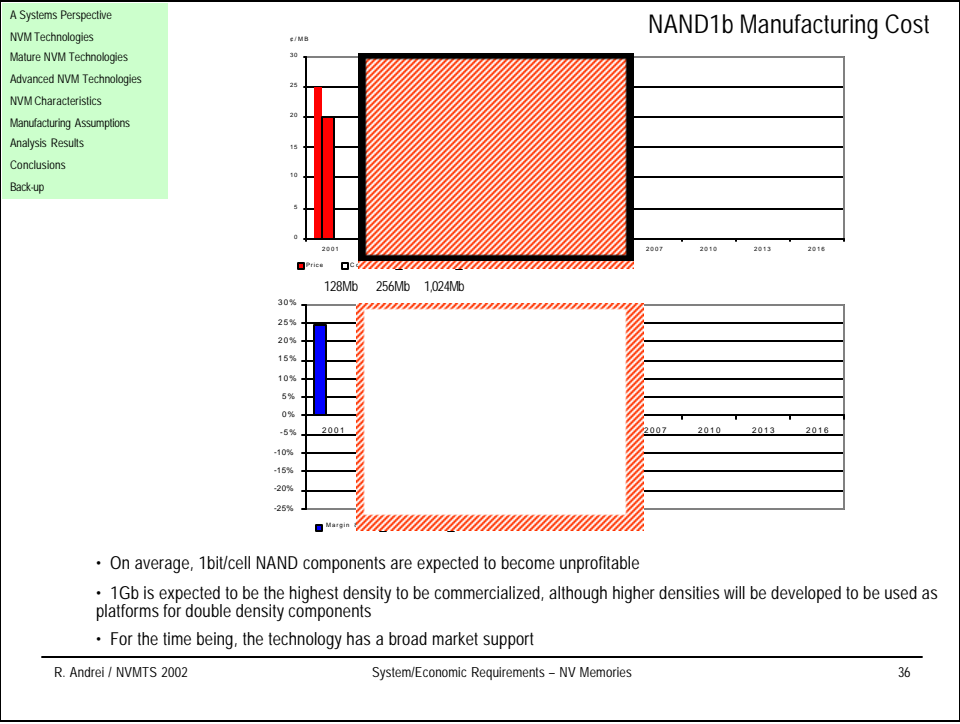
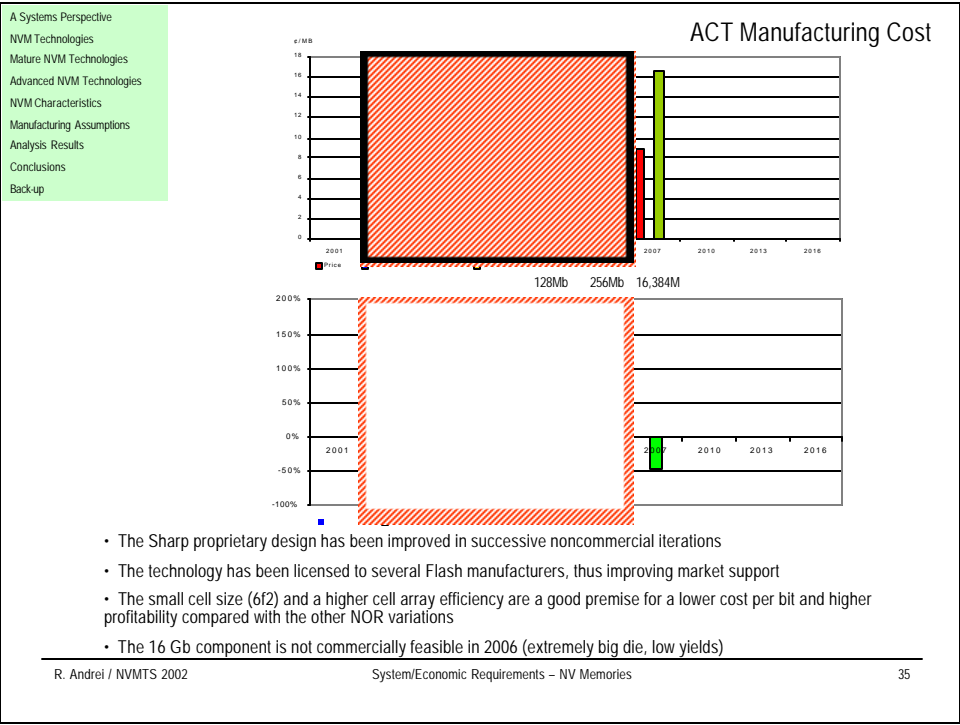
- No 4bits/cell NOR components are firmly scheduled so far; the first devices might become available in 2004, if at all
- The very high density components are expected to command above average profits from 2004 through 2006; the profits might shrink if the production yields are not radically improved
- The technology variation has the potential to replace the simple and double density variations, providing the design and manufacturing technology will mature at the expected pace
- 4bits/cell NOR components that fail the final test might be sold as 2bits/cell NOR or as 1bit/cell NOR components

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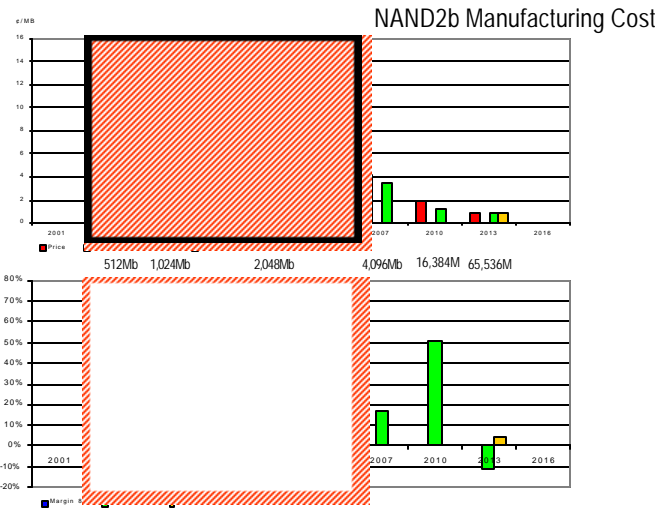
DINOR Manufacturing Cost



- The technology has limited market support (Mitsubishi only), which severely restricts the research resources In addition, DINOR appears not to have a decisive competitive edge over NOR
- The available simple density variations are not profitable any more and there is little probability that they can return to profitability
- Obsolescence!!

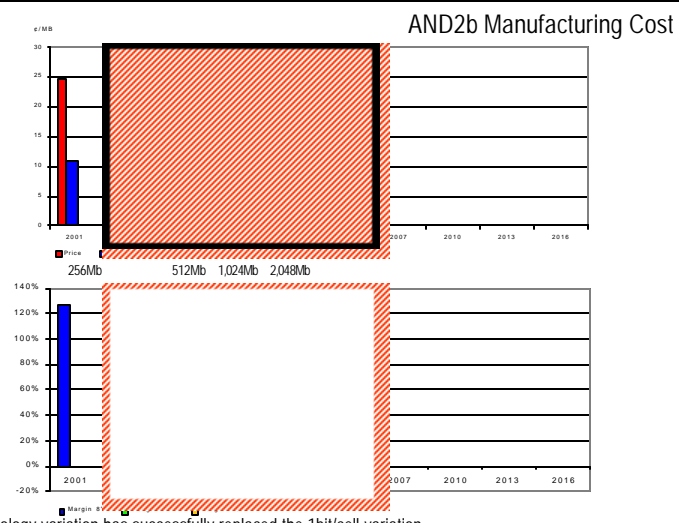


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- NAND2b variation is supposed to remain highly profitable throughout the forecast period
- A major profitability enhancer is the capability to logically map out bad cells and to replace them with on-die spare cells; the average built-in redundancy for this purpose is 5%
- Additional map outs can be performed by the system, which represents a de facto supplementary yield increase
- The relative NAND performance degradation from 1bit/cell to 2bit/cell is smaller than the equivalent NOR performance degradation

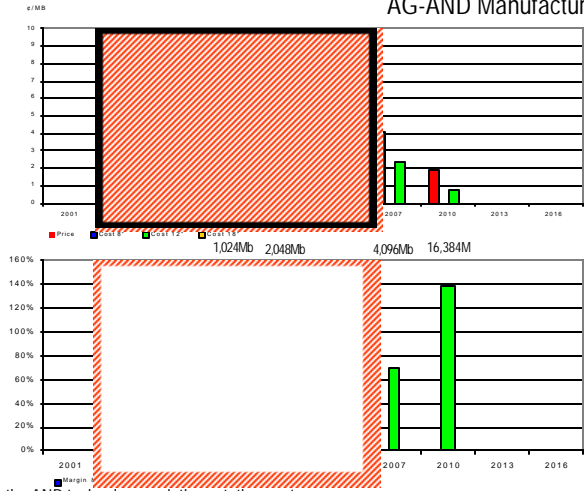
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- The 2bits/cell AND technology variation has successfully replaced the 1bit/cell variation
- A major profitability enhancer is the capability to logically map out bad cells and to replace them with on-die spare cells; the average built-in redundancy for this purpose is 5%
- For economic reasons, during the forecast period, Hitachi might obsolete this technology variation, in order to better support the more advanced AG-AND variation
- Three times higher write endurance than NOR

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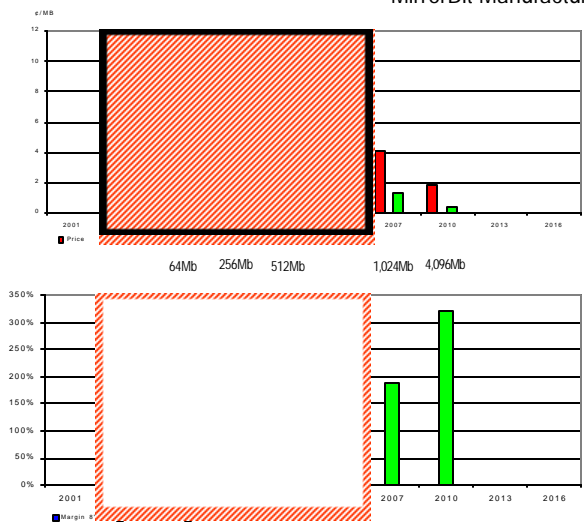
AG-AND Manufacturing Cost



- AG-AND might obsolete the AND technology variations staling next year
- The small cell size and the improved cell array vs. overhead ratio pushes the technology profitability above the NAND technology average
- A major profitability enhancer is the capability to logically map out bad cells and to replace them with on-die spare cells; the average built-in redundancy for this purpose is 5%
- Three times higher write endurance than NOR

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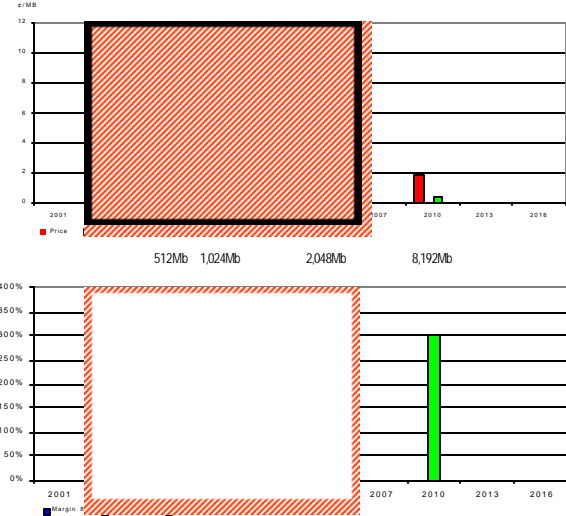
MirrorBit Manufacturing Cost



- MirrorBit is forecast to yield nearly an order of magnitude higher margins than the industry average
- The design and manufacturing technology is mature, for it has been developed and improved for more than two decades by now
- Relatively low write endurance level (currently ~ 10⁴ cycles)

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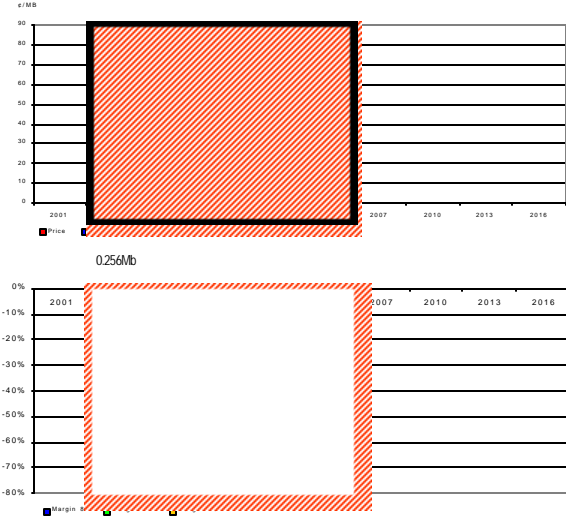
NROM Manufacturing Cost



- NROM is forecast to yield nearly an order of magnitude higher margins than the industry average
- The design and manufacturing technology is mature, for it has been developed and improved for more than two decades by now
- Relatively low write endurance level (currently ~ 10⁴ cycles)

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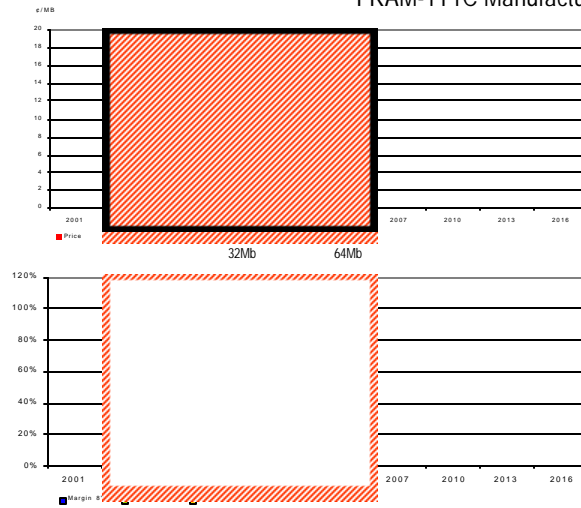
FRAM-2T2C Manufacturing Cost



- The technology variation has had a lengthy development period, in excess of three decades
- Only few components have been manufactured so far
- The large cell size and the poor manufacturing performance are expected to obsolete the technology right away

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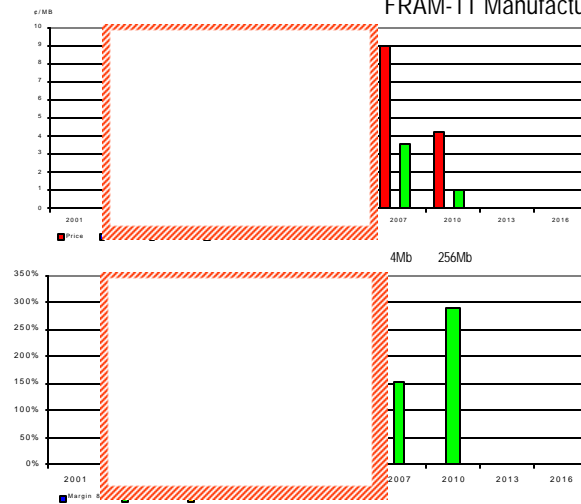
FRAM-1T1C Manufacturing Cost



- 1T1C FRAM components are expected to command high yields, providing that the manufacturing technology will mature according to the historic industry curves
- The technology variation can be used for embedded configurations as well, for it requires a small overhead area and no high voltage circuitry
- The major risk factor remains, as before, the immaturity of the manufacturing technology

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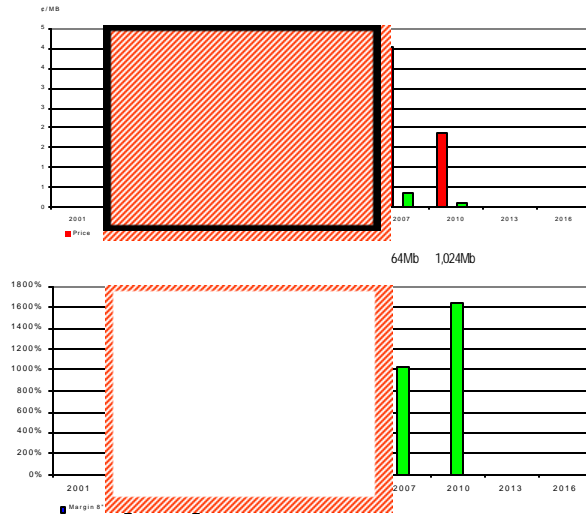
FRAM-1T Manufacturing Cost



- Subject to the development of an adequate manufacturing process, the technology variation has good prospects to become an economically efficient universal memory candidate
- The only FRAM variation with a non destructive readout (NDRO) cycle; this creates the premise to be used for both work and storage memory blocks
- Unlike the 1T1C FRAM variation, the complexity of the manufacturing process makes out of the 1T FRAM a less likely candidate for embedded memory configurations

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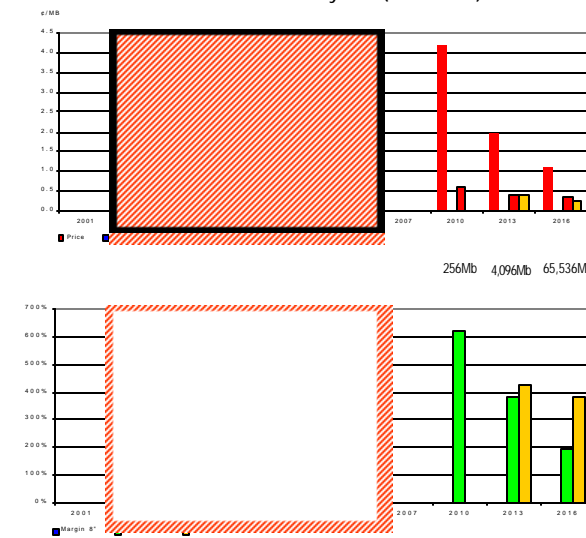
PFRAM Manufacturing Cost



- PFRAM has the potential to become the first semiconductor based memory technology to overtake the mechanical magnetic technology in terms of storage density, at a similar normalized cost range
- A successful PFRAM market introduction might lead to a further memory market segmentation

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Nanocrystal (Nano FG) Manufacturing Cost



- Nanocrystal (Nano Floating Gate) technologies could become a highly efficient technical and economic replacement for floating gate NVM technologies, some time after the forecast period