The Future of Nonvolatile Memories

Thomas Mikolajick[1)], Cay-Uwe Pinnow[2)]

1) Infineon Technologies Dresden, IFDD MDC TIN

Königsbrueckerstrasse 180, 01099 Dresden, Germany

Tel. +49351-886-7770, Fax +49351-886-7772, Thomas.Mikolajick@infineon.com

2) Infineon Technologies, MP TI TD INN

Balanstrasse 73, 81541 Munich, Germany

Abstract— In this paper the ongoing research and development activities on future nonvolatile memory technologies are described. After reviewing the mainstream nonvolatile memories on the market today, memory concepts based on switching effects in inorganic and organic materials as well as in single molecules are summarized. Finally the pros and cons are compared and conclusions for the near, mid and long-term perspectives are drawn.

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1. INTRODUCTION

Driven by an increasing demand for mobile devices, the market for nonvolatile memories is rapidly growing [1]. Today the majority of nonvolatile memories are based on charge storage and are fabricated by materials available in CMOS processes. These devices have some general shortcomings like slow programming (from microseconds up to milliseconds), limited endurance (typically $10^5 – 10^6$ write/erase cycles) as well as the need for high voltages (10-20V) during programming and erase.

These shortcomings imply some severe restrictions on the system design side. A memory that works like a random access memory (similar to DRAM or SRAM) and is also nonvolatile would therefore greatly simplify system design, since one universal memory could be used, where two or three memories are required today. Moreover, much higher data densities than the present ones will be required for storing multi media data like videos. This calls for a memory with an extremely small bit cell size. To achieve these goals, novel materials showing new switching mechanisms have to be introduced into the CMOS process flow. Fig. 1 shows the hierarchy of possible CMOS memory material extensions used as a basis for the following discussion

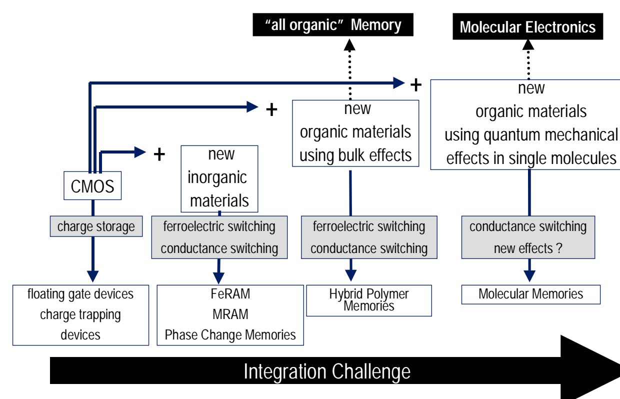

Fig. 1 The hierarchy of future nonvolatile memories

2. NONVOLATILE MEMORIES BASED ON CHARGE STORAGE

The vast majority of nonvolatile memories available on the market today is based on charge storage [2]. Two possibilities to store charges are commonly used, namely floating gates and charge trapping layers. The dominant devices today are floating gate memories. In charge storage devices the requirement for 10 years of data retention calls for a large energy barrier that has to be overcome during programming and erasing [3, 4]. This, on the other hand, leads to massive shortcomings. A high voltage (10-20V) is needed to pass the potential barrier during program and erase, write/erase speed is rather slow

(from microseconds up to seconds) and write/erase endurance is limited (typically about 10^5-10^6 cycles).
The different options of nonvolatile memories on the market today can be mainly characterized by the amount of alterability and the cell size. A mask ROM (Read only memory) can only be programmed during fabrication but has a very small cell size. An EEPROM (electrically erasable programmable read only memory), on the other hand, is writable and erasable on a byte level, but has a rather large cell size utilizing two transistors per cell. Flash memories, which are programmable on a byte or word basis and erasable on a block or sector basis, can be realized using a single transistor as a memory cell and, therefore, have proven to be the best compromise for many applications. Among the Flash memories there are two different array architectures that are commonly used. In the NOR architecture the cells on one bitline are arranged in parallel making a fast random access (well below 100ns) possible. In the NAND architecture the cells connected to one bitline are arranged in series [5].

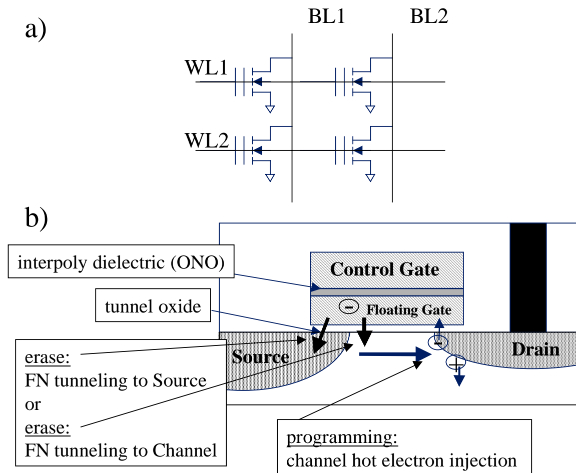

Fig 2. NOR Flash Array (a) and typical NOR Flash cell (b)

Fig. 2 shows the schematic of a NOR array and a standard NOR Flash cell. The cell consists of a MOS transistor with an additional floating gate between the channel and the control gate. The cell is programmed using channel hot electrons leading to short programming times in the 1-10µs range and a high programming current due to the low efficiency of hot electron injection. Erase is done by Fowler Nordheim tunneling. Up to very recently it was common to erase by tunneling to the source junction of the transistor. Using a channel erase scheme, however, leads to smaller possible channel lengths and therefore to a better scalability [6] of the cell. In 0.13µm technology and below channel erase is becoming more important.

Fig.3 shows the schematic of a NAND array and the cross section of a few NAND cells. Again the cell consists of a MOS transistor with an additional floating gate in between the channel and the control gate. Programming and erasing is done using Fowler Nordheim tunneling from and to the channel. This leads to much longer programming times of typically a few 100s of microseconds and higher required voltages than in the NOR cell (up to 20V). The programming current, on the other hand, is much lower than for channel hot electron programming, making it possible to program a much larger number of cells in parallel and achieve much faster effective programming speed if single byte programming is not required.

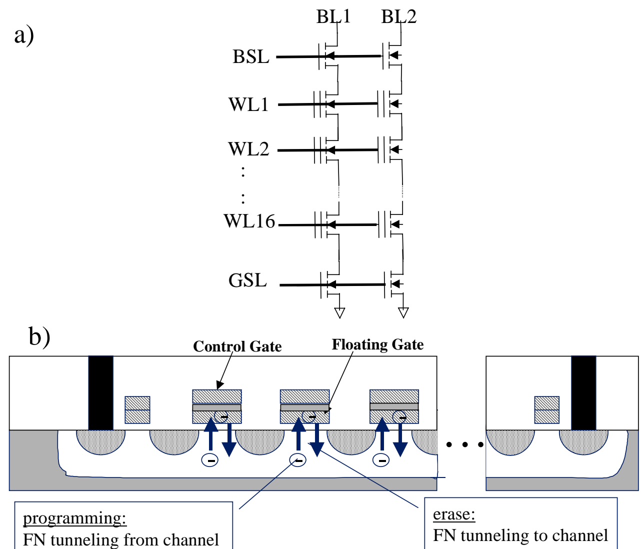

Fig 3. NAND Flash Array (a) and typical NAND Flash cell (b)

The main advantage of the NAND architecture is the very small effective cell size due to the fact that no contacts are necessary between individual cells. This is paid for by a much larger random access time than in the NOR case. Therefore NAND memories are used where large amounts of data that are accessed in larger portions (e.g. pictures, music etc.) have to be stored. NOR Flash memories, in contrast, are primarily used for code storage. To be competitive in the standalone memory market the cell size has to be as small as possible. One way to reduce the effective cell size is to store more than one bit in a memory cell (Multi Level Cell = MLC) [7]. This approach is implemented in NOR [8,9] as well as NAND [10] Flash Memories, but it has the drawback of a reduced write and read performance.

An alternative way to store two bits in one memory cell is to store one bit on each side of a charge trapping device. In this multi bit approach the second bit in a cell can be accessed simply by reversing the direction of the cell and therefore causes no performance drawback. Combined with a virtual ground NOR array, this approach leads to effective bit sizes of about 3-4F^2 (F is the minimum feature size of the manufacturing process) which is roughly 30% of the bit size of a conventional 1 bit NOR Flash.

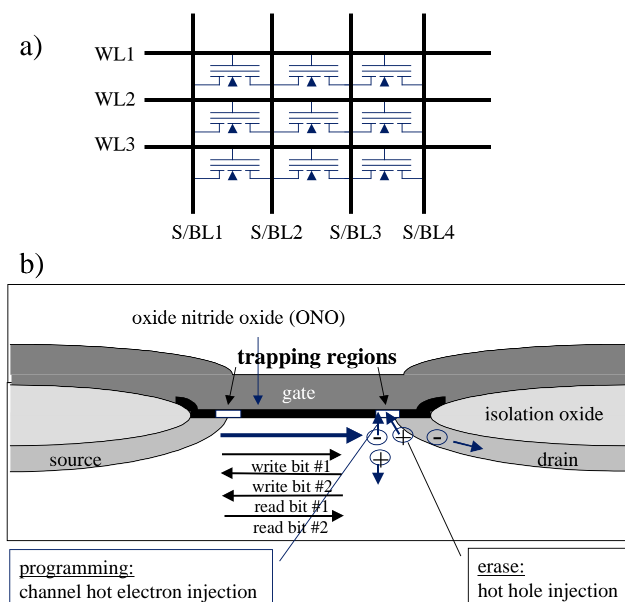

Fig 4. Multi bit charge trapping device a) virtual ground array b) cross section of cell

Fig 4 shows a typical multi-bit charge trapping device [11]. The device is programmed using channel hot electron injection and erased by hot hole injection. The hot holes are generated using band to band tunneling at the respective junction. By reading the device in reverse mode compared to programming and using a sufficiently large drain voltage, the effect of the second bit can effectively be suppressed. Many research and development activities are currently observed with multi bit charge trapping devices [12,13,14] and first high density products are beginning to appear [15].

Due to the high energy barrier required, which leads to rather thick oxides (>8nm for the tunneling oxide and >15nm effective thickness for the ONO) and high voltages during program and erase conventional charge storage devices are facing serious scaling limits below 100nm ground rules [16]. To overcome these scaling limits and to address some of the other issues associated with charge storage devices, a number of alternative devices is investigated. One way to address the scaling limit is to use a device with a vertical channel. Two options namely a pillar type device [17] and a trench type device [18] have been proposed.

The scaling limit as well as the low write performance and limited endurance can be addressed by using thinner tunneling barriers. To overcome the retention problems of such an approach a combination of different materials as tunnel oxide is used in crested barrier devices [19] and a Coulomb blockade effect is utilized in nanocrystal devices [20]. The latter approach uses nanocrystals of silicon or germanium in a matrix of silicon dioxide rather than a massive floating gate. High programming speed of 1µs, low programming and erase voltage [21] as well as significantly higher write erase endurance up to 10^{11} cycles [22] have been demonstrated for such nanocrystal devices. However, sufficient nonvolatile retention remains to be proven in approaches with very thin tunneling oxides.

Another way to overcome the write/erase speed and endurance issue is to use a device that is merged with the actual storage device that will allow to lower the potential barrier during writing and erase and maintain the high barrier during storage. Memories called PLEDM (Phase State Low Electron Drive Memory) [23] and STTM (Scalable Two transistor Memory) [24] by the respective authors are memory cells that apply this concept by using multiple tunnel junctions covered by the control gate and an additional signal line to supply the charge during write and erase. Again the nonvolatile retention of these devices is not demonstrated yet.

In Proton Memories a protonic charge is introduced into the gate oxide of a MOS transistor during fabrication. This charge is then moved inside the oxide only during program and erase making it unnecessary to inject charge during program and erase [25]. The stability of the protons inside the gate oxide at elevated temperatures is still questionable for this approach.

3. NONVOLATILE MEMORIES BASED ON INORGANIC MATERIALS

A lot of experimental research effort and modeling has been spent on new memory technologies based on inorganic materials [26,27]. These memory mechanisms include the use of ferroelectric, magnetic and material phase change to store bit information. Most of these memory options are aspired to merge into a CMOS technology platform by adding modules to a standard CMOS process flow, so that these concepts are generally thought to be converted to competitive products in the next few years. These additive modules may be realized as switchable capacitors or resistors with different reading and writing schemes. In order to implement highest memory density, passive crossbar arrays instead of active transistor cells can be generated, having the advantage of a lower cell size but requiring a read out by a complex periphery thus compromising memory performance.

Ferroelectric memory technology [28] is based on the electric dipole switching of a certain class of materials. These crystalline ferroelectric materials can be remanently programmed in two different states by simply applying an electrical bias to the films. This electric field causes mobile ions to align along the applied field. Moreover, the individual unit cells of the crystal interact with their neighboring cells to form ferroelectric domains in the material. The nonvolatility is based on the fact that the majority of the polarized domains will retain their polarization state along the external field after removing it. A perovskite unit cell of a ferroelectric material and a typical hysteresis curve is shown in Fig.5.

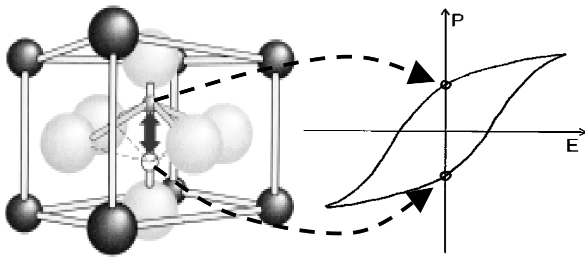

Fig.5 Perovskite unit cell of ferroelectric material and polarization (P) hysteresis curve in external electric field (E), schematic drawing

Common ferroelectric materials, which seem suitable for memory applications, are $PbZr_xTi_{1-x}O_3$ (PZT), $SrBi_2Ta_2O_9$ (SBT) and $(Bi,La)_4Ti_3O_{12}$ (BLT). There are different approaches to implement these ferroelectric materials into a memory cell, some of which are shown in Fig.6. A common approach is to use a 1T/1C cell, which is similar to a DRAM cell and consists of one ferroelectric capacitor being addressed by a transistor. In order to sense the polarization state of the ferroelectric film in a capacitor, a switching of the polarization is required. Depending on the polarization state of the ferroelectric film a small or a large amount of charge will flow in the circuit. The initial state can be identified by comparing this signal to that of a suitable reference. However, a write back cycle is necessary in this cell concept in order to restore the initial read information. There are also concepts to realize non destructive read out cells, one of which is the 1T Ferroelectric Field Effect Transistor (FeFET) cell [29]. This cell type is a MOS transistor, where the gate oxide is replaced by a ferroelectric film thus giving the possibility of nonvolatile data storage in an extremely compact cell. The read out is – like in a Flash cell – performed by sensing the source drain current, which is dependent on the threshold voltage given by the polarization state of the ferroelectric gate layer. Another approach, which connects a select transistor and a capacitor in parallel and arranges these cells in a chain of 8 or 16 cells has the potential of $4F^2$ cells. This chain FeRAM (CFeRAM) approach, combined with a rather large offset capacitor, was used to demonstrate an 8M device [30].

Ferroelectric materials show some specific reliability issues, one of which is the decrease in switching polarity with the number of performed switching cycles. This so called fatigue phenomenon depends on the material, its deposition and the choice of the electrodes used for the integration. After a high number of switching cycles (typically 10^9-10^{12}) one observes a gradual decrease in the remanent polarization P_r, which is generally attributed to a decrease of the domain wall mobility. Another issue is that the capacitor has the tendency to prefer a state, in which it has been stored for extended periods of time. This so called imprint phenomenon can lead to a failure if the opposite state is written into and subsequently read from the capacitor. Nevertheless, ferroelectric memories for low density applications have been produced [31], however high density memories have not hit the market so far.

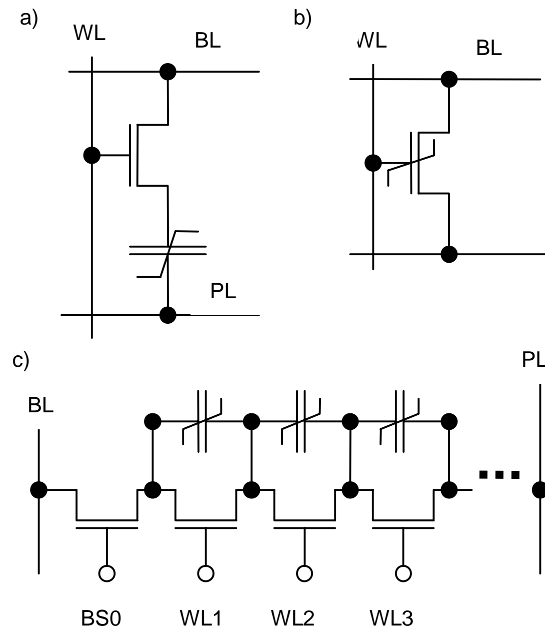

Fig.6 Cell concepts for the integration of ferroelectric memories into CMOS. a) 1T/1C, b) 1T Ferroelectric Field Effect Transistor, c) Chain FeRAM

For the realization of magnetic random access memory (MRAM) three different physical effects, namely anisotropic magnetoresistance (AMR), giant magnetoresistance (GMR) and tunneling magnetoresistance (TMR) are potential candidates [32,33]. AMR was used for the first MRAM products but is obsolete today due to the very low resistance change. The GMR effect is based on the spin dependent interface scattering of charge carriers in a sandwich structure of a conducting layer embedded between two magnetic layers. A resistance change of up to 6% is observed between the case, where the two magnetization states are in parallel and the case, where they are anti parallel. If one magnetic layer is pinned and the other is free to switch its magnetization, the structure is referred to as a spin valve (SV). By modifying the cell design and the reading sequence a pseudo Spin valve (PSV) can be constructed leading to a doubling of the observed resistance change [34]. But like with AMR cells, GMR based cells consist of all metal structures leading to low resistance cells, which are not favorable for high density memories.

Finally, in the tunneling magneto resistance cell concept a Magnetic Tunnel Junction (MTJ) is used, where the tunneling current from one ferromagnetic layer to another through a very thin insulating layer is dependent on the magnetic state of the two ferromagnetic films as sketched in Fig.7. In this MTJ cell concept the current flow is perpendicular to the layers of the structure whereas in the SV and PSV cell it is in plane. The resistance of an MTJ can be adjusted by increasing the

thickness of the tunneling barrier. The resistance change between the case, where the two magnetization states are in parallel and the case were they are anti parallel is about 30-50% [35]. This number is quite low compared to other memory concepts, which will be discussed later in this article.

The MRAM cells are written by current pulses through the bitline and the wordline in order to generate a magnetic field H_c, which is large enough to switch one of the ferromagnetic layers (called free layer), but not large enough to switch the second magnetic reference layer. The difference in H_c is generated by pinning the reference layer to a antiferromagnetic layer. The magnetic domain switching and thus the writing time of the cells is in the range of a few ns and there is no endurance limit expected like it is observed in ferroelectric materials, since the electronic spin flipping mechanism does not degrade with continuous cycling.

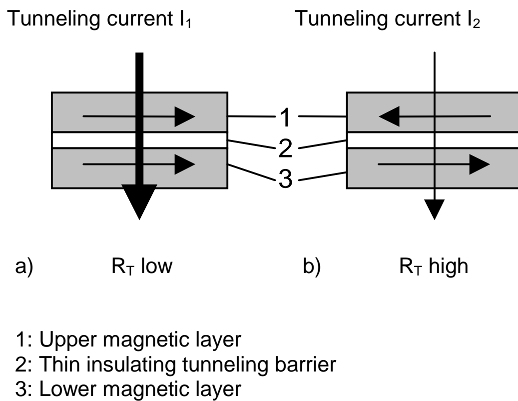

Fig.7 Magnetic Tunnel Junction cell with a) magnetization aligned in parallel and b) magnetization spins aligned anti parallel

MRAM has some challenges, which should be discussed briefly. The integration of the magnetic stack is a very critical issue due to the exact thickness definition of the insulating tunnel layer, which is required to avoid on-die array nonuniformity and to avoid shorting the tunneling electrodes. As the critical switching field (and thus the current density in the word line) becomes even larger upon shrinking the width of the cell size, a method for scaling the word line current has to be engineered in order to avoid electromigration and cross talk of neighboring cells. One way of decreasing the critical switching field is to use very thin magnetic layers, however, this again leads to reliability problems, especially at increased temperatures due to thermal fluctuations of the magnetization [36].

Phase Change Memory is another interesting competitor in the class of nonvolatile memory contenders. This concept is based on the reversible phase change between the amorphous and the crystalline phase of a chalcogenide glass [37]. These two physical states of matter differ in their resistivity, as the conduction is generally much better in a crystalline chalcogenide than in an amorphous one due to the reduced scattering of charge carriers in films with atomic long range order. The transition from the crystalline to the amorphous state is performed by applying a very short electrical pulse to the a resistive heater in contact with the phase change material thereby melting (typical melting temperature is about 600°C) it and thereafter rapidly cooling it below the glass transition temperature to freeze the amorphous phase. In order to write the crystalline state into the cell a lower but a little bit longer pulse is applied, thereby heating the material over the critical crystallization temperature (about 300°C in materials typically used) and leaving it in the low resistivity polycrystalline phase. Typical currents for setting and resetting the cell are about 100µA and 1mA, respectively [38]. The difference in resistivity of the two phases is about 1-2 orders of magnitude, which is considerably higher than in MRAM. The writing mechanism also allows the realization of Multi-Level-Cell (MLC) data storage by programming the cell to intermediate resistance levels, thus yielding a lower fraction of the crystalline phase. Reading is accomplished by measuring resistance changes in the cell. A simplified cross section of such a phase change memory cell is shown in Fig.8.

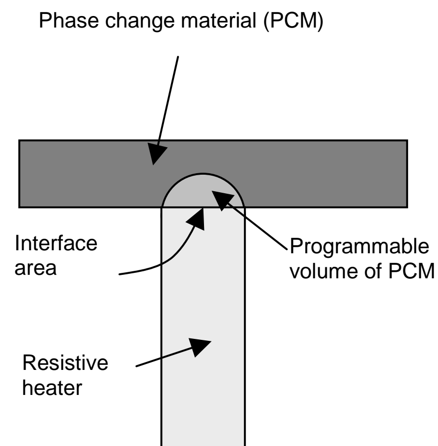

Fig.8 Simplified cross section of a phase change memory cell

The most promising candidates for phase change memory applications are the chalcogenide Ge-Sb-Te or Ag-In-Sb-Te alloys, which are also used in rewriteable CD and DVD optical memories [39]. These films exhibit good performance for memory applications, because the phase transition in these materials is very fast occurring in a few nanoseconds and can be repeated for about 10^{12} write/erase cycles [37]. Another advantage of the proposed memory concept is the small cell size (which is about 5-8F²) [38] and the scalability: By scaling down the cell the energy required for the phase change and thus the writing and erasing current decreases.

The recently reported resistance switching in perovskite materials is another candidate for nonvolatile memory applications [40,41]. The effect is based on a

large change in electrical resistance, if a perovskite material is exposed to voltage pulses. These materials are typically oxides having a perovskite crystal structure, some of which show the colossal magnetoresistance (CMR) effect, the best known ones are (Pr,Ca)MnO_3 [41] and Cr-doped $SrTiO_3$ and $SrZrO_3$ [42]. However, for this recently discovered reversible switching no clear physical explanation has been given so far. The relative conductance change can be as much as several orders of magnitudes. It is thus comparable to the ratio observed in phase change materials, however, in this case the electrical field only affects the electronic structure of the films, whereas the crystal structure remains unchanged during switching. Typical switching times are well below 100ns. By applying various pulse lengths and heights or by varying the number of pulses, it is possible to program the film into intermediate resistance levels thus enabling multi level cells. From the viewpoint of switching endurance and data retention this concept is very promising, however, there is still very little data available.

A new memory concept, which is also based on resistance change of an active material, was introduced lately. This so called programmable metalization cell (PMC) consists of an oxidizable anode and an inert cathode encapsulating an amorphous solid state electrolyte [43]. In the unprogrammed state this cell has a high resistance, however, by applying an external voltage to it, metal cations formed in the anode diffuse into the electrolyte and thus metallic dendrites form through the film. This effect is due to the fact that metals such as Cu or Ag can dissolve in chalcogenide glasses such as As_2S_3 or GeSe, which are generally used for the realization of a PMC [44]. So, by the formation of the bridging metallic electrodeposit the electron conduction is largely increased thereby changing the overall resistance of the cell. Again, the relative change in the proposed cell can be as high as several orders of magnitude. Other advantages of this concept are low-voltage and low power capabilities.

4. ORGANIC MEMORIES

Instead of using an inorganic switching material an organic material is also possible. The advantage of organic materials lies in the fact that the properties of organic materials can easily be tailored. The main drawback is that usually the stability – especially the temperature stability – is limited. Therefore organic materials are usually limited to memory concepts that are processed in the back end of line (BEOL). The processing in BEOL, on the other side, introduces the possibility to stack several memory layers on top of each other and drastically increase the memory density. In Fig. 9 the principal arrangement of such a three dimensional (3D) stacked organic hybrid memory is shown. The Si chip includes all the CMOS circuits necessary to operate the array. These can be placed under the array resulting in a very high cell efficiency. The organic memory layers are stacked on top of each other separated by insulators. In Fig. 9 every electrode is used for one memory layer only. Depending on the switching effect used, electrodes may also be shared among different memory layers reducing the processing steps for the memory array [45].

In this paper we discriminate between organic memories, which are memories using bulk switching effects in organic materials, and molecular memories which use the properties of a single (usually also organic) molecule. The latter will be covered in the following section.

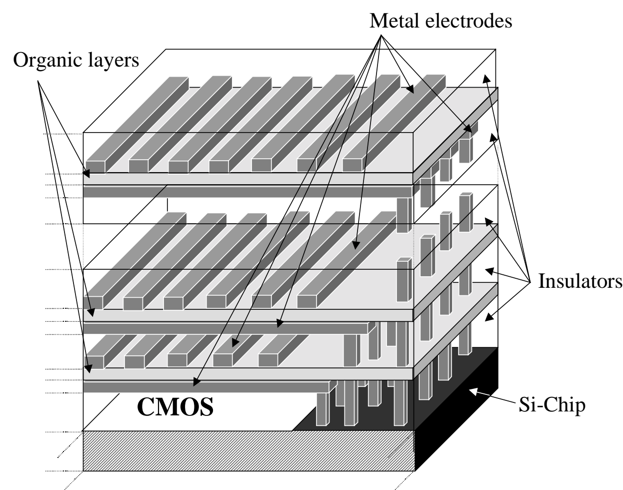

Fig. 9 Principal arrangement of 3D stacked organic memory

For organic memories either ferroelectric switching or conductance switching is used. Ferroelectric Polymers have much lower permittivity and much slower switching speed than inorganic ferroelectrics [46,47]. This may lead to the possibility of realizing the above mentioned pure cross point arrays which were not successful with inorganic ferroelectrics [31]. The slow switching speed can be compensated for by massive parallelism in high density data storage applications like digital cameras, MP3 players or digital videos.

For resistance switching a number of different concepts have been published. Krieger et al. have proposed the use of structural electronic instability in one-dimensional molecular systems. [48]. In a concrete realization they used a polyconjugated compound (polyphenylacetylene) with 5-7% of potassium chloride By applying an electrical field the sodium and chloride ions are separated and form conducting complexes with the one-dimensional molecular system. Fast switching, 10^8 cycles, retention of 1.5 months as well as a multi level cell storing 4 different resistance values were demonstrated [49, 50].

Potember et al. proposed an electrical induced phase transition in Charge transfer complexes like silver and copper tetracyanoquinodimethane (TCNQ) salts as another class of material showing promising switching behavior [51]. Recently a structure consisting of Al/AIDCN/Al/AIDCN/Al (AIDCN: 2-amino-4,5-

imidazoledicarbonitrile) was proposed by Ma et al. [52]. The interesting aspect about this approach was that an additional floating metal layer was needed to achieve the desired switching effect. Although the switching mechanism is not fully understood in detail, the structure shows very promising memory characteristics.

A large number of other materials showing resistance switching effects have been reported in the literature [53, 54, 55]. In most cases further work will be required to achieve stability and switching properties that are suitable for memory applications. On top of the pure electrical approaches there are also approaches that use combinations of electrical and optical writing and reading effects [56]. The integration of these effects into high density memories still has to be proven.

5. MOLECULAR MEMORIES

The term molecular memories contains a wide variety of different materials and concepts all of which using individual molecules as building blocks for memory cells storing bit information in the space of an atom or a molecule. The term molecular memory should be interpreted in such a way, that these memory elements make use of physical effects which occur in a single molecule involving quantum mechanical effects. In fact it is not necessary to establish an electrical contact to one single molecule, but it is generally more convenient to create a monolayer (ML) film consisting of a large number of functional molecules and thereafter contacting these films by depositing an electrode layer on top of it. However, these types of memories have the potential to be scaled down to use only one single molecule for memory operation.

One example for molecular memories is the rapid reversible conductance switching of molecules attached between two electrodes which can be controlled by the applied voltage. Using this approach, Rotaxane molecules were investigated by Collier et al. [57]. Though a reasonable on/off ratio has been proven, it has also been found that these molecules were only programmable once. However, by introducing redox centers to molecules Reed and Tour showed, that it is possible to produce a large reversible switching behavior [58,59]. By using a self assembled monolayers of these molecules and embedding them into an Au/molecular ML/Au electrode structure a fast and reversible resistance switching with a thermally activated decay time of about 10^3 seconds at room temperature was achieved. The retention is thought to depend on the energy barrier given by the thiol/Au contact. The exact mechanism for the conductivity change is still under investigation. However, it is believed, that the charge transfer to or from a molecule alters its geometric form and thereby its electronic orbital structure. Another concept based on Multiporphyrin nanostructures uses a redox reaction to store charge in the molecule as the basic operational principle. The effect has been demonstrated in liquids [60] but no solid state realization of this concept is known so far.

Nanoelectromechanical nanotube memories are a crossbar arrangement of carbon nanotubes using switchable bistable device elements with well defined on/off states [61]. The proposed memory array consists of single walled nanotubes arranged in parallel rows lying on an insulating substrate. These rows are crossed by perpendicularly arranged nanotubes, which are suspended from periodic supporting pillars. Memory functionality is based on the electrostatic forces which act in between transiently charged nanotubes. Attractive or repulsive electrostatic forces can bring the nanotubes in contact or separate them, where the resistance at a matrix crosspoint is by some orders of magnitude lower if the two nanotubes are in contact. The degree of mechanical strain required for bistability is well below the elastic limit of the material. Though this type of memory could lead to ultrahigh density of 10^{12} elements per square centimeter and to very high operation frequencies [61], no procedure for defined manufacturing is known yet.

Finding of adequate deposition methods and tayloring the chemical properties of the materials are subject of the current research on molecular memories, however the characterization and optimization will certainly require much more time. Especially the thermodynamic stability of the different molecular states and the reaction kinetics have to be studied in more detail in order to give a deeper insight in the suitability of such molecules for their application in nonvolatile memories. Another difficult aspect is the formation of a well defined metallic contact to the molecules or molecular arrangements in order allow a reliable reading and writing.

6. SUMMARY AND CONCLUSIONS

Today the vast majority of nonvolatile memories are based on charge storage. Due to the intrinsic limitations of this approach, novel materials with new switching effects are currently investigated to develop new memories. The aim is to either realize a memory that can be operated like a DRAM or SRAM and additionally exhibits nonvolatility, or to realize a considerably higher density of nonvolatile memories than the currently available ones.

Inorganic materials are simplest to integrate into an existing CMOS process. Ferroelectric, magneto-resistive and phase change memories are three candidates to realize a genuine nonvolatile RAM. Ferroelectric memories in low densities (currently up to 256kb) are available on the market for many years [31] and demonstrators up to 32M in density have been published [62]. With MRAM a first 1M demonstrator was recently published [63] and products are expected soon. The success of these two technologies for high density memories depends on how quick the existing integration and scaling issues can be solved. Phase change memories,

in contrast, seem to have less integration issues. On the other hand the phase change memory concept has a number of open questions with respect to the stability of the electrode/chalcogenide interface as well as the thermal isolation between neighboring bits. The realization of a 4M test chip has already been published [38] and the way to higher densities seems to be open if the basic issues can be solved. All the other concepts using inorganic switching materials are still in a much more basic development stage and more data will be required to judge the likelihood of realizing high density memory products in the near to mid term future.

The integration of organic materials could open the path to much higher densities compared to the present memory concepts which are feasible with conventional semiconductor manufacturing techniques by utilizing the concept of three dimensional (3D) stacking. Ferroelectric polymer memories (PFRAM) seem to be a very promising candidate in this arena, although very little information is published on the actual status and performance [45]. For a realization using resistance switching, a large number of materials have been proposed in the literature, but only a few have demonstrated adequate characterization data for memory applications [49, 52]. On the long run an organic memory could be combined with organic electronic leading to an all organic memory device (see fig. 1) which could drastically simplify the fabrication of such devices.

Molecular memories based on quantum mechanical effects in single molecules or on carbon nanotubes are still in a very basic stage. Fundamental fabrication and integration issues will have to be solved before we can expect first products. The advantage would be the very small feature size such a memory cell could be fabricated on. Additionally – like with organic memories – in the far future also the electronics could be fabricated using molecular devices, again leading to a much easier fabrication.

For the nearest future, however, classical devices based on charge storage will continue to dominate the market. As a serious contender to floating gate devices, multi-bit charge storage devices could find widespread application very soon. To overcome the severe scaling limitations of charge storage devices some of the concepts now discussed for future charge storage devices (e.g. modified tunneling barriers) as well as vertical devices [17,18] may also be implemented into charge storage devices in the near to mid-term future.

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Thomas Mikolajick was born in Nuremberg, Germany in 1963. He received his Dipl-Ing. degree in Electrical Engineering in 1990 and his Dr.-Ing. Degree in 1996 both from the University of Erlangen-Nuremberg. In 1996 he joined Siemens Semiconductor (now Infineon Technologies) working on process integration and electrical characterization of CMOS technologies. From 1999 till 2000 he was working on integration of ferroelectric memory devices. Since 2000 he is working on future nonvolatile memory technologies. His main research interests are memory devices, CMOS devices and electrical and physical device characterization.

Cay-Uwe Pinnow was born in Kiel, Germany in 1974. He received his Dipl.-Phys. degree in 1999 and his Dr. rer. nat. degree in 2002 both from the University of Göttingen. From 1999 to 2002 he worked on the integration of ferroelectric materials into CMOS as a Ph.D. student for Infineon Technologies in Munich. Since 2002 he is working on future nonvolatile memory technologies. His main research interests are novel memory materials and devices, especially ferroelectric devices and their integration.