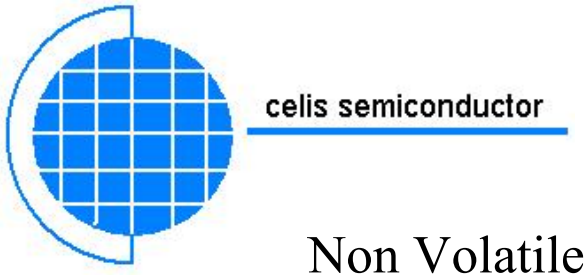

Non Volatile Memory Technology Symposium
7 - 8 November 2001
San Diego, California

Future Development of Dense Ferroelectric Memories for Space Applications

Stephen C. Philpy and Gary F. Derbenwick,
Celis Semiconductor Corporation
5475 Mark Dabling Blvd., Suite 102
Colorado Springs, Colorado 80918

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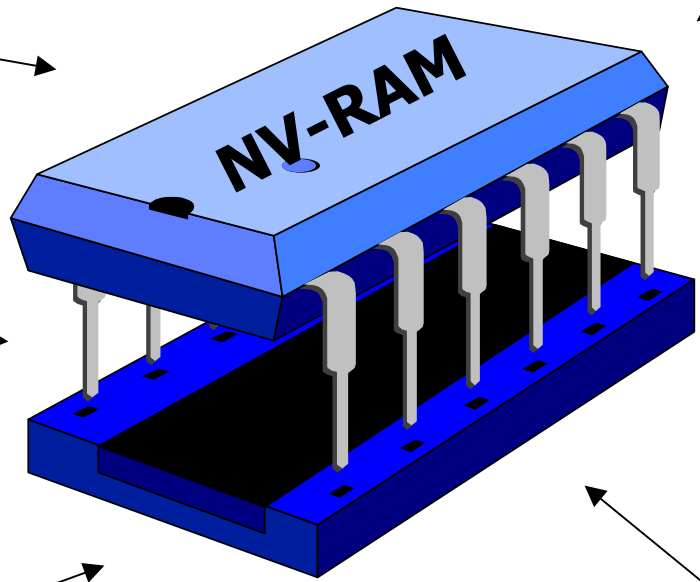
The Ideal Non-volatile Memory!



Excellent Reliability

Fast Programming

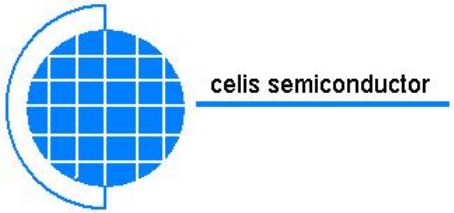
Unlimited Retention

Low Voltage

Small memory cell

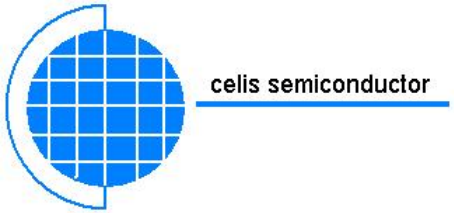
Unlimited Endurance

Radiation Hardness for Hi-Rel



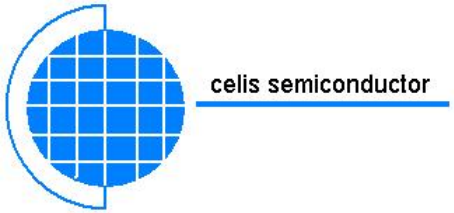
FERROELECTRIC MEMORY COMMERCIALIZATION

COMPANY	PRODUCTS
Fujitsu	Embedded 64k-bit ferroelectric memory
Matsushita	1k-bit embedded ferroelectric memory in RFID chip
Ramtron	4k-bit FRAM®, 16k-bit FRAM®, 64k-bit FRAM®, 256k-bit FRAM®
Rohm	16k-bit ferroelectric memory



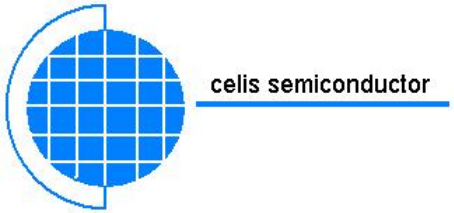
OTHER FERROELECTRIC DEVELOPMENT ACTIVITIES

COMPANY	ACTIVITY
Hitachi	R&D
Hughes/Raytheon	R&D flip-chip Fe capacitor stack
Hynix	Prototype 64k to 1M-bit FeRAM Development
Infineon/Toshiba	Stacked 1T/1C 8M-bit and 64M-bit FeRAMs
Mitsubishi	R&D
NEC	Prototype embedded FeRAM
OKI	R&D
Samsung	4M-bit FeRAM R&D
Seiko-Epson	R&D
Sharp	High density FeRAM R&D
Sony	R&D 1T
STMicroelectronics	R&D consortium with IMEC
Texas Instruments	R&D embedded FeRAM at 0.18 / 0.13 micron



HIGH DENSITY FeRAM COMMERCIALIZATION ISSUES

- PZT – Focus is on high temperature retention instead of stacked memory cell development
  - Special electrodes/dopants needed for >10^9 endurance
- SBT – High temperature ferroelectric phase formation / process integration
  - Oxidation of poly plug / barrier metal
- Large Cell Size
  - Offset memory cell (Fe capacitor over field oxide)
  - 2T/2C (sense amplifier reference for 1T/1C is difficult)
- Contamination (Fe layer must be sealed)
- Technology generation is not advanced
- Funding level (total FeRAM=$500M vs. latest DRAM generation=$10B)



COMMERCIAL FeRAM RADIATION TOLERANCE

Device/Manufacturer	Test Facility	Results*
FM1608/Fujitsu (64k-bit, PZT)	Brookhaven-Heavy Ion	Indeterminate threshold, latchup at 18.7 MeV-cm^2/mg
FM1608/Ramtron (64k-bit, PZT)	Brookhaven-Heavy Ion	Latchup at 22.9 to 37.4 MeV-cm^2/mg
HY8064/Hynix (64k-bit, SBT)	JPL-TID	Failure at 25 krads (Si)
FM1608/Ramtron (64k-bit, PZT)	NASA GSFC-TID	Indeterminate threshold, failure observed at 63 krads (less than 63 krads was not tried)

* See results at: http://klabs.org/memories.htm

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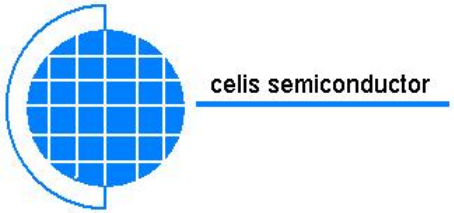
SOLUTIONS FOR HIGH DENSITY RAD-HARD FeRAM

- Three short term solutions
- Two long term solutions



SHORT TERM SOLUTIONS for HIGH DENSITY (≧16 M-bit) RAD-TOLERANT FeRAM

- U.S. rad-hard wafer processing (6-inch wafers) w/split process and stacked thinned-die packaging (0.5 micron, 3 to 5V PZT) (1 to 2 Mrads)

- UTMC CRH wafer processing (8-inch wafers) w/split process and stacked thinned-die packaging (0.35 micron, 3V SBT) (~300 krads)

- UTMC B^2JT transistor design w/split process (8-inch wafers) and Multi-Chip (4 die) Module packaging (0.25 micron, 3V SBT) (3 to 5 Mrads)

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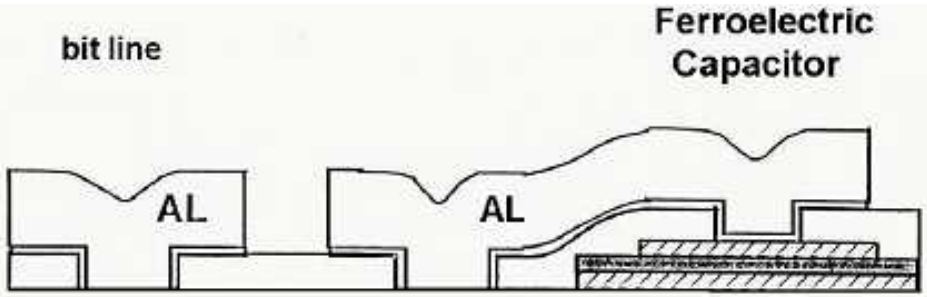
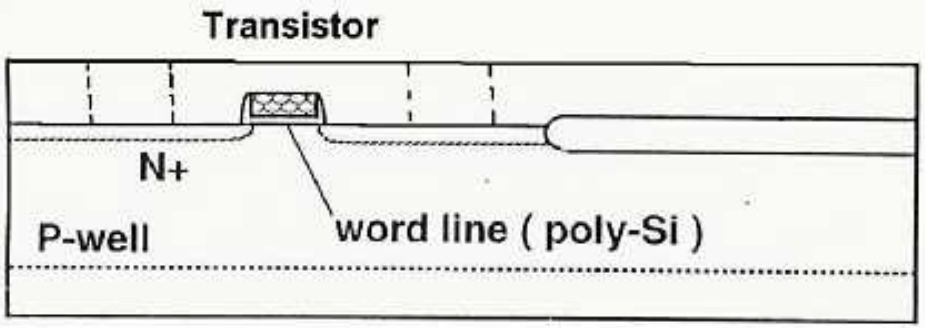
SHORT TERM SOLUTIONS
(SPLIT PROCESS)



FERROELECTRIC FAB

(Ferroelectric Module)



RAD-HARD FAB

(Radiation-Hardened CMOS)

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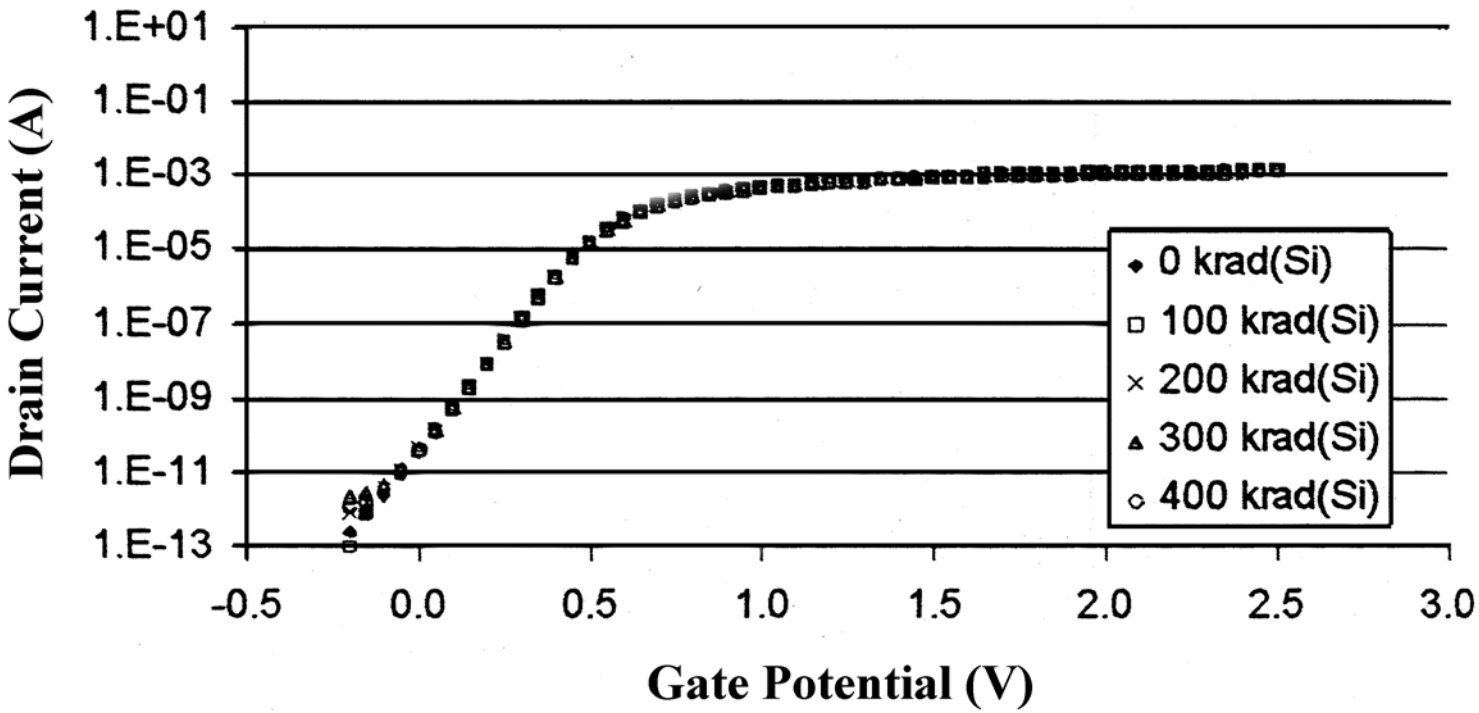
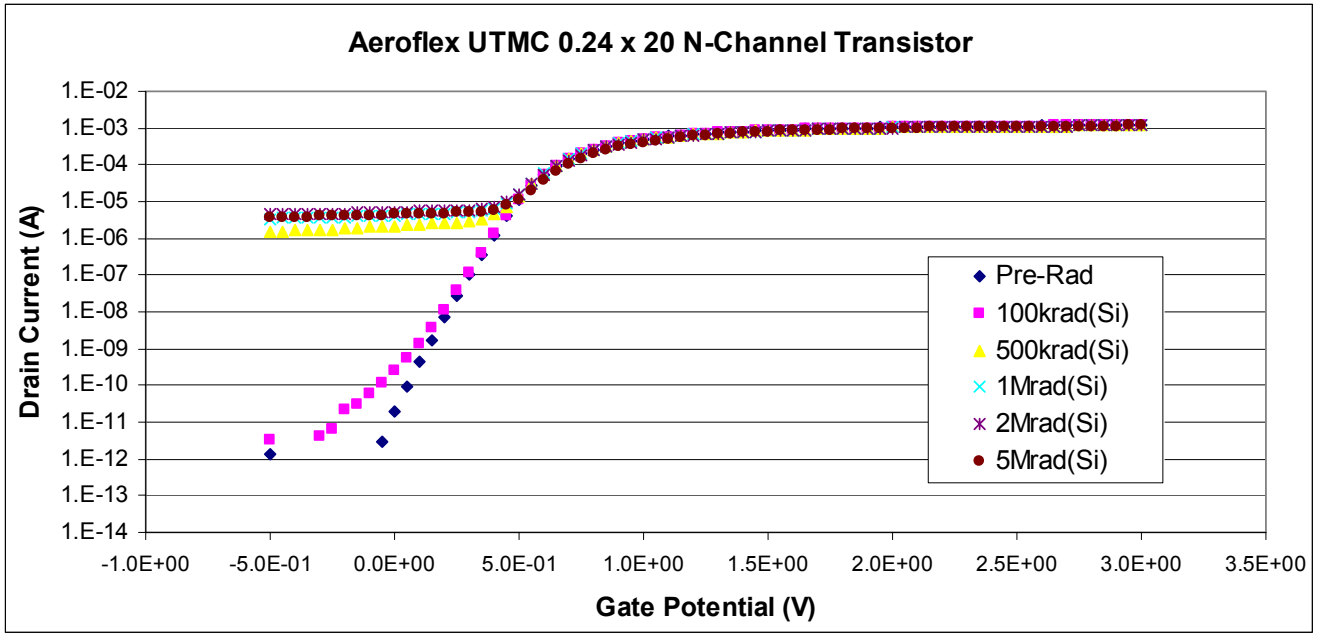
UTMC CRH PROCESS



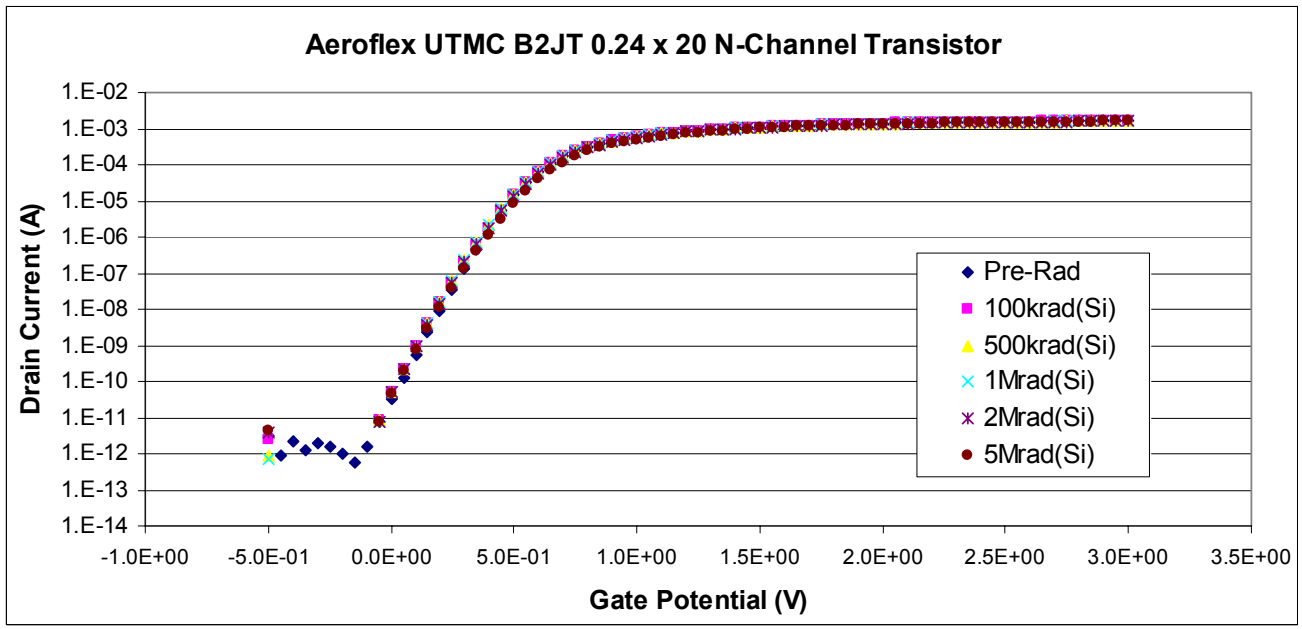
Standard

N-Channel Transistor



B^2JT

N-Channel Transistor



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SUGGESTED SHORT TERM SOLUTION

- Split Process (6-inch wafers)
  - Rad-Hard (underlayer) U.S. foundry (1 to 2 Mrad transistors) (no fabs committed yet)
  - Fe/finishing foundry (Fujitsu - 0.5 micron) (in discussions)
- SEU Tolerant FeRAM Design
  - 1M to 2M-bit, double-level-metal design (3 to 5V PZT) (using reliable Fujitsu 64k-bit core design, >3yr history)
  - 2T/2C Offset Fe Memory Cell
- Stacked Thinned-Die Packaging (e.g. neo-stacking) (Achieve 16M-bit and Greater Densities)
- ~1 Year Development Time

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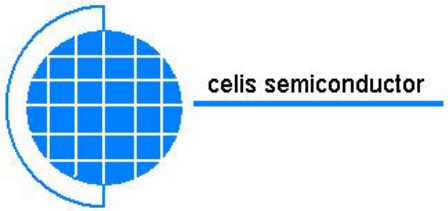
LONG TERM SOLUTIONS for HIGH DENSITY (≧16 M-bit) RAD-TOLERANT FeRAM

- 1T FeRAM fabricated at rad-hard U.S. ferroelectric fab (≤0.18 micron)
- 1T/1C FeRAM (w/stacked cell) fabricated at rad-hard U.S. ferroelectric fab (≤0.18 micron)



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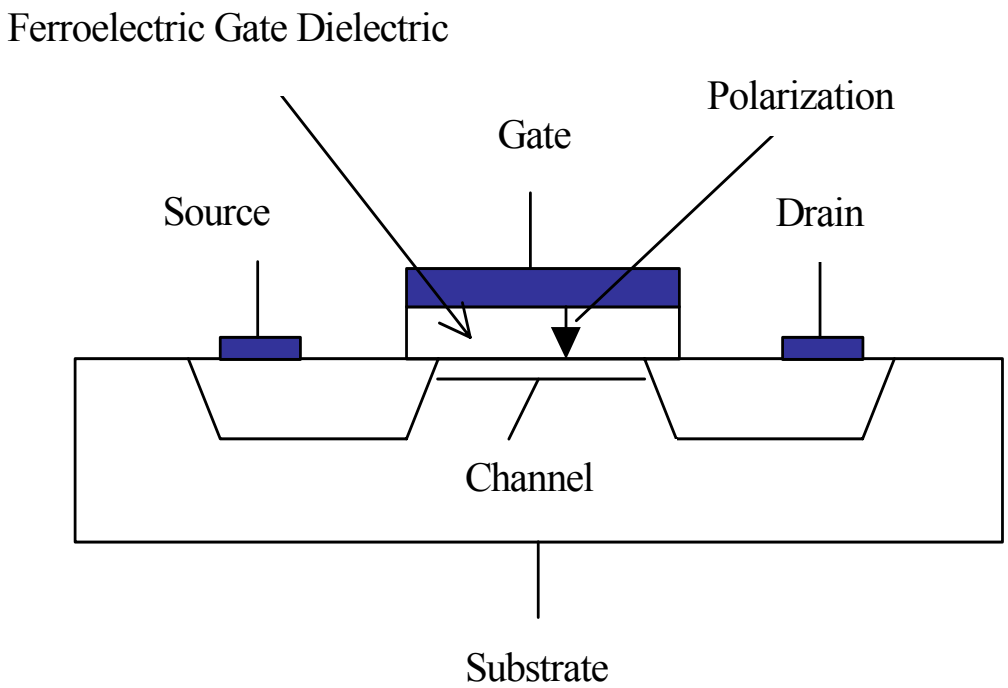
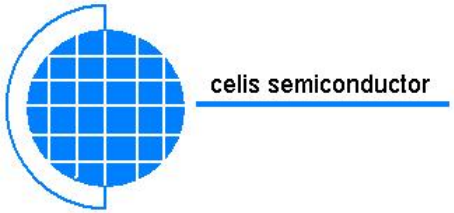
1T Ferroelectric Memory

- Small (~ 5 F^2) ferroelectric FET memory cell
- Non-Destructive Read Out
- Uses breakthrough ferroelectric that integrates well
- Capable of radiation-hardened (>1 Mrad) design
- Low programming voltage (1 to 3 V)
- Low power consumption
- High endurance, fast read/write access

➔Federal Matching Funding Awarded for R&D (NIST/ATP)

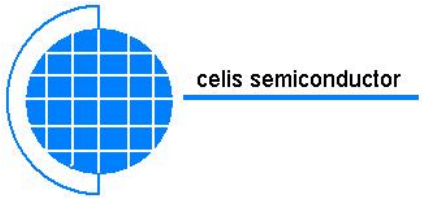
1T Ferroelectric Transistor Cell





Typical Feature Sizes of Memory Cells Compared to 1T FeRAM Cell

Memory Cell Type	Cell Size (F^2)
SRAM	50 to 100
DRAM	7 to 12
Flash	5 to 12
DRO FeRAM (1T/1C)	25 to 75
NDRO FeRAM (1T)	5 to 6 (target)



COVA Technologies

COVA / Celis NIST/ATP 1T Memory Development Plan

YEAR	MAJOR PROJECT TASKS
Oct 2001-Sep 2002	- Materials and Process Development - Cell Design / Layout, Modeling - Define and Design Test Chip
Oct 2002-Sep 2003	- Materials and Process Development (continued) - Array Circuit Simulations - Fabricate Test Chips - Design 1T FeRAM
Oct 2003-Sep 2004	- Fabricate, Test and Characterize 1T FeRAM

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CONCLUSIONS

(HIGH DENSITY RAD-HARD FeRAM)

- **FeRAMs with rad-hard CMOS are well suited for radiation-hardened applications**
- **Split process short term solution**
  - **Stacked-die packaging**
- **Long term solutions**
  - **1T**
  - **1T/1C (Stacked cell)**
- **Celis is active in making both short term and long term solutions possible**
- **Funding is needed to develop short term rad-hard FeRAM**