

Design Hardness Techniques for Radiation Hardened Non-Volatile Memory

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Background

Aeroflex UTMC has successfully engaged with commercial fabrication facilities to produce radiation hardened CMOS at the 0.6, 0.5, 0.25, and 0.18 μ m levels. These results have been presented at various forums over the past few years.

The hardening approach is as follows:

SEU-Cell architecture/circuit design

SEL-Cell Architecture, Layout

Total Dose-Design Rule Modification, Transistor Layout, and/or process modules.

Background

A number of one-time and reprogrammable non-volatile technologies are available in commercial fabs including:

Floating Gate (EEPROM / Flash)

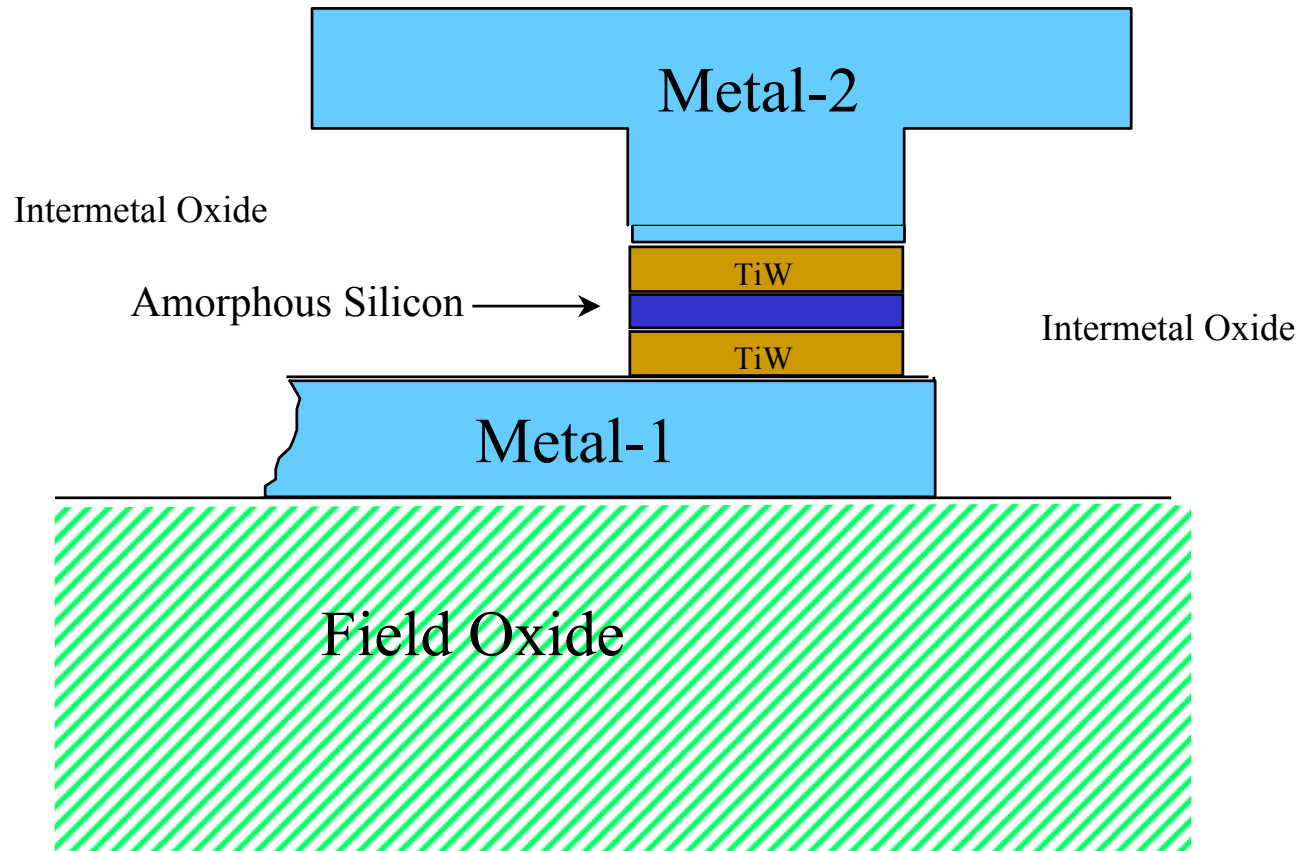
Amorphous Silicon Antifuse

Ferroelectric

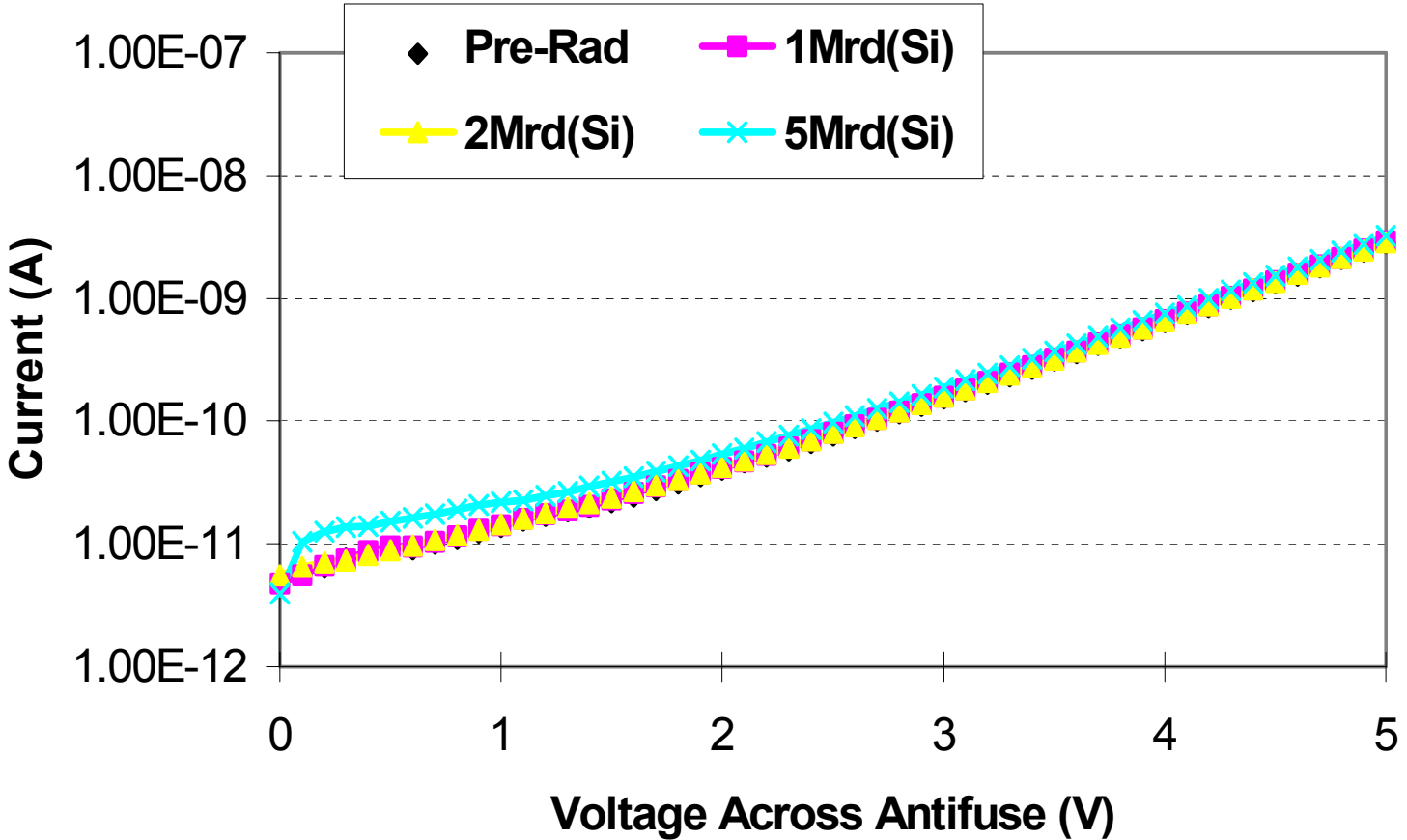
SONOS

Each of these technologies has an intrinsic radiation tolerance from good to excellent.

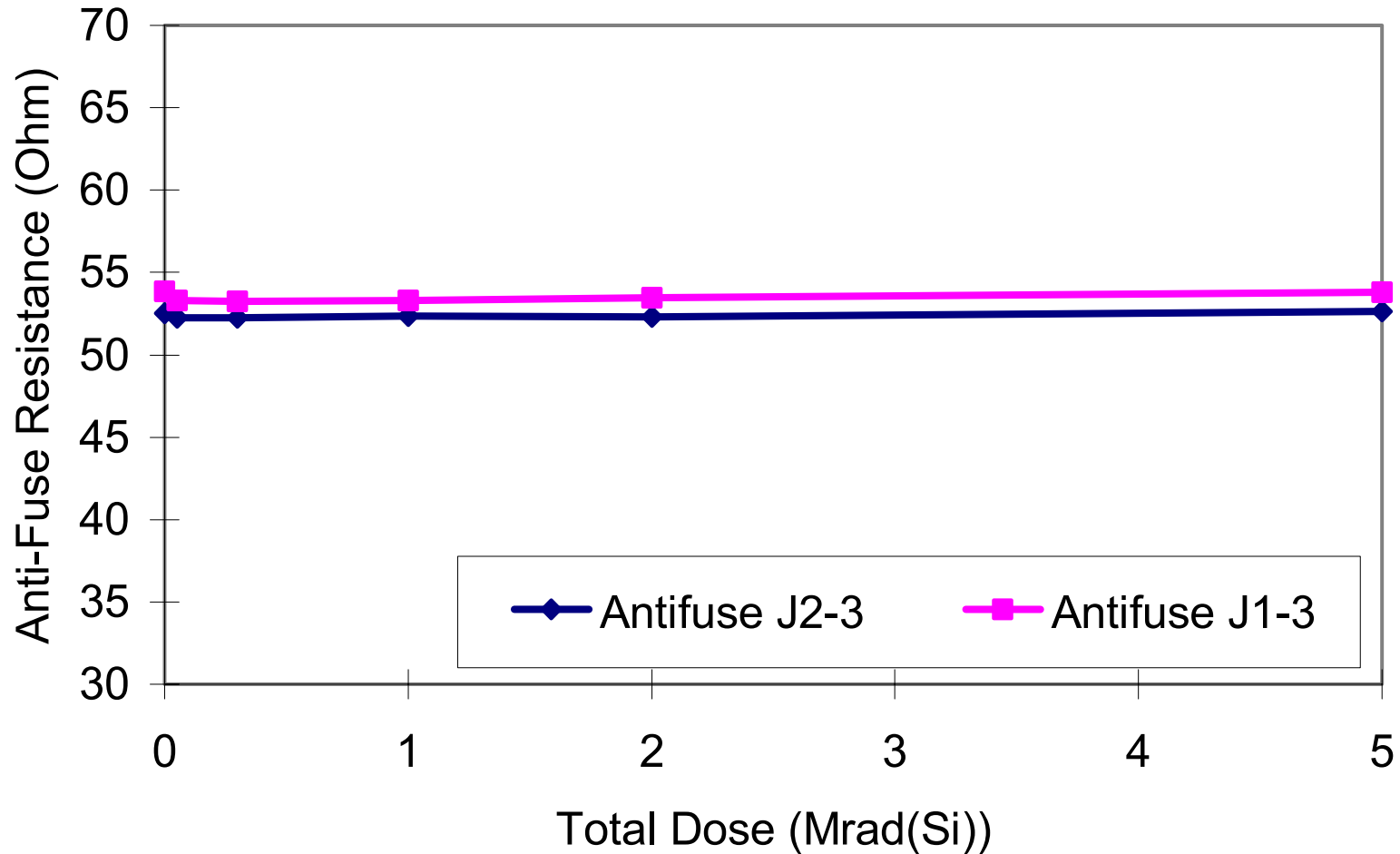
Schematic Cross-Section of an *a*-Si Antifuse



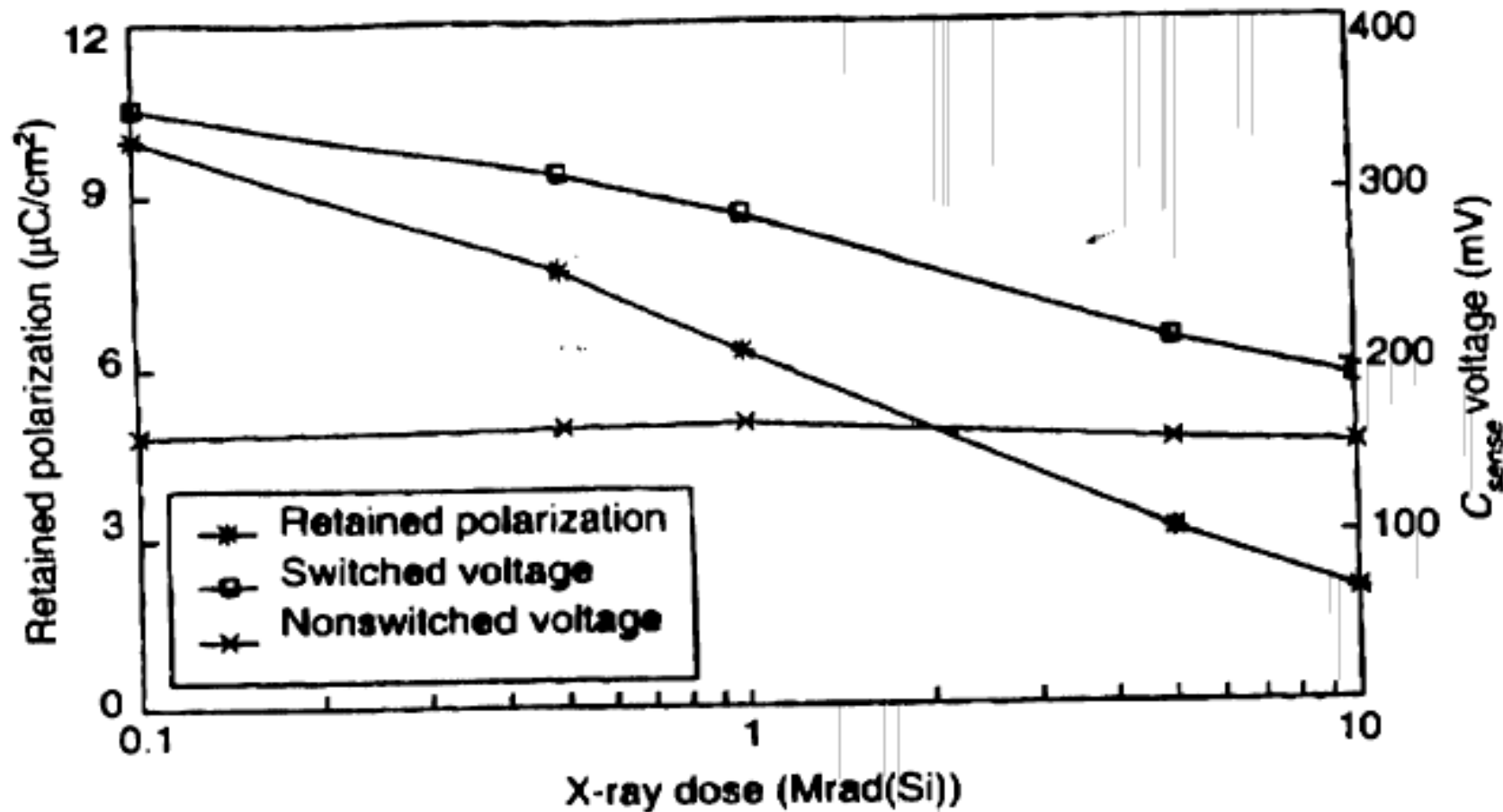
Current-Voltage Characteristics of an Unprogrammed Antifuse Irradiated with a 0V Bias



Resistance of a Fully Programmed Antifuse as a Function of Total Dose



Total Dose Response a Strontium Bismuth Tantalate (SBT) Ferroelectric



FE SEE Data Summary

Device	Ion	Fluence	Angle	Effective LET
RFID Tag #1	Xe	1×10^7	0	64 MeV-cm ² /mg
RFID Tag #2	Xe	1×10^7	0	64 MeV-cm ² /mg
RFID Tag #3	Xe	1.1×10^7	0	64 MeV-cm ² /mg
RFID Tag #2	Xe	3×10^6	45	90.5 MeV-cm ² /mg
RFID Tag #3	Xe	3×10^6	45	90.5 MeV-cm ² /mg
RFID Tag #3	Xe	1×10^6	60	128 MeV-cm ² /mg
RFID Tag #3	Xe	1×10^6	0	64MeV-cm ² /mg

No data loss or loss of reprogrammability was observed

Hardening a Commercial Process via Process Module, Design Rule Modifications, Lay-Out Techniques, and Circuit Design

Pro: Can be used on standard library.

Process Module: **Con:** TID Hardening only, development work

Pro: “Universal” acceptance

Design Rule Modifications: **Con:** Requires custom layout, limited effectiveness

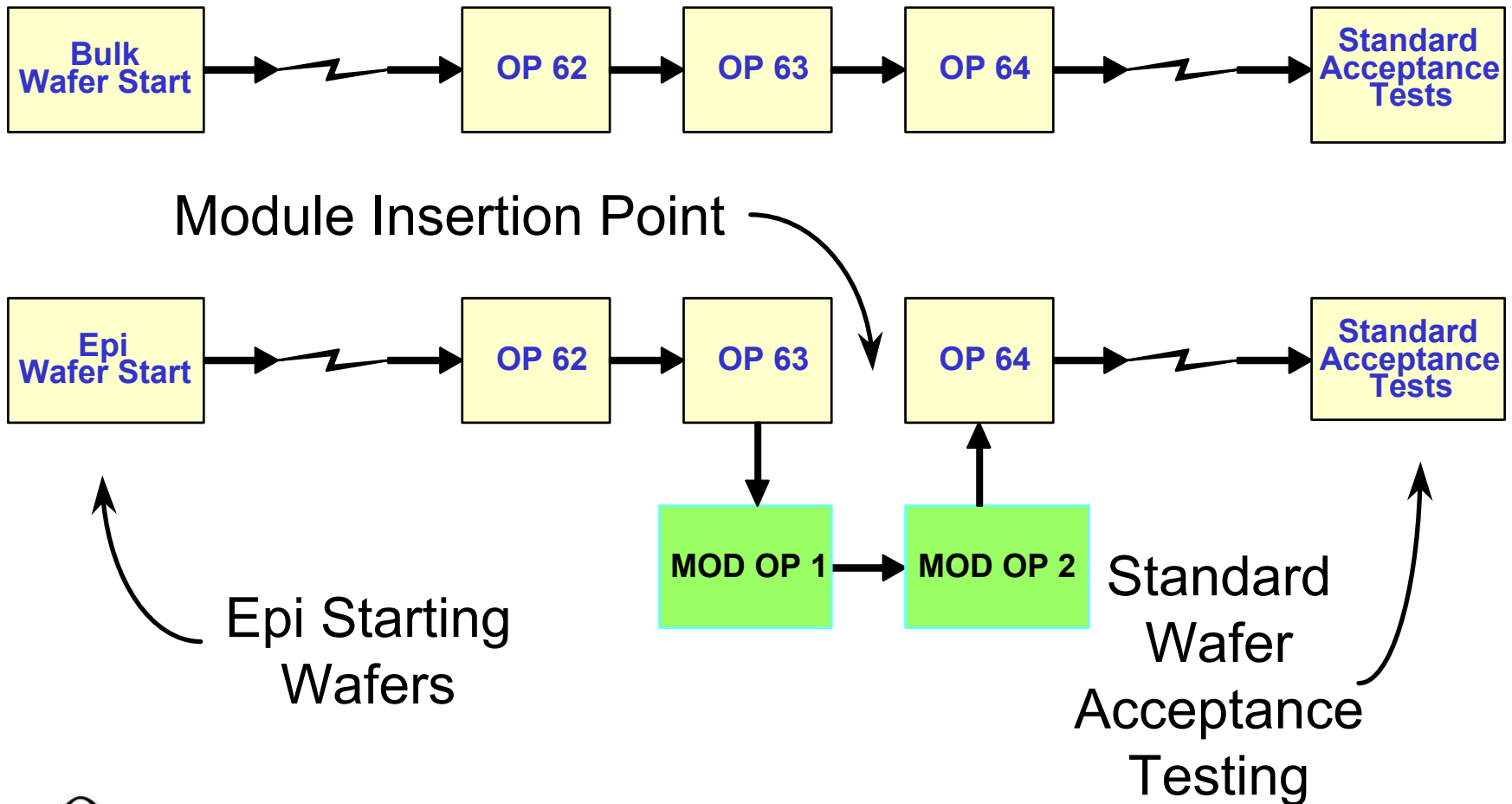
Pro: “Universal” acceptance, very effective

Lay-Out Techniques: **Con:** Requires custom layout & more area

Circuit Design: **Pro:** “Universal” acceptance, very effective SEU

Con: Not practical for TID

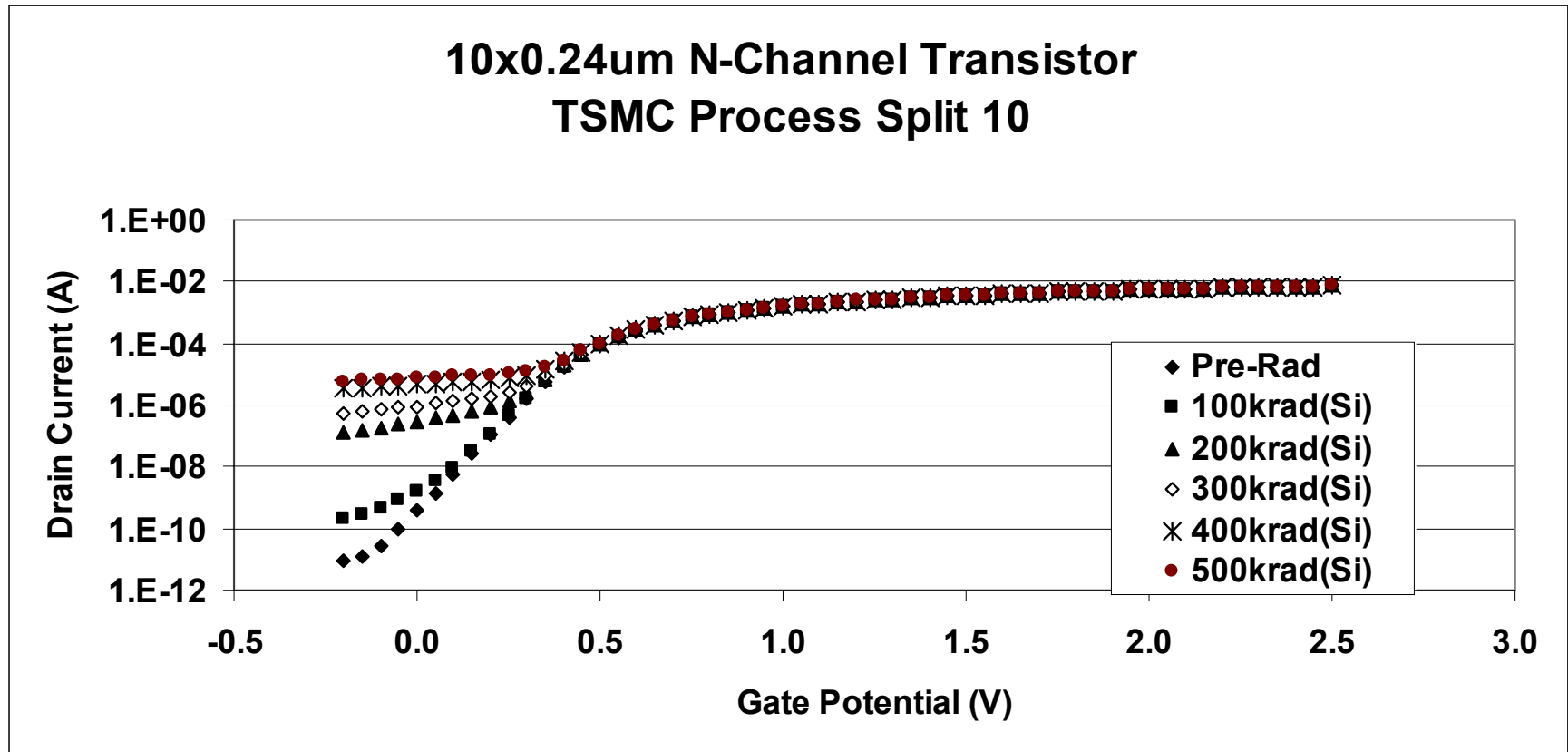
Commercial RadHard™ Module



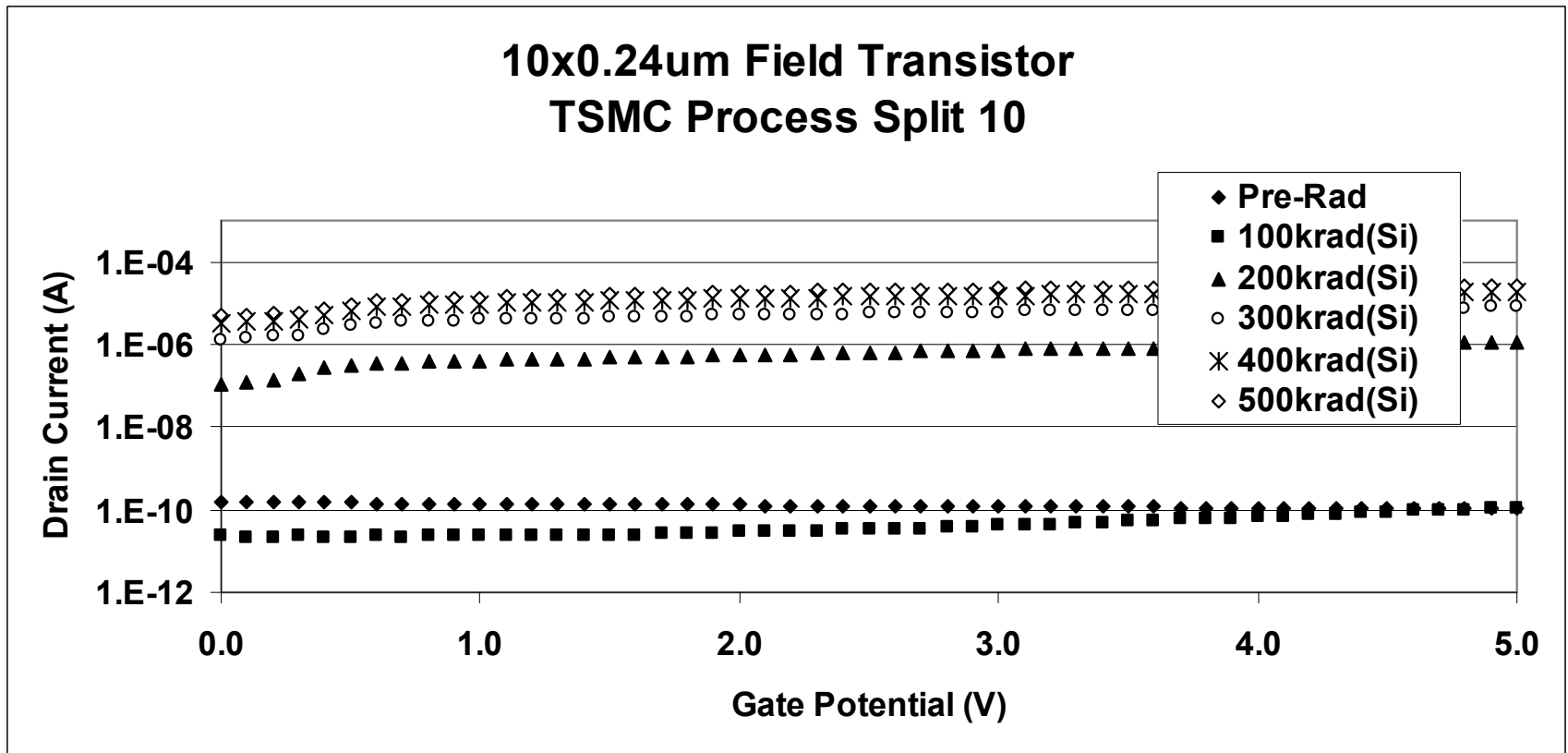
Radiation Hardening Treatments and Their Levels

Wafers	Treatment				Split
	Treatment A	Treatment B	Treatment C	Treatment D	
1, 18, 21		Level 1		Level 1	1
3, 7		Level 1		Level 2	2
10, 20, 23		Level 1		Level 3	3
5, 15	Level 1	Level 1			4
4, 17	Level 1	Level 2			5
6, 16, 22	Level 2	Level 1			6
11, 13	Level 2	Level 2			7
8, 14		Level 1	Level 1		8
12, 19		Level 1	Level 2		9
2, 9, 24					10

Baseline Process: N-Channel Transistor

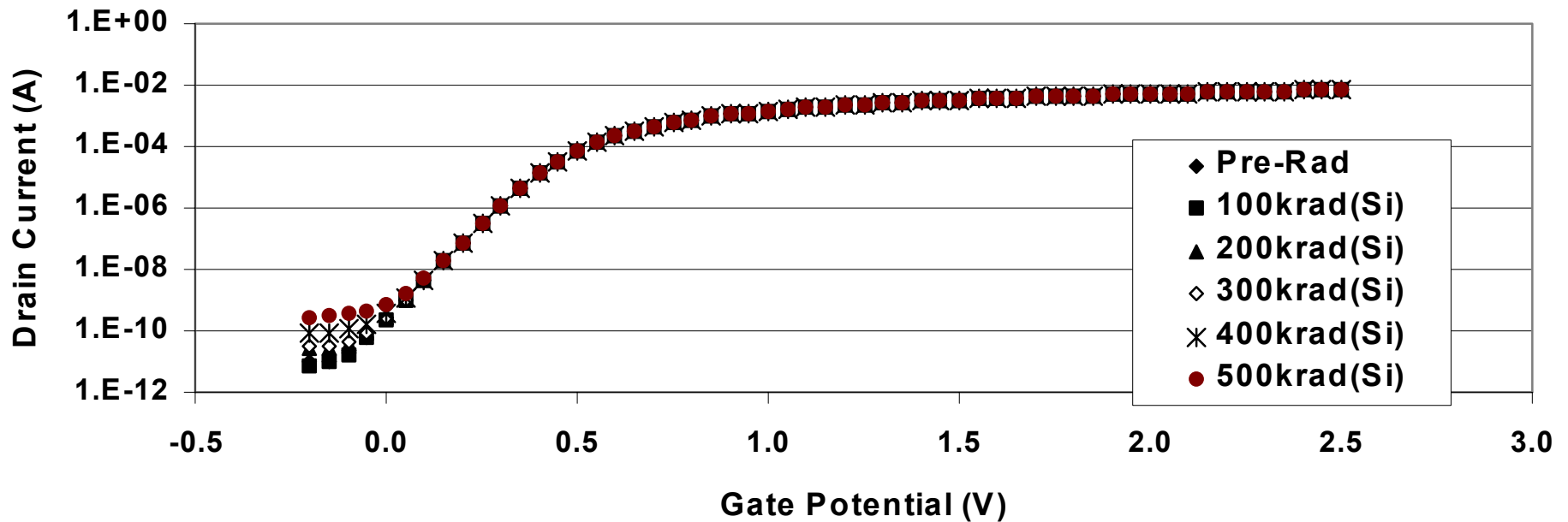


Baseline Process: Field Structure



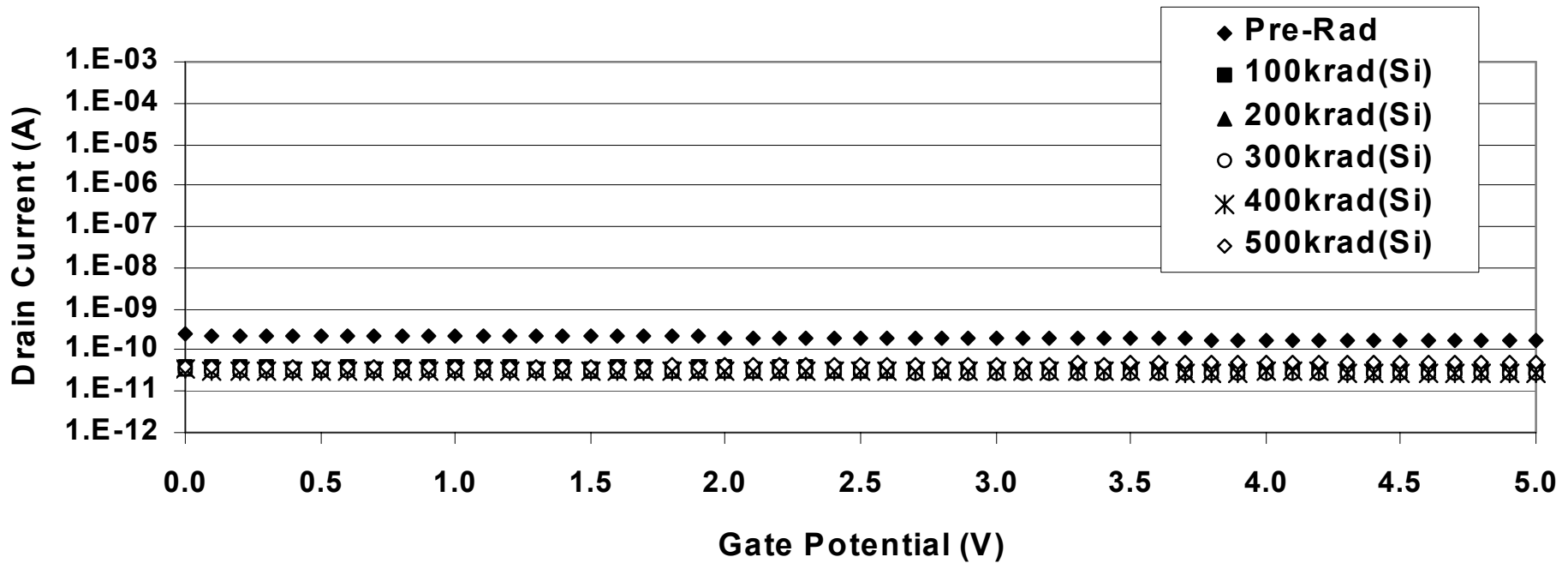
Split 3: N-Channel Transistor

10x0.24um N-Channel Transistor
TSMC Process Split 3a



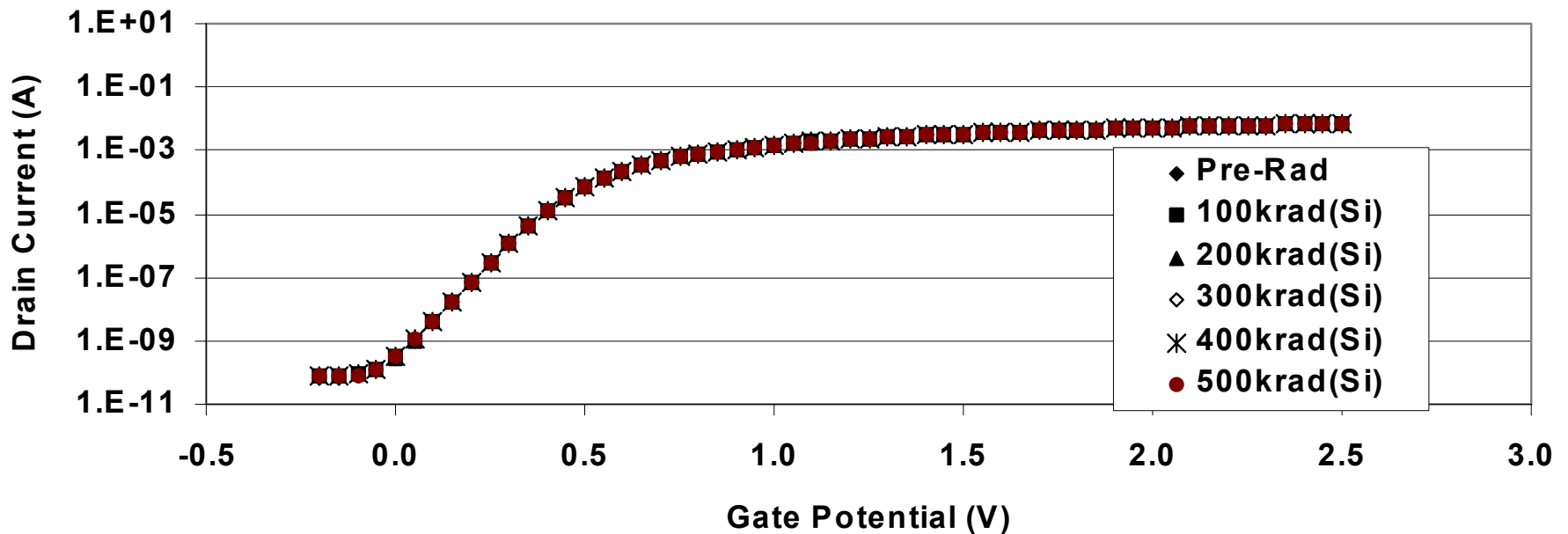
Split 3: Field Structure

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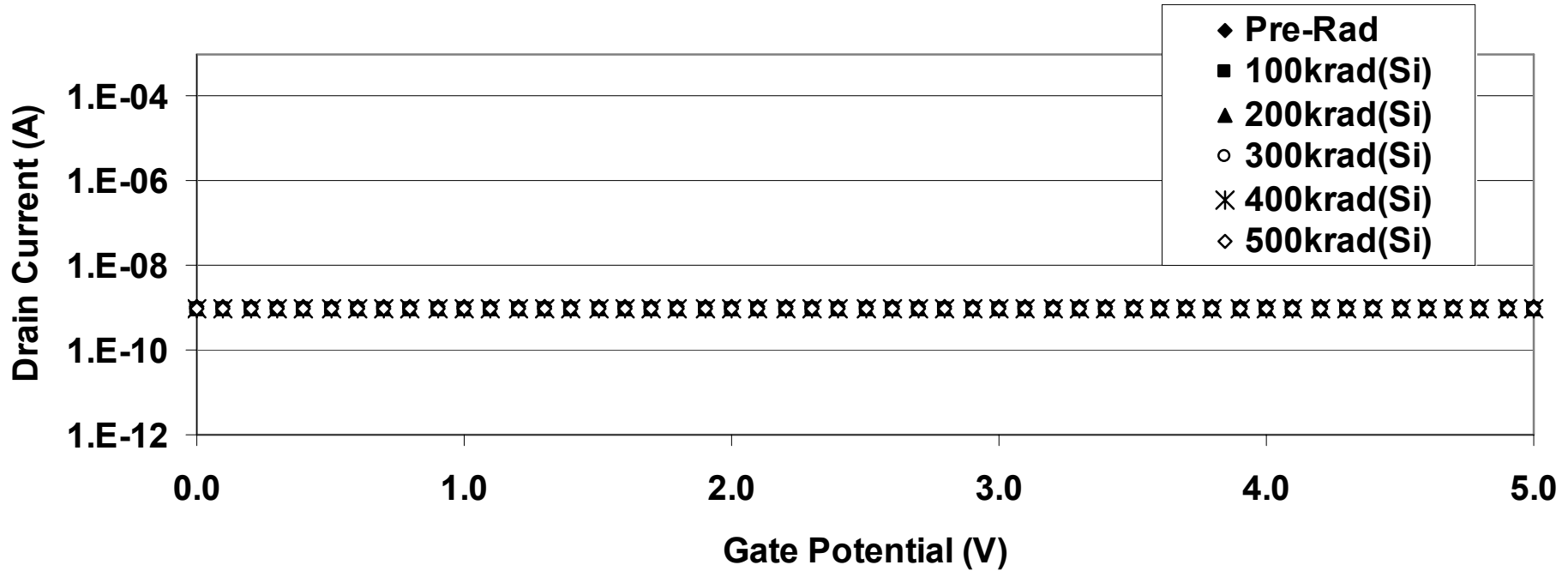
Split 9: N-Channel Transistor

10x0.24um N-Channel Transistor
TSMC Process Split 9a

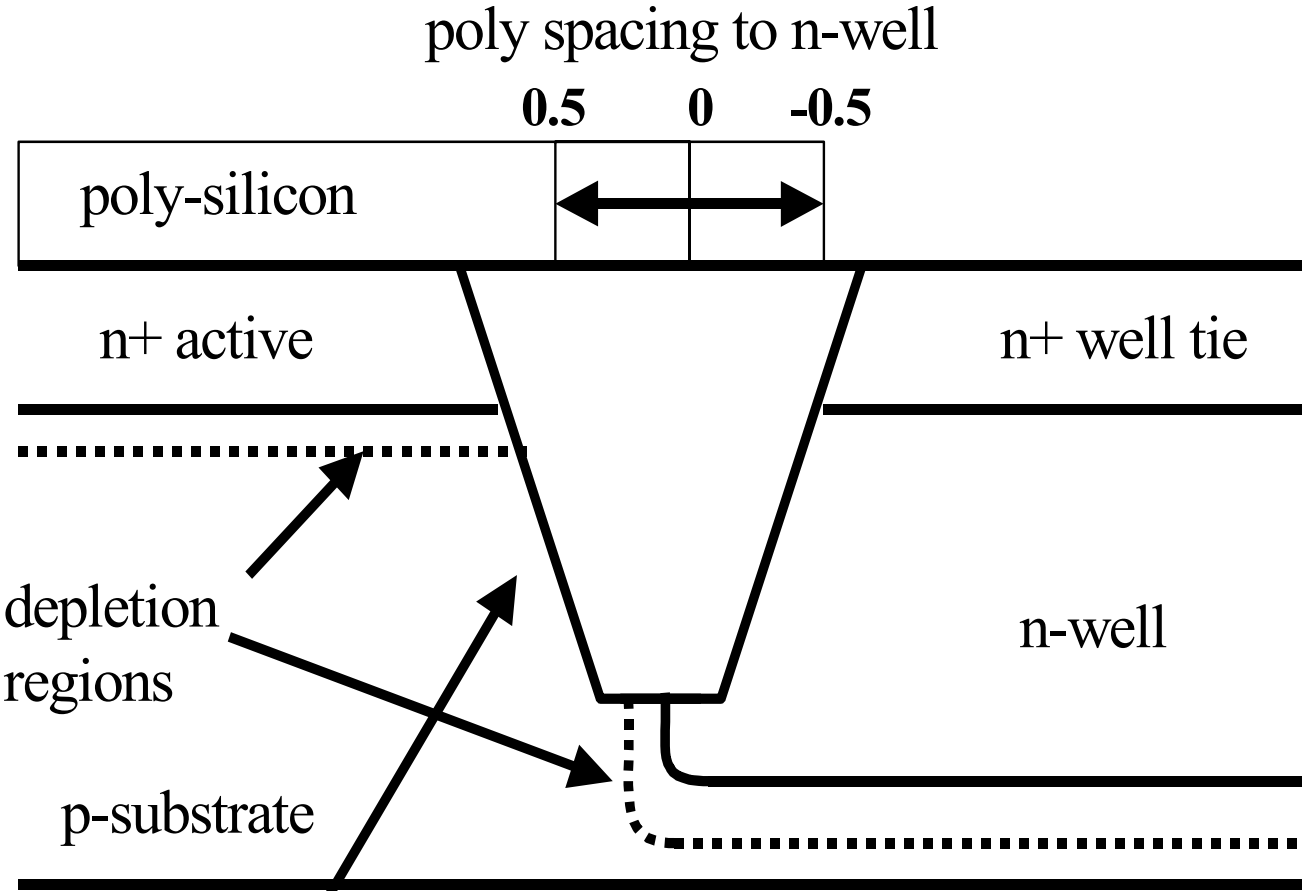


Split 9: Field Structure

10x0.24um Field Transistor
TSMC Process Split 9a

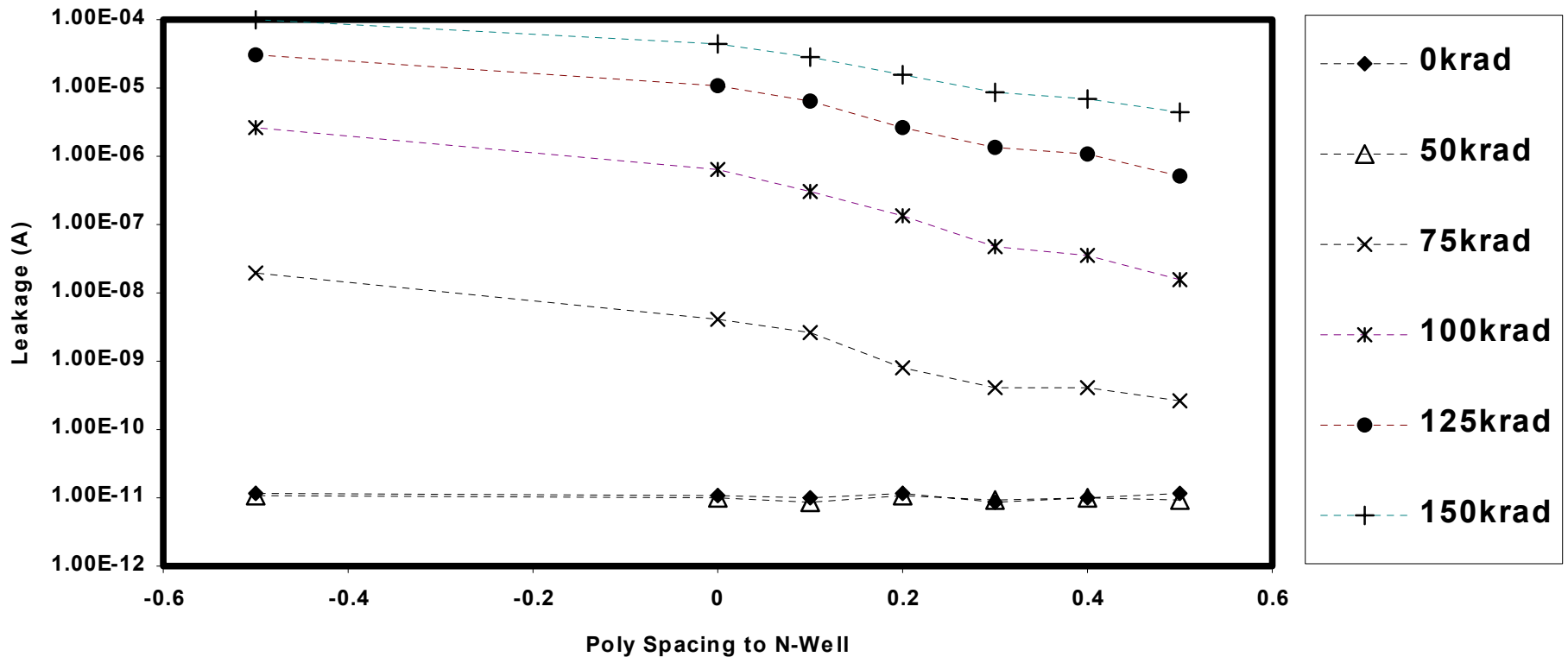


Design Rule Modification Example: Poly-Silicon to N-Well Spacing



Potential leakage path along side of shallow trench isolation

Inter-device leakage characteristics versus total dose, Poly spacing to n-well was varied from -0.5 to $+0.5\mu\text{m}$



Hardening by Design: Layout Modifications

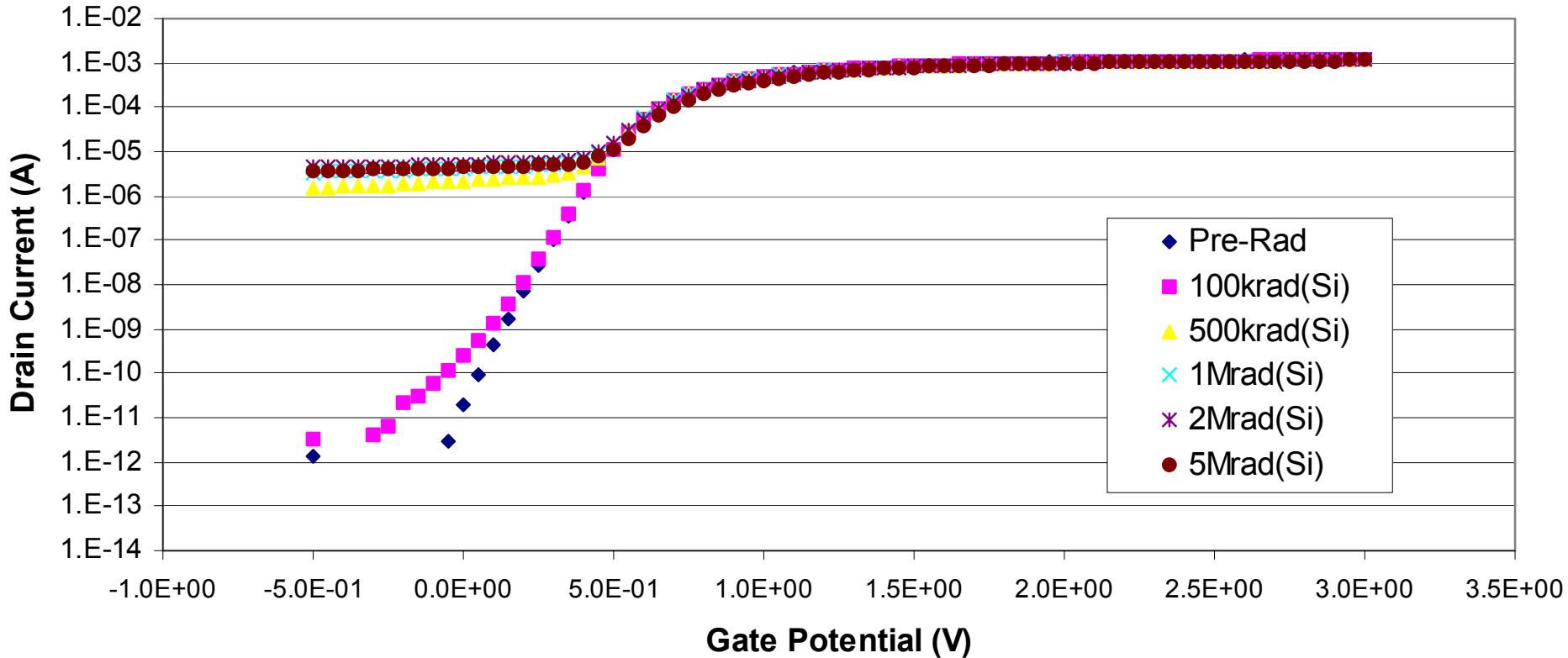
Aeroflex UTMC has developed and manufactured a novel transistor structure/process (internally called the B²JT) that is capable of radiation hardening n-channel transistors without requiring any changes to the commercial process.

The essence of the hardening approach is to utilize select existing mask levels to “engineer” a hardened structure. With this approach all standard mask levels are used, except that some are modified from their traditional role (to essentially serve a dual purpose)

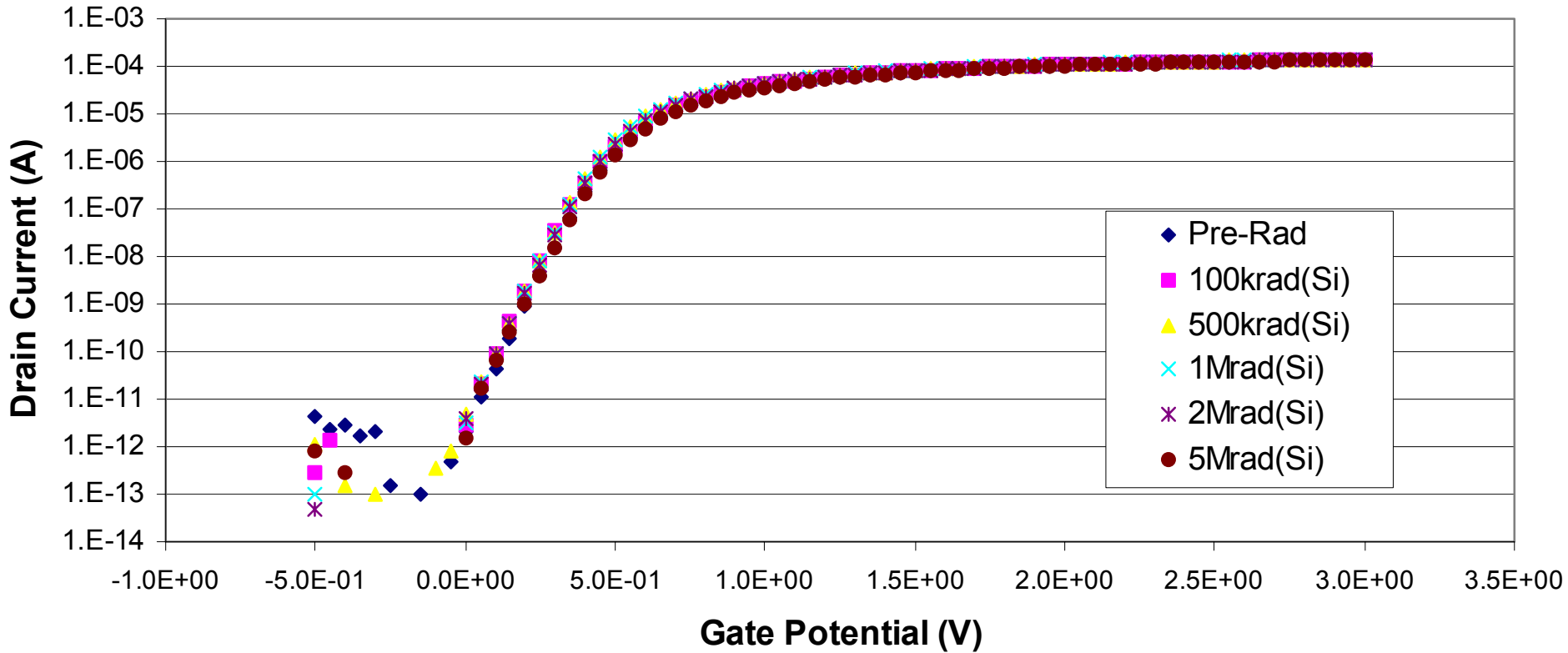
The n-channel transistor manufactured using this approach is only slightly larger than an unhardened conventional transistor. The structure/process is fully compatible with commercial foundry processes but may violate some design rules.

Standard Transistor (MOSIS Test Chip at TSMC)

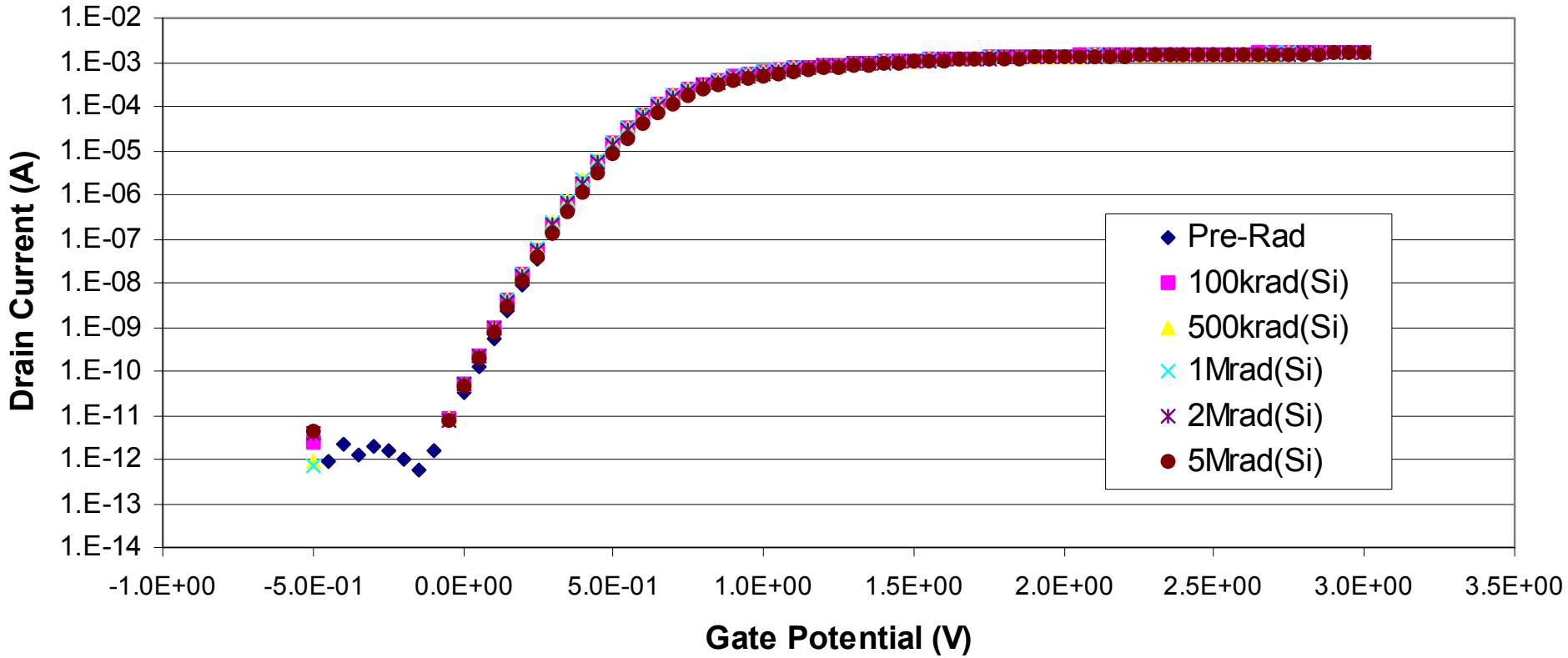
Aeroflex UTMC 0.24 x 20 N-Channel Transistor



Aeroflex UTMC B2JT 0.24 x 1 N-Channel Transistor



Aeroflex UTMC B2JT 0.24 x 20 N-Channel Transistor



Aeroflex UTMC RadHard NonVolatile RoadMap

- 1. Migrate 256Kbit one-time programmable PROM to TSMC 0.35um process using QuickLogic amorphous Si antifuse. Hardening via design rule and layout modifications.**
- 2. Develop 1M EEPROM on SOS with Peregrine Semiconductor and MRC. Hardening via intrinsic process tolerance and layout modifications**
- 3. Develop 4M (and larger) SONOS Flash memory using commercial fab. Hardening via process modification on standard cell.**