

Neo-Stacking of Packaged Flash Memory

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Abstract—A variation on Irvine Sensors’ Neo-Stacking process allows extremely dense packaging of Flash or other memory while sidestepping the problems associated with obtaining Known Good Die (KGD). Memory is often difficult or impossible to obtain in die or wafer form, and comprehensive testing and burn-in is prohibitively expensive for many applications. Readily available plastic encapsulated packaged memory chips are pre-tested and can easily be further tested and screened, speed sorted, tested over a different temperature range, etc. However, they cannot be packaged densely enough to meet the requirements for many applications. This paper describes a method for reprocessing and stacking standard packaged memory, along with support circuitry, into a chip-scale footprint with a very low profile.

available, an important design issue to be addressed is that of Known Good Die (KGD). Generally, KGD solutions are rather costly. The problems of bare die availability and KGD testing can be addressed simultaneously.

TSOPs are the most readily available part type, and they are already fully tested in that packaged format. The process being developed further processes the TSOPs into smaller, very thin, stackable layers.

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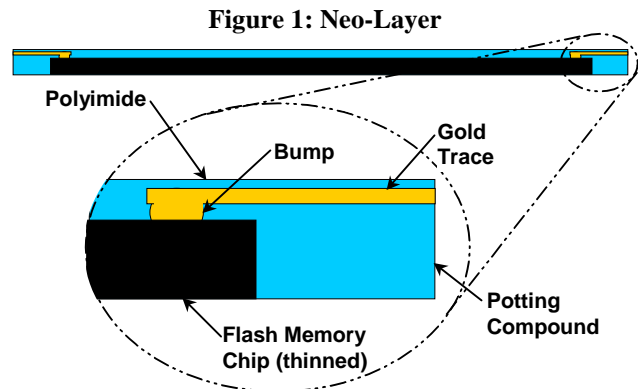
1. INTRODUCTION

Often, flash memory is most readily available in a plastic encapsulated thin small outline package (TSOP). Processes for stacking TSOPs are available from several sources, Irvine Sensors Corporation among them. The process is economical and allows two to eight chips to use the board space of only one. However, the overall volume is not reduced since the stacked TSOPs, plus interposers, form a relatively tall subassembly. For many applications, stacking TSOPs provides the needed density, although for extreme miniaturization, stacking bare silicon chips is required.

Irvine Sensors Corporation has established processes for bare die stacking that require that the chips be available in either die or wafer form. Obtaining chips in either form is sometimes difficult or impossible. When bare die are

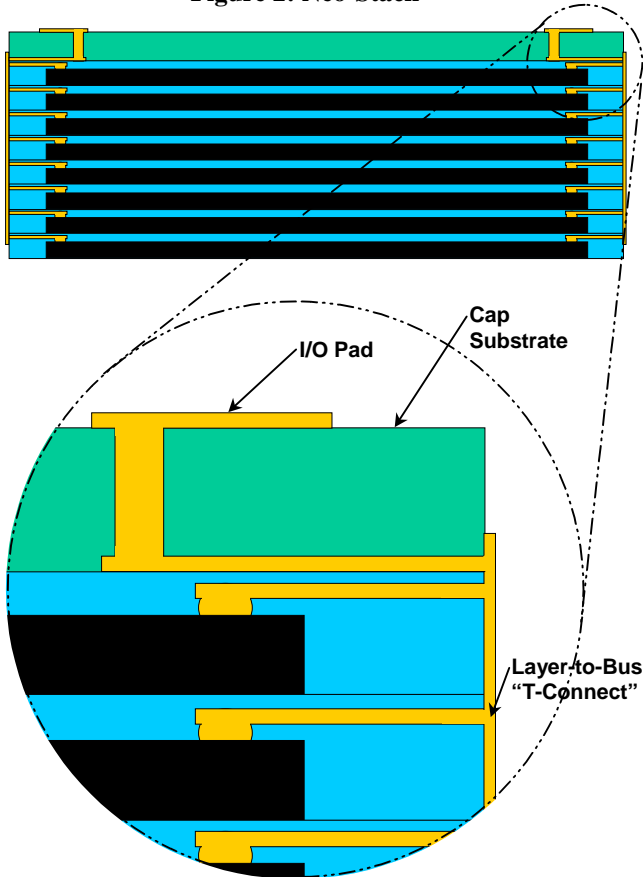
2. NEO-STACKING

Irvine Sensors’ Neo-Stack™ process starts with a bumped KGD that is encapsulated in a potting compound. Thin film metal traces contact the I/O bumps and route the signals to the edges of the potting material. The layer is ground from the backside resulting in a thin (.25 mm to .10 mm) complete layer, as shown in Figure 1.



A Neo-Stack is created by laminating Neo-Layers with a cap substrate, which uses through-holes to provide I/O paths. Bus metalization is applied on one or more sides to interconnect layers and the cap substrate. The intersection of the layer traces and the bus traces form the “T-Connects”, which are key to high reliability. Unlike wrap-around or “L-Connect” approaches where step coverage problems can result in a reduced metal cross section, the trace thickness of T-Connects remain the full thickness as deposited. A complete Neo-Stack is shown in Figure 2.

Figure 2: Neo-Stack



3. STACKABLE LAYERS FROM TSOPS

The typical internal construction of a TSOP package lends itself to processing into a stackable layer of almost identical structure to a Neo-layer constructed from a KGD. Within the TSOP, gold wire bonds are used to connect the die I/O pads to the lead frame, as shown in Figure 3.

Standard wafer grinding equipment is used to remove most of the encapsulant material on the top surface, down to the cross section of the gold ball of the interconnecting wire bond. This process leaves a thin layer of encapsulant on the die surface, which serves as the insulating surface for metal trace deposition. Grinding is also used to remove the encapsulant and carrier from the bottom of the die, and to thin the die itself. During this backside-grinding step, the leads are also removed. A final dicing step minimizes the layer footprint, while leaving enough of the original TSOP encapsulant around the die edges to provide an insulating surface for the bus metalization. The process sequence is shown in Figure 4.

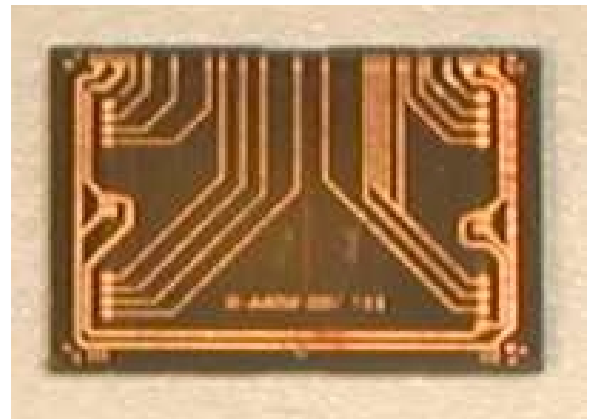
Typical TSOP encapsulant materials are chemically similar to the potting material used in fabricating Neo-Layers, which allows layers made from TSOPs to be stacked with the identical Neo-Stacking process.

4. COMBINING TECHNOLOGIES

The material compatibility allows layers made from TSOPs to be stacked along with standard Neo-Layers, which can contain different die types. The only constraint is that the die types in the Neo-Layers must not be so large that the Neo-Layer becomes larger than the memory layers. This is normally not a problem because memory die sizes are usually quite large as compared to other chip types in a typical subsystem.

Irvine Sensors is currently developing two products using modified TSOPs combined with standard Neo-Layers. The first is a stack for the mass memory storage portion of a miniature stacked computer. A single Neo-Layer is stacked together with eight layers of flash memory. The Neo-Layer contains two driver chips, which are procured in bare chip form, and the memory layers are made from standard TSOPs. Fully functional layers of modified TSOPs have been fabricated and tested down to a thickness of four mils (0.01 mm). Figure 5 shows a top view of a flash memory layer with the routing traces applied.

Figure 5: Flash Memory Layer



The second product is for use in a space application for NASA. Twelve memory layers are combined with a single Neo-Layer containing a radiation hardened Field Programmable Gate Array (FPGA). The FPGA provides I/O control and an Error Detection and Correction (EDAC) function. The compact assembly is sealed in a hermetic package. This strategy allows the use of Commercial Off-The-Shelf (COTS) components without the reliability compromise usually associated with the use of COTS parts. The original TSOP part has most of the plastic packaging removed, and the finished stacked hermetic component can be screened and qualified in accordance with full military and space requirements. Proof-of-concept stacks containing modified TSOPs have demonstrated the viability of the approach for this program.

5. SUMMARY

Neo-Stacking is a high-density packaging solution intended for use with bare die, and die contained in TSOP or other plastic packages can also be accommodated. The technique described in this paper overcomes the problems of bare die availability and KGD testing by treating the original plastic package as a low-cost temporary test carrier, from which the die is eventually removed. The resulting stackable layer is almost identical to standard Neo-Layers and can be stacked along with Neo-Layers containing other die types.

Figure 3: TSOP Construction

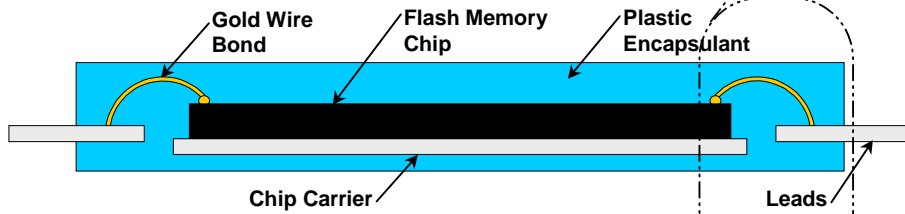


Figure 4: Layer Process Sequence

