

# **NEO-STACKING OF PACKAGED FLASH MEMORY**

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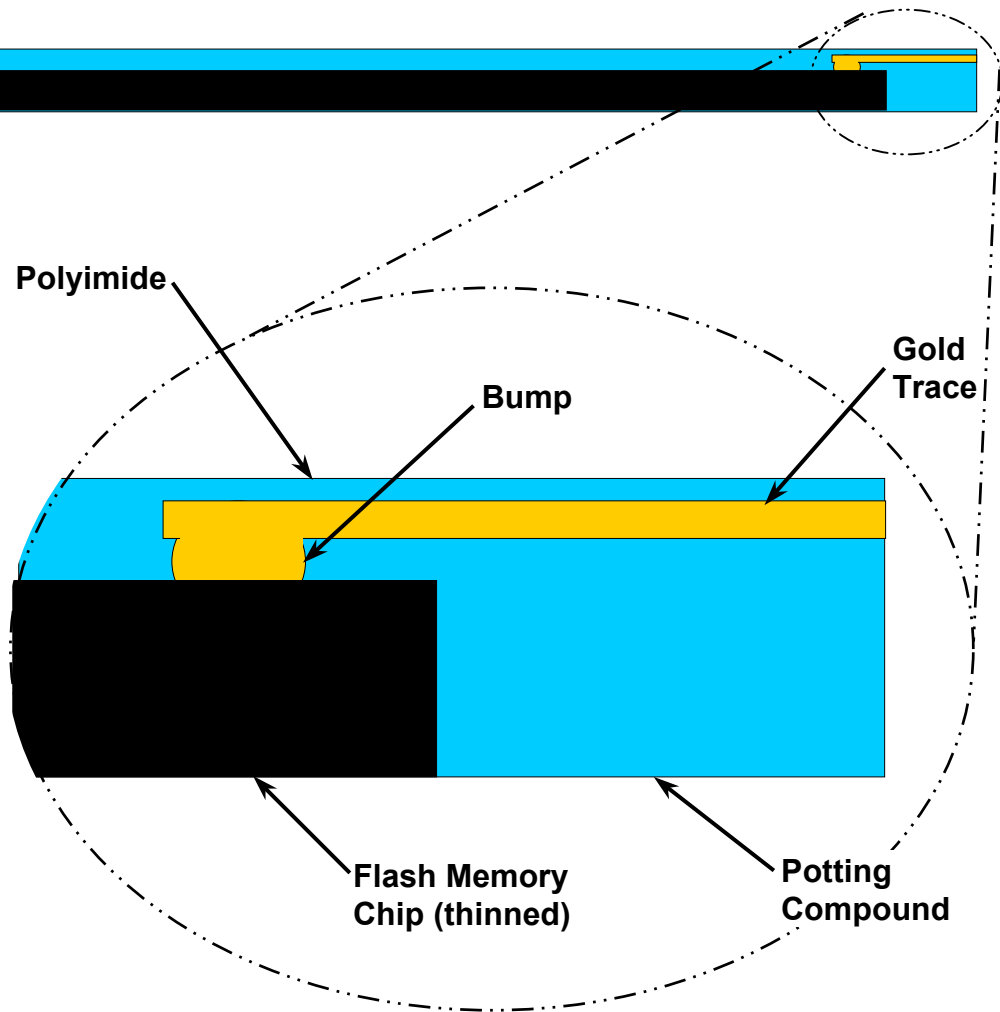
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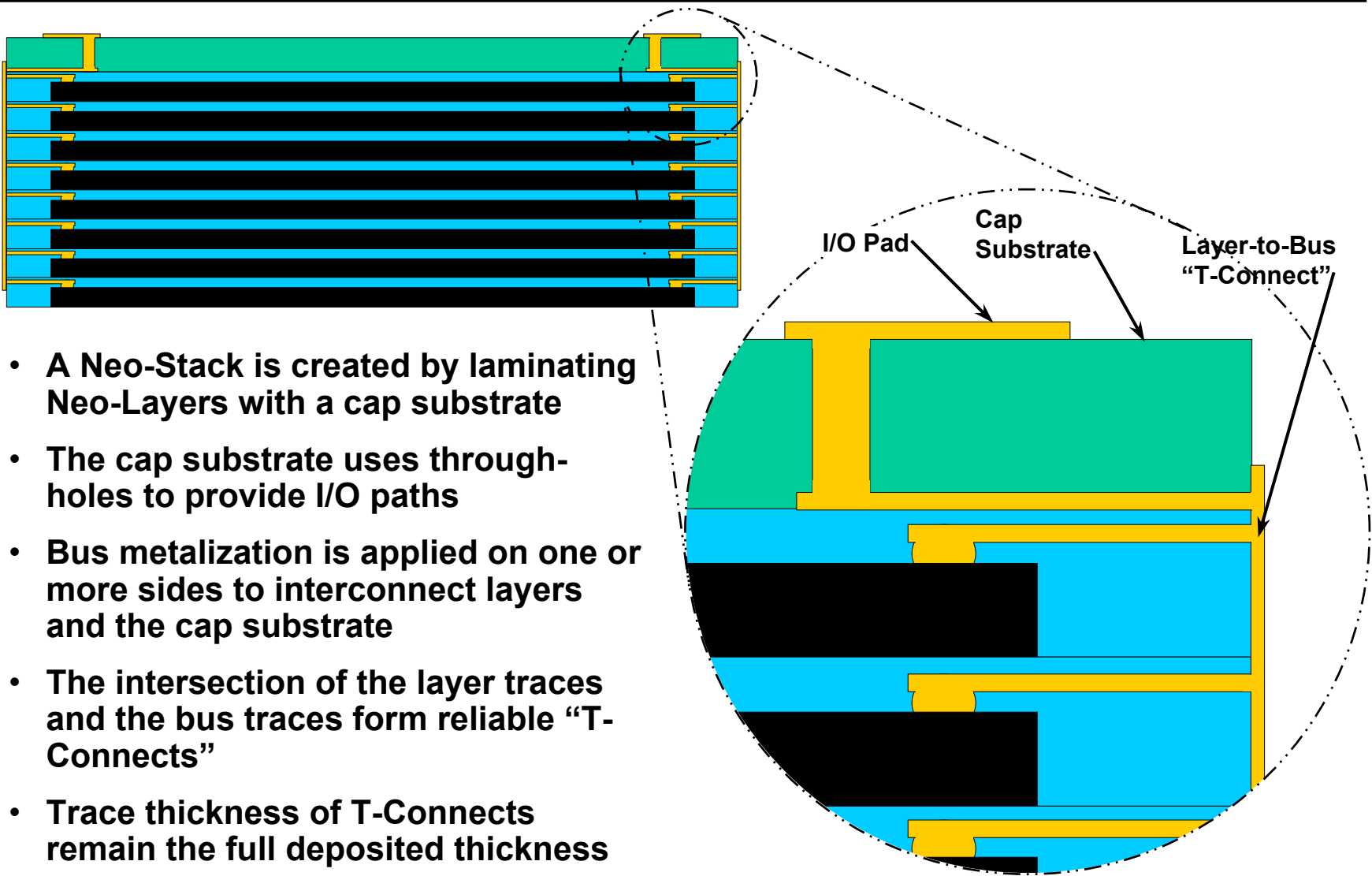
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- **A variation on Neo-Stacking allows extremely dense packaging while sidestepping the problems associated with obtaining Known Good Die (KGD)**
- **Extremely dense packaging normally requires unpackaged memory chips**
  - **Flash Memory is often not offered for sale in die or wafer form**
  - **Bare die testing is too limited to ensure acceptable stack yields**
  - **Comprehensive testing and burn-in is expensive**
  - **These problems are referred collectively as the KGD “problem”**
- **Flash memory is available in a plastic encapsulated thin small outline packages (TSOP)**
  - **Pre-tested and easily further tested and screened, speed sorted, tested over a different temperature range, etc.**
  - **Processes for stacking TSOPs reduce board footprint, but not overall volume**
- **A new process for reprocessing and stacking standard packaged memory, along with support circuitry, can be used to stack many chips into a single a chip-scale footprint with a very low profile**

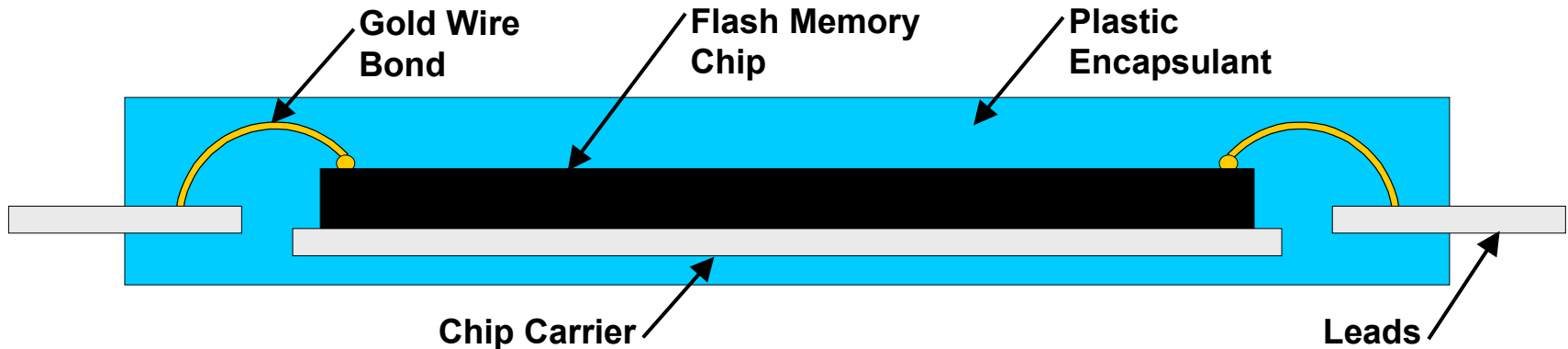
- **Process starts with a bumped die**
- **Die is encapsulated in a potting compound**
- **Thin film metal traces contact the I/O bumps and route the signals to the edges**
- **The layer is ground from the backside (.25 mm to .10 mm)**



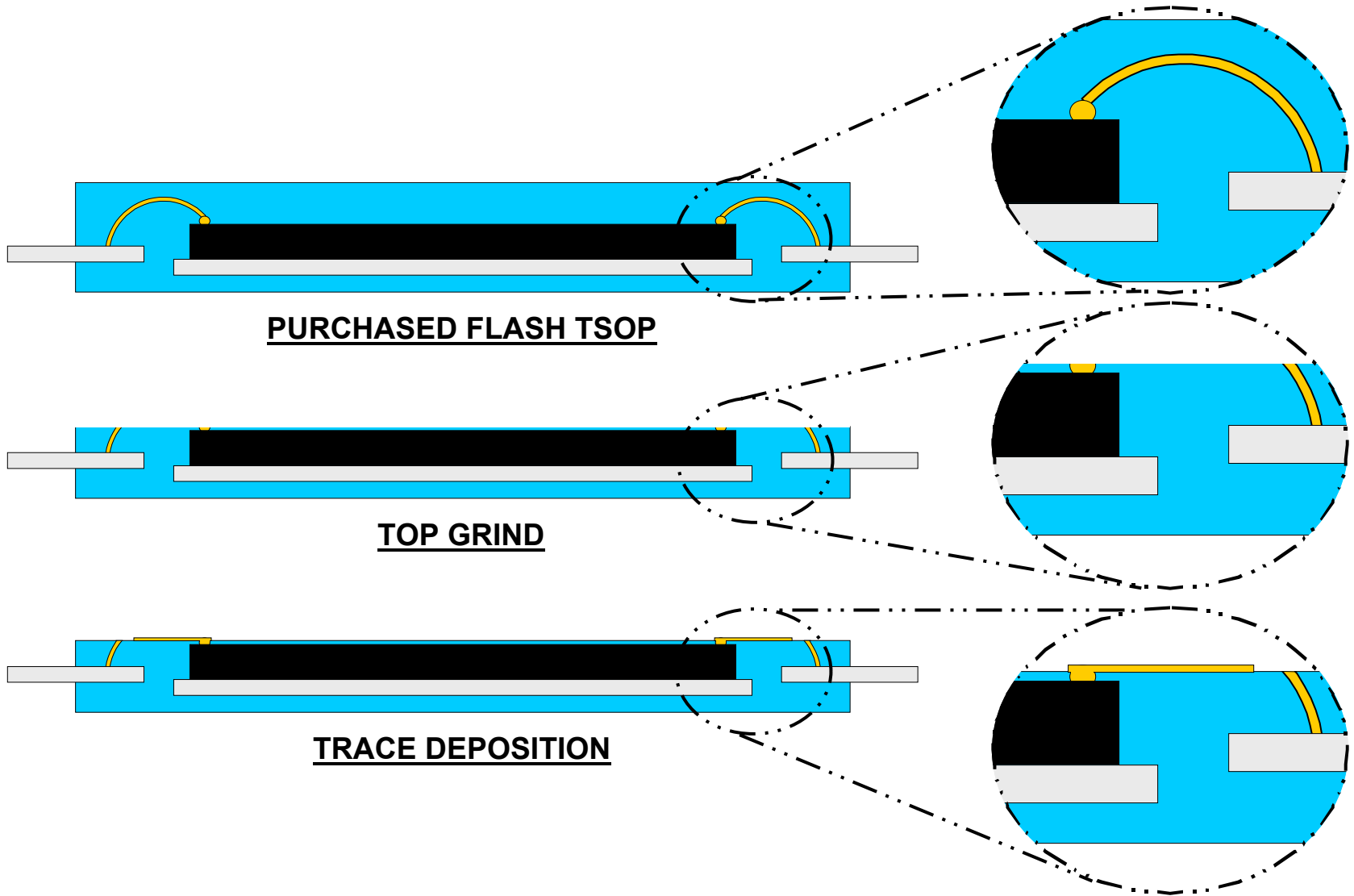


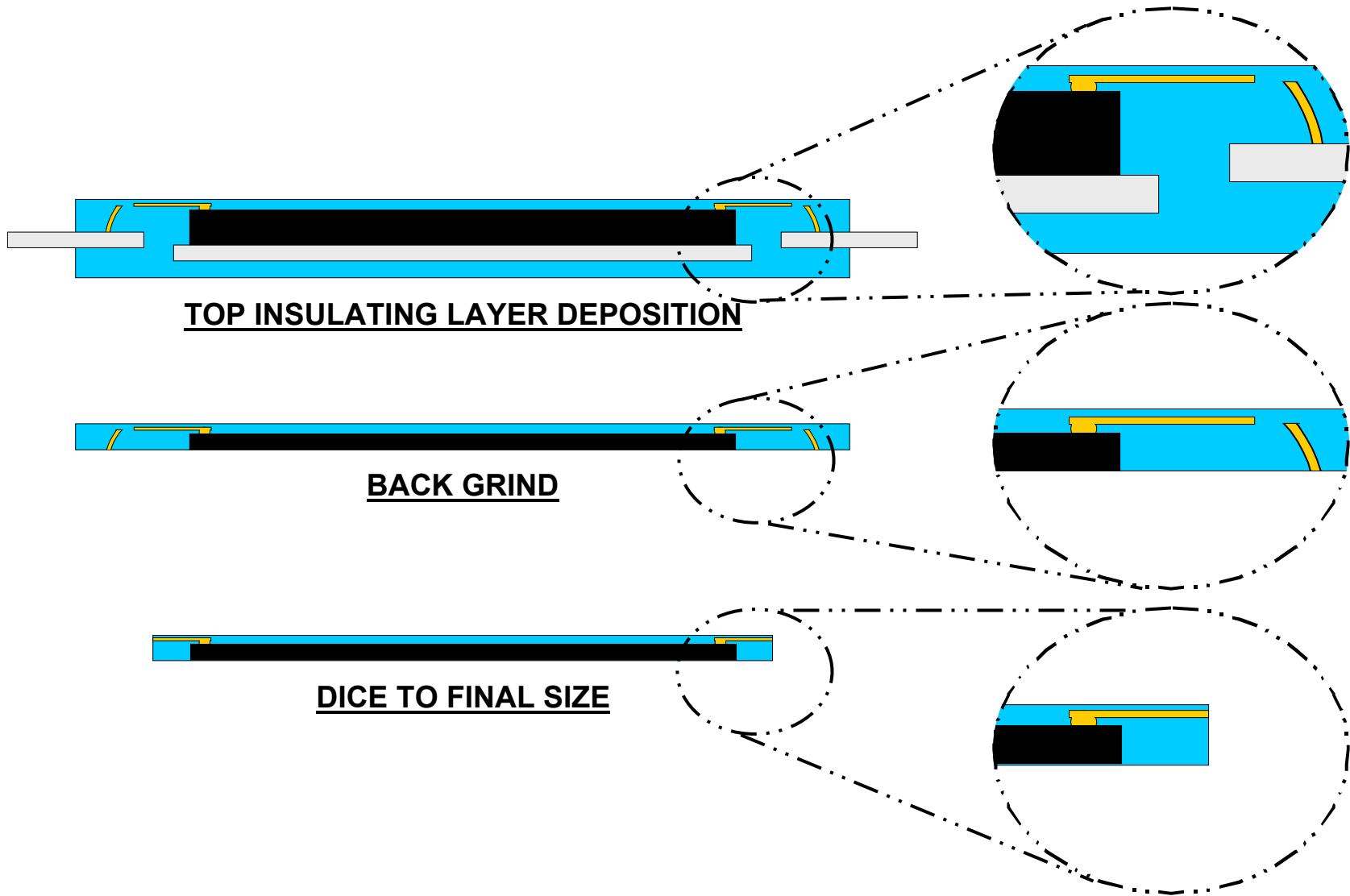
- A Neo-Stack is created by laminating Neo-Layers with a cap substrate
- The cap substrate uses through-holes to provide I/O paths
- Bus metalization is applied on one or more sides to interconnect layers and the cap substrate
- The intersection of the layer traces and the bus traces form reliable “T-Connects”
- Trace thickness of T-Connects remain the full deposited thickness

### Typical TSOP Cross Section

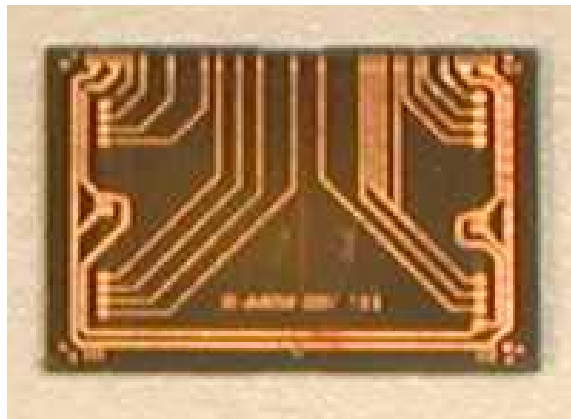


- Typical TSOP package construction allows processing into a thin stackable layer
- Wafer grinding equipment removes most of the encapsulant from the top surface cuts into the backside of the silicon, resulting in a thin layer
- Thin layers of encapsulant are left on the top surface and edges, providing an insulating surface for reroute and bus deposition
- Finished layer has almost identical structure to a standard Neo-Layer
- Typical TSOP encapsulant materials are chemically similar to the potting material used in fabricating Neo-Layers
- Layers made from TSOPs to be stacked with the identical Neo-Stacking process





- **Mass memory storage portion of a miniature stacked computer**
- **A single standard Neo-Layer contains two driver chips, which are procured in bare chip form**
- **Eight flash memory layers are made from standard TSOPs**
- **Fully functional layers of modified TSOPs have been fabricated and tested down to a thickness of four mils (0.1 mm)**
- **The picture below shows a top view of a flash memory layer with the routing traces applied**



- **Twelve memory layers are combined with a single Neo-Layer containing a radiation-hardened Field Programmable Gate Array (FPGA)**
- **The FPGA provides I/O control and an Error Detection and Correction (EDAC) function**
- **The compact assembly is sealed in a hermetic package**
- **Allows the use of Commercial Off-The-Shelf (COTS) components without reliability compromise**
- **Finished stack is hermetically packaged and screened/qualified in accordance with full military and space requirements**
- **Proof-of-concept stacks containing modified TSOPs have demonstrated the viability of the approach for this program**

- **Neo-Stacking is a high-density packaging solution intended for use with bare die**
- **Die contained in TSOP or other plastic packages can also be accommodated**
- **The technique described in this paper overcomes the problems of bare die availability and KGD testing**
- **The original plastic package is treated as a low-cost temporary test carrier, from which the die is eventually removed**
- **The resulting stackable layer is almost identical to standard Neo-Layers and can be stacked along with Neo-Layers containing other die types**