

Copper/low-k interconnect integration into 0.15 μm single poly EEPROM technology.

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Abstract

Successful and reliable integration of Copper and low-k interconnect into single poly non-volatile EEPROM technology is demonstrated for the first time. EEPROM cell reliability and performance of Copper interconnect EEPROM cell is compared with Aluminium interconnect EEPROM cell. Additionally, viability of replacing silicon nitride with oxynitride as a diffusion barrier layer underneath metall to prevent contamination related to charge loss from getting into EEPROM cell is discussed.

Introduction

Below 150 nm technology use of Cu as interconnect becomes a necessity [1]. Unlike Al, Cu is known to diffuse through oxide. Using a barrier layer such as TaN, Cu diffusion through oxide is prevented. On account of charge loss concerns in programmable logic circuits, the prevention of Cu diffusion is even more critical to EEPROM circuits than to the logic circuits. Successful integration of Cu interconnect technology with non-volatile EEPROM cell (Figure 1: 3 transistors, 1 capacitor and 1 tunneling diode single poly Si EEPROM cell) will allow programmable logic devices with EEPROM memory cell to shrink to and beyond 150 nm gate length.

To prevent interconnect related contamination from entering the EEPROM cell floating gate, furnace grown silicon nitride has been used as a diffusion barrier underneath metall. However, it has a higher dielectric constant associated with it ($\epsilon = 7.8$) which results in higher interconnect capacitance. For shrinking technologies, interconnect capacitance should be as small as possible. By choosing a suitable

composition, plasma enhanced CVD (PECVD) grown oxynitride layer (ϵ between 3.8 and 7.8) could be used as a diffusion barrier layer [2, 3] which due to the lower k would provide lower interconnect capacitance. The lower deposition temperature of oxynitride would reduce the thermal budget as well.

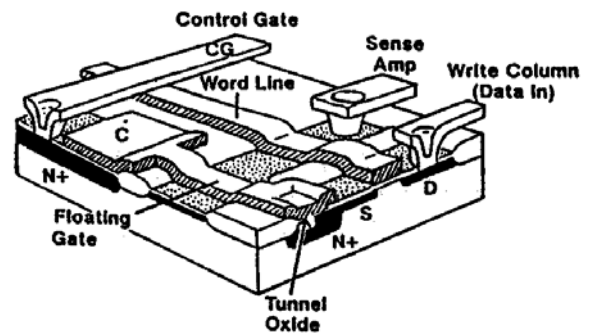


Figure 1: Single-poly Si EEPROM cell view.

Manufacturing Process

Front End Process: The front-end process for both Cu and Al interconnect EEPROM devices includes a p-substrate, STI, twin-well process with single poly-silicon and cobalt silicide. High voltage required for program and erase of the EEPROM cell is supported by N+/p-sub junction in conjunction with a deep phosphorous implant to get a more gradual junction profile. High field threshold voltage (V_t) is set by the field implant through the silicon trench isolation (STI).

Back End Process: EEPROM cell with Cu back-end comprised W CMP contact plugs along with Cu metall and low-k dielectric material IMD. Cu was deposited on dry-

etched oxide trenches (single damascene) using a combination of sputtering (TaN liner/Cu seed) and electro-chemical plating (ECP). The Cu film was subsequently planarized with CMP followed by nitride passivation. The Al test chip comprised W CMP contacts and via plugs with a TiN/AlCu/TiN liner stack and SiO₂ ILD. Splits for silicon nitride (furnace grown) and oxynitride blanket layer (PECVD-grown using SiH₄ + N₂O constituent gases) underneath metal1 was used with Al back-end wafers to compare the effect of these layers as a diffusion barrier layer for unwanted species. A brief process flow is shown in Table 1.

TABLE 1. Process Flow

Logic (Core)	EEPROM Module
OD/STI	(additional steps to the Logic steps) N+ imp under Tunnel Window
Twin-well	
Field Implant	
	Tunnel Oxide
Gate Poly	
	Deep P Implant at HV S/D
LDD Imp for all devices	
Spacer Formation	
NMOS S/D	
PMOS S/D	
	Diffusion Barrier Layer
Contact and Metallization	

Experimental Results and Discussions:

Characterization of EEPROM cells with Al and Cu interconnects as well as silicon nitride and oxynitride diffusion barrier layers were performed for reliability and performance. The erase and program cycling for the EEPROM cell is done through a Fowler-Nordheim (F-N) tunneling mechanism. Erase and program verification is done through the read path.

Reliability and performance comparison of EEPROM cells with Al and Cu interconnects

Performance comparison of EEPROM cells with both types of interconnects was done by taking erase Vt versus erase time and Icell versus program time measurements in figure 2 and figure 3 respectively. Icell is the current

through the sense amp when EEPROM cell is programmed (electrons are tunneled back into the substrate) and word line is high (figure 1). According to the graph in figure 2, after 1000 ms of erase time, the difference in Vt between the Al and Cu interconnects EEPROM cells is less than 1%. According to the graph in figure 3, after 100 ms of program time, difference in Icell between the Al and Cu interconnect EEPROM cells is less than 1%. The graphs in figure 2 and 3 reflect, as expected, that performance of EEPROM cells with Al and Cu interconnects is almost the same.

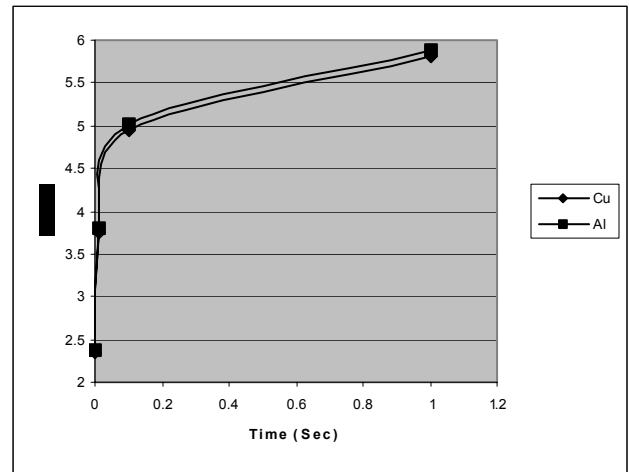


Figure 2: Erased Vt versus erase time graph for single bit EEPROM cells with Cu and Al interconnects.

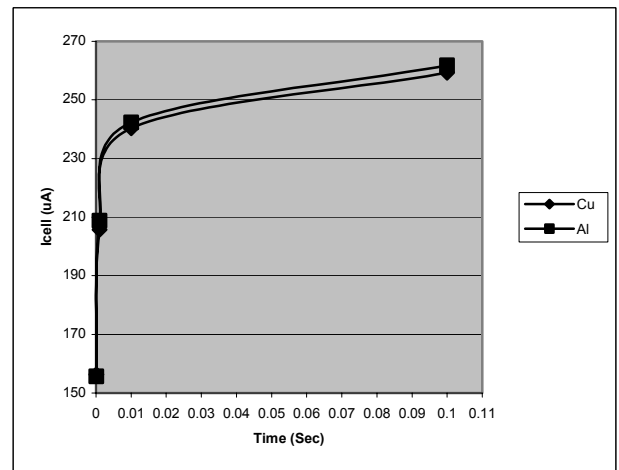


Figure 3: Icell versus program time graph for single bit EEPROM cells with Cu and Al interconnects.

Data Retention: Wafer level bake was done on both wafers with Al and Cu backend. The following procedure was adopted for the data retention test: (1) program/erase cycling (2) erase margin V_t (3) bake at 125 °C (4) erase margin V_t . Step 3 followed by step 4 was repeated for different bake times.

Erase margin after 500 hours bake time at 125 °C shifted less than 1.5% for the EEPROM cell with Cu interconnect. This is comparable to the erase margin shift under the same bake conditions for the identical EEPROM cell with Al interconnect. The graph in figure 4 plots erase V_t versus bake time for both Al and Cu interconnect EEPROM cells. This demonstrates that Cu interconnect technology can be integrated reliably with the non-volatile EEPROM cell.

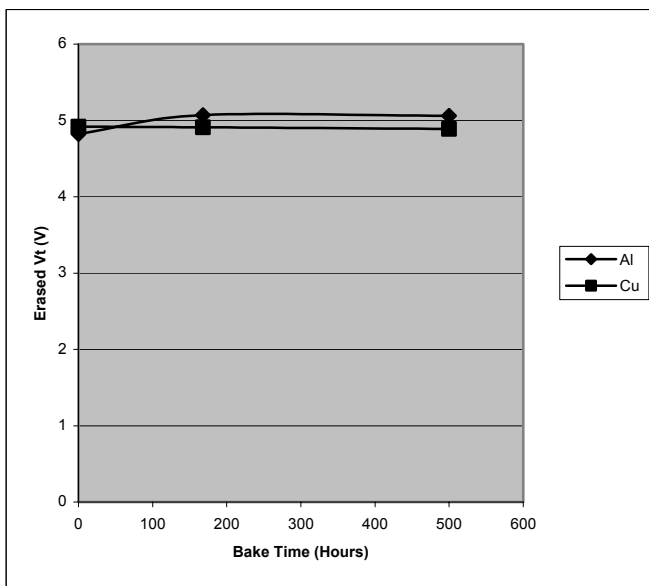


Figure 4: Graph showing erase margin versus bake time for single poly EEPROM cell with Al and Cu interconnect.

Reliability comparison of EEPROM cells with silicon nitride and oxynitride barrier layers.

Furnace grown silicon nitride was used as a diffusion barrier layer to prevent contamination from reaching the floating gate of the non-volatile cell. Oxynitrides as barrier layers have

received an increasing amount of interest due to the possibility that, by choosing the proper composition, the excellent electrical characteristics of SiO_2 and the barrier properties against moisture and other sources of contamination of silicon nitride may be preserved [2]. Additionally, oxynitrides deposited by PECVD at low temperature would be a better choice than furnace-deposited silicon nitride at higher temperature for shrinking technologies due to smaller thermal budget of the former [4-6].

Data Retention: Wafer level bake at 125 °C was done on both wafers with identical EEPROM cells but different diffusion barrier layers of nitride and oxynitride. The same procedure described earlier in this paper was used for the data retention test. The graph in figure 5 shows erase margin versus erase bake time after 500 hours of bake at 125 C for both EEPROM cells. Erase margin shift for EEPROM cell with oxynitride as diffusion barrier blanket layer was more than 12% while that for EEPROM cell with silicon nitride as a diffusion barrier blanket layer was less than 1.5%. However, there was no erase V_t margin shift from 168 hours to 500 hours. On account of shift in the V_t margin from zero hour to 168 hours, it is concluded that plasma enhanced oxynitride is an unsuitable choice for diffusion barrier layer.

The possible cause of erase V_t margin shift from zero hour erase margin to 168 hours might not be due to real charge flow from the floating gate but could be as a result of charges in the oxynitride layer that couple voltage to the floating gate thereby shifting the margin. Charges in the oxynitride layer deposited by PECVD could arise from the creation of dangling bonds (DB) which are enhanced as more O atoms are incorporated in the oxynitride film. However, the formation mechanism of defects in oxynitride films with different compositions is unclear [7]. Also, conventional plasma-assisted CVD with SiH_4

as silicon source introduces hydrogen in the deposited films that causes thermal instability of physical and electrical properties during subsequent processing [2, 8]. D. R. Cote and co-authors [9] have suggested that PECVD oxynitride film with higher refractive index ~ 1.80 to 1.85 might be more desirable for barrier application. The bonding structural analyses and electrical measurements on PECVD oxynitride films done by these authors have shown that films with refractive indices of 1.75 to 1.80 have low surface states with minimal leakage.

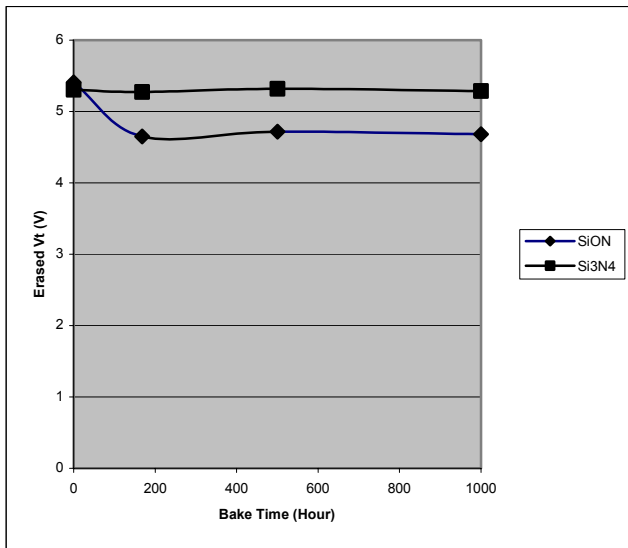


Figure 5: Graph showing erase margin versus bake time comparison for EEPROM cell with silicon nitride and oxynitride as diffusion barrier layers underneath Al metall.

Conclusions

The experimental results show that Cu/low-k interconnect can be used as an interconnect of choice with non-volatile EEPROM devices without causing significant reliability and performance concerns. Experimental results also indicate that PECVD oxynitride may not be a good substitute for furnace grown silicon nitride presently used as a diffusion barrier layer underneath metall in the EEPROM cell

due to increased charge loss possibly caused by the creation of dangling bonds and charge states in PECVD oxynitride.

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