An FPGA-Based Test-bed for Reliability and Endurance Characterization of Non-Volatile Memory

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Memory Technology Background:

Memory technologies are divided into two categories. The first category nonvolatile memories, are traditionally used in read-only or read-mostly applications because of limited write endurance and slow write speed. These memories are derivatives of ROM technology, which includes EPROM, EEPROM, Flash, and more recent Ferroelectric non-volatile memory technology. Nonvolatile memories are able to retain data in the absence of power. The second category, volatile memories, are RAM-devices including SRAM and DRAM. Writing to these memories is fast and write endurance is unlimited, so they are most often used to store data that change frequently, but they cannot store data in the absence of power. Non-volatile memory technologies with better future potential are FRAM, Chalcogenide, GMRAM, Tunneling MRAM and SONOS EEPROM.

FRAM is a uses a ferroelectric capacitor to store the data. This storage mechanism is quite different from that of other non-volatile memories, that use floating gate technology where the charge is stored. The ferroelectric effect is the ability of a material to store a state of electric polarization in the absence of an applied electric field. An FRAM memory cell is created by depositing a film of ferroelectric material in crystal form between two electrode plates to form a capacitor very similar to a DRAM capacitor. FRAM cell could be one transistor one capacitor (1T1C) or a more robust design using two transistors two capacitors (2T2C) for better fault tolerance (complementary storing). However, rather than storing data as a charge on the capacitor, a ferroelectric memory stores data within a crystalline structure known as Perovskite. The Perovskite crystals maintain two stable polarization states resulting from the alignment of internal dipoles, which are used to represent '1' and '0' states. Since no external electric field is required for the ferroelectric material to remain its polarization, a ferroelectric memory device can retain data in the absence of power.

EEPROM (electrically erasable programmable read-only memory) use memory cells with transistors that are very similar to normal MOS

transistors, but the transistors have a second, floating gate. Applying a programming voltage VPP (usually greater than 12 V) to the drain of the n-channel EEPROM transistor programs the EEPROM cell. A high electric field causes electrons flowing toward the drain to move so fast they "jump" across the insulating gate oxide where they are trapped on the bottom, floating, gate. The energetic electrons are referred to as hot and the effect is known as hot-electron injection or avalanche injection. EEPROM technology is sometimes called "floating-gate avalanche MOS" (FAMOS). Electrons trapped on the floating gate raise the threshold voltage of the n-channel EEPROM. Once programmed, an n-channel EEPROM device remains off even with a logic high applied to the top gate. An un-programmed n-channel device will turn on as normal with a logic high top-gate voltage. The programming voltage is applied either from a special programming box or by using on-chip charge pumps. In programming an EEPROM, an electric field is used to remove electrons from the floating gate of a programmed transistor. This is in contrast to EPROMs, which must be exposed to a UV-lamp to remove electrons from the floating gate. This usually requires the removal of the EPROM from the system.

Reliability Issues of FRAM

The major non-fabrication-related issues of FRAM reliability include data retention, fatigue, aging, imprint, and radiation. Data retention, one of the most important characteristics of non-volatile memories, is defined as the ability of a memory to maintain stored data between the time it is written and the time it is subsequently read. Although data retention is influenced at a fundamental level by design and manufacturing factors, retention failures are accelerated by high temperatures, which cause thermal depolarization of the poled state in the ferroelectric material. The signal loss due to data retention failures recovers after a rewrite and immediate read.

Fatigue occurs in ferroelectric materials with an increased number of switching cycles (read or write cycles) and is characterized by a decrease in switchable polarization. This process is related to the electrode interfacial areas of the memory cells and electric-field assisted migration of oxygen vacancies within ferroelectric materials.

Aging is similar to retention failure in that it is characterized by signal loss over time, but, unlike retention failures, failures due to aging occur during the retention period and do not recover after a rewrite and immediate read. During the aging process, a gradual stabilization of the domain structure occurs, which causes the ferroelectric material to become less responsive to applied electric fields.

Imprint is a reliability issue specific to ferroelectric material. Accumulation of charge in the ferroelectric cell over time make a capacitor

that has spent a significant amount in one polarity reluctant to switch polarities.

The radiation tolerance of ferroelectric memory is limited by the CMOS circuit elements. Prior studies have shown no significant difference between the radiation tolerance of commercial memory devices with and without ferroelectric material.

Reliability Issues of EEPROM

The reliability issues with EEPROM are very similar with the exception of imprint, which is specific to FRAM. In addition, the process by which fatigue occurs differs, and charge-trapping is an aspect specific to EEPROMs. During programming, the control gate of an EEPROM cell is made positive relative to the source-drain area. The floating gate is capacitatively coupled to the control gate, and when sufficient voltage is generated and the tunneling threshold is exceeded, electrons tunnel through the thin "tunnel" oxide window into the floating gate. The negative charge then remains trapped in the floating gate since inadequate voltage exists, normally to allow the electrons to tunnel back out. To erase the memory cell, the process is simply reversed. To read the cell, the control gate and source are brought to predetermined reference voltages and the current through the cells is measured. The transistor of a programmed cell is "on" and the transistor of an erased cell is "off".

Two basic types of failure occur when EEPROM cell are repeatedly written and erased: dielectric failure and charge trapping. Dielectric failures are the source of very low level random failures. They are caused by leakage through minor unscreenable flaws in the tunnel oxide. On contemporary production EEPROMs, dielectric failures are typically too rare to be noticed by standard lot sampling techniques until several hundred thousand write-erase cycles have passed. After this, they create a very low but visible level of random bit failures.

Charge trapping is the effect that creates intrinsic failure in EEPROMs. During write-erase cycling, small amounts of isolated negative and positive charge become trapped in imperfections in the tunnel oxide. Once trapped, the charge is no longer free to tunnel out of the oxide. In practice, electrons are more commonly trapped, and their presence creates a barrier to the tunneling of other electrons through the tunnel oxide. The apparent voltage needed to tunnel in either direction through the oxide increases. This reduces the amount of charge that can be moved in and out of the floating gate. When the accumulation of trapped charge becomes severe enough, it is no longer possible to move enough charge to clearly distinguish a one from a zero. At this point, the memory cells affected must be abandoned.

It is desirable to be able to program EEPROMs as quickly as possible. However, accelerating the programming of EEPROM cells requires the use of higher programming voltages, which accelerate the charge trapping mechanism and generally degrade the endurance of the EEPROM.

It might seem intuitive that tunnel oxide might degrade with endurance cycling and that data retention would suffer as a result. But the effect of cycling on the retention characteristics of EEPROM memory is very slight. That does occur is not due to increasing leakage through normal tunnel oxide, but the statistical influence of the random failures which are in fact caused by leakage through rarefied defects. The effect of cycling on the retention characteristics of before reaching the intrinsic limit of EEPROM memories is so slight, in fact, that it is usually ignored.

Tester Design

A custom memory tester was designed to create a low-cost, user-customizable testing for non-volatile memory that could perform reliability and endurance tests. The objective was to evaluate the reliability and endurance characteristics of various non-volatile memories for potential use in space applications.

A XILINX XC4010E 10,000 gate, 5V FPGA was chosen for the 5V memories, and a XILINX XC4010XL, a 3.3V version of the XC4010E, was chosen for the 3.3V memories. The tester board contains a parallel port for communication with a PC, an LED for error readout, and an EEPROM socket for PC-independent operation.

The tester can be configured to perform reliability or endurance tests, and each test can log errors in one of two ways. The error data can either be logged on a PC through the parallel port, or the tester can be used by itself, independent of a PC, by using an EEPROM to load the bit stream file and "scrolling" the error information on a 7-segment LED display. The memory tester configuration for a parallel FRAM is shown below.

This test bench offers several advantages over commercial testers when used for reliability and endurance testing. Endurance testing to a chip's specifications could involve more than 10^{10} read/write cycles, which can take up to 28 days for the Ramtron FM24C04 serial FRAM. Commercially available memory testers with high hourly rates may prove extremely expensive for testing NVMs with 10^{12} to 10^{15} read/write cycles. In comparison, the FPGA-based testers are inexpensive and more flexible. If several FPGA boards are used, many chips can be tested simultaneously at a fraction of the cost compared to the commercial testers. The highly portable, PC-independent nature of the test bench would also make it suitable for use in radiation testing, given proper shielding for the tester.

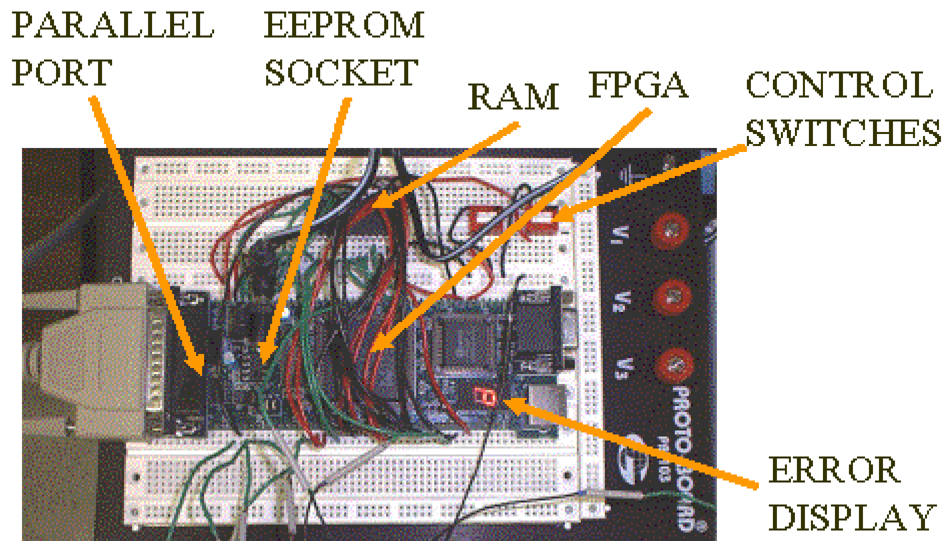

Figure 1: Non-volatile memory tester

Test Methodology

A MATS+ test was chosen to test the reliability of the non-volatile memories. In order to understand the test procedure, a brief example and explanation of Van de Goor's memory test notation is provided below:

```
UP(W10101010; R; W01010101)
– UP = Perform the entire set of operations in parentheses
from the first memory address to the last
– W10101010 = Write the data pattern '10101010'
– R = Read back the data
- W01010101 = Write the data pattern 01010101
–(Increment address and loop)
```

The MATS+ reliability test can detect address decoder faults and stuck-at faults, and was programmed to cycle through all the addresses in the memory. This reliability test was chosen because it met the minimum test criteria while fitting into the relatively small FPGA. Again using Van de Goor's notation, the MATS+ test is described as follows:

```
1. UP(W01010101)
2. UP(R; W10101010)
3. DOWN(R; W01010101)
4. LOOP BACK TO (2)
```

In order to test the endurance of the non-volatile memories, the following basic endurance test was used:

```
1.(W01010101; R; W10101010; R)
2. LOOP BACK TO (1)
```

Due to the prohibitive amount of time required to exhaust all addresses in the memories with an endurance test, it was decided that a single address or small range of addresses would be used instead.

Upon an error in during either test, the tester logs the total number of errors that have occurred, the number of read and write cycles at the point the error occurred, the memory address at which error occurred, the incorrect data value read, and (on the reliability test) it indicates the part of the memory test the failure occurred on. If the parallel port version of the tester is used, a simple program logs the data on the screen and gives the user the option of saving the data to a file. The other version of the tester, which is independent of the PC, scrolls the error information corresponding to the most recent error across the LED display, using various symbols to describe the data about to be displayed. An EEPROM is used in this tester so that a PC is not required to download the FPGA bit stream, which makes it completely independent of the PC.

Test Procedure and Preliminary Results

Memory testing is ongoing, and the results to date are preliminary. Three non-volatile memories are under test: Ramtron FM24C04 serial FRAM, Ramtron FM1808 Parallel FRAM, and the Northrop-Grumman's 256 kb Rad-Hard EEPROM. Reliability tests have produced no errors in any of the memories. Endurance testing on the Ramtron FM24C04 serial FRAM has exceeded the endurance specification of the chip ($1.0x10^{10}$ read.write cycles) by over four times (it has undergone $4.2x10^{10}$ read/write cycles) with no errors. Endurance testing on the Ramtron FM1808 parallel FRAM has not yet exceeded the endurance specifications, but no errors have surfaced to date.

	Status	# R/W Cycles (Endurance)	Endurance Spec
Ramtron Serial FRAM	Testbed complete: Both tests running	4.2E10	1E10
Ramtron Parallel FRAM	Testbed partially complete: endurance tests running	.6E10	1E10
NG EEPROM	Testbed work in progress	N/A	10,000

Table 1: Preliminary Results

Full test results will be available by December, 2001.

Concluding remarks

A custom memory tester was designed to create a low-cost, user-customizable testing for non-volatile memory that could perform reliability and endurance tests. The tester board contains a parallel port for communication with a PC, an LED for error readout, and an EEPROM socket for PC-independent operation. The main objective is to evaluate the reliability and endurance characteristics of various non-volatile memories for potential use in space applications. Testing is currently in progress for various memory chips. Results are expected form various tests in next two months.

Acknowledgments

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