Characterization of Scaled SONOS NVSM Devices for Space and Military Applications

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Abstract**—**We present results on scaled Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) non-volatile semiconductor memory (NVSM) devices designed specifically for high-density, EEPROMs operating in space and military environments. We describe scaling considerations and process optimization to achieve low-voltage operation (+7V write for 2.5 ms/-7V erase for 7.5 ms) with 10-year retention at 80C. We have conducted studies on 'oxynitride' films at temperatures ranging from 22-250C. An extrapolated 10-year memory window of 1.2V is obtained at 22C reducing to an acceptable 0.8V at 80C. SONOS device trap density profiles are compared for both 'oxynitride' and 'silicon-rich' nitride films.

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1. INTRODUCTION

Since the advent of the nonvolatile MNOS semiconductor memory in 1967 [1], there have been a wide variety of roles for nitride-based nonvolatile memory structures. Researchers at Northrop Grumman and Westinghouse Corporations have been involved in this work from almost its inception [2]. Northrop has been working with Sandia National Laboratories and Lehigh University in order to refine this technology for use in applications, such as satellites and nuclear technology. Our work focuses on the characterization of thermal acceleration effects with a goal of establishing a screening procedure to guarantee 10-year memory retention at +80 C.

In our studies, SONOS nonvolatile memory devices are fabricated with a gate dielectric consisting of an 18 A tunneling oxide, 80 A "oxynitride" layer, and a 40 A so-called 'blocking' oxide underneath a phosphorus-doped polysilicon gate [2]. The gate dielectric is programmed by applying either +7 V to the gate terminal for 2.5 msec, or a –7 V pulse for 7.5 msec. The applied voltage attracts electrons or holes to the surface of the silicon depending on the polarity of the gate voltage [3]. Subsequently, these carriers tunnel through an ultra-thin oxide and store in "traps" within a nitride layer. Fig. 1 shows the write/erase operation and Fig. 2 the electric field for tunneling.

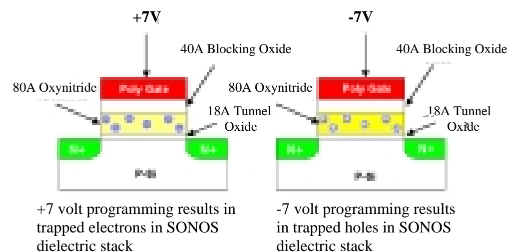

Figure 1–Write/Erase Operation for a SONOS Device

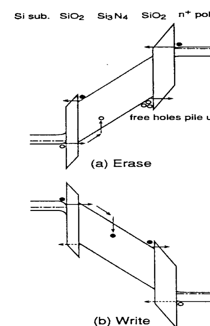

Figure 2 – Tunneling in a SONOS Device

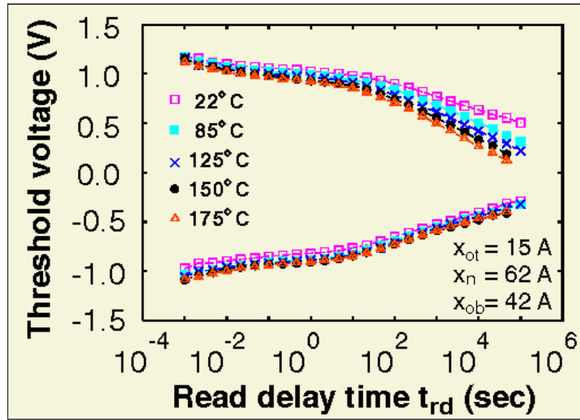

Figure 3 Threshold Voltage decay vs. Temperature for a 'silicon-rich' Scaled SONOS NVSM Device. The device has experienced 10^3 erase/write cycles. The initial V_{TH} is set with a series of erase/write pulses of ±7V, 1msec [13].

2. SONOS RETENTION AT ELEVATED TEMPERATURES – MODELING

The decay of the charge stored in the nitride layer at room temperature has been modeled by a number of investigators, such as White and Cricchi [4], Lundkvist, Lundstrom, Svensson [5], Roy and White [6], Kamagaki and Minami [7,8], and Hu and White [9]. These models invoke back tunneling of charge from the nitride to the semiconductor substrate. An internal field due to trapped charges enhances the process of tunneling.

The characterization of charge trapped in a nitride dielectric at elevated temperatures had been investigated for SNOS devices by Sandia researchers [10,11] and researchers from Chalmers University in Sweden [12]. Recently, with the advent of scaled SONOS devices, Lehigh researchers Yang and White [13] have examined the temperature dependence with an amphoteric trap model, which attributes the electron and hole charge storage to a silicon dangling bond. Their results, shown in Fig. 3, indicate the trapped 'electrons' in the nitride layer are thermally excited at elevated temperatures and 'back tunnel' through an ultra-thin tunnel oxide to the silicon. In contrast, the distribution of trapped 'holes' is influenced very little with increasing temperature. This result was explained by suggesting the activation energy for the electron traps lies closer to the conduction band edge in the silicon nitride than the activation energy for hole traps to edge of the valence band in the silicon nitride as shown in Figure 4.

Using this trap model, Yang and White [13] derived an expression for the charge trapped in the nitride,

$$\rho_n(x, E_{TA}, t) = -qg(x, E_{TA})f^- \qquad (1)$$

where E_{TA} is the energy level of the trap, f^- is the trap occupancy function for electrons, and $g(x,E_{TA})$ is the density of traps in the nitride (traps/cm^{3}eV) at a distance 'x' from the tunnel oxide-nitride interface into the nitride.

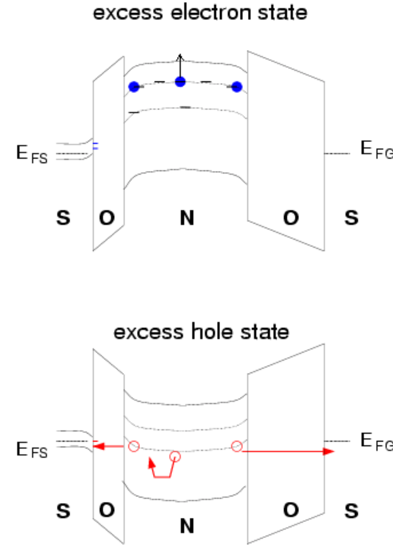

Figure 4 – Storage of Nitride Trapped Charge

The charge stored in the nitride causes a shift in the threshold voltage of the device, ΔV_{TH}, which can be written as [13],

$$\frac{\partial \Delta V_{TH}}{\partial \log(t)} = -2.3 k_B T X_N \left(\frac{X_N}{2\varepsilon_N} + \frac{X_{OB}}{\varepsilon_{OX}} \right) g(E_{TA}) \qquad (2)$$

where X_N and X_{OB} are the thicknesses of the nitride and blocking oxide, respectively, while ε_N and ε_{OX} are the dielectric constants of the nitride and blocking oxide, respectively. Equation (2) assumes a uniform distribution of nitride traps and the activation energy responsible for the decay rate is [13]

$$E_{TA} = k_B T \ln(AT^2 t) \qquad (3)$$

where A is a constant given as

$$A = 2\sigma_n \sqrt{\frac{3k_B}{m^*}} \left[\frac{2\pi m^* k_B}{h^2} \right]^{3/2} \qquad (4)$$

where σ_n is the trap capture cross-section, m^* the effective electron mass in the nitride and 'h' is Planck's constant. These relationships were used to interpret measurements of retention at elevated temperatures for retention times out to 10^5 seconds for the written state of a scaled SONOS device (See Fig. 3). Since the thermal activation energy of electron traps is near the conduction band edge, the electrons are thermally excited from these traps and back-tunnel through the tunneling oxide. Eqn. (3) shows the trap energy may be probed at a given temperature by measuring the slope of the decay characteristics as a

function of retention time. The capture cross-section, σ_n, may have temperature dependence.

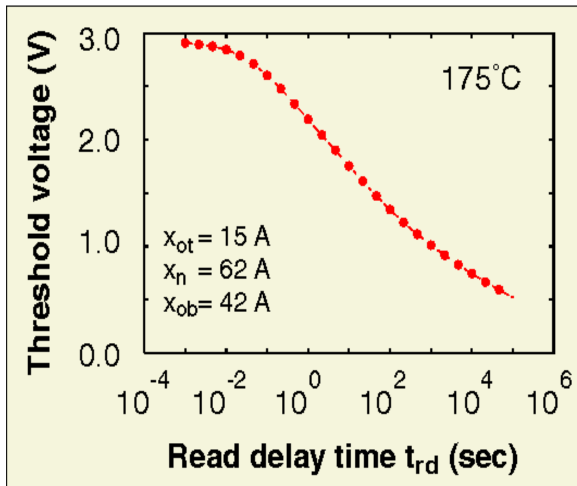

Figure 5 Threshold Voltage decay versus retention time for a Scaled SONOS NVSM device at T = 175C. The device is fabricated with a 'silicon-rich' nitride [13].

Using Eqns. 1-4, the decay rate of the threshold voltage [Fig. 5] was used to extrapolate the trap profile in the nitride of the silicon-rich nitride, as shown in Fig. 6.

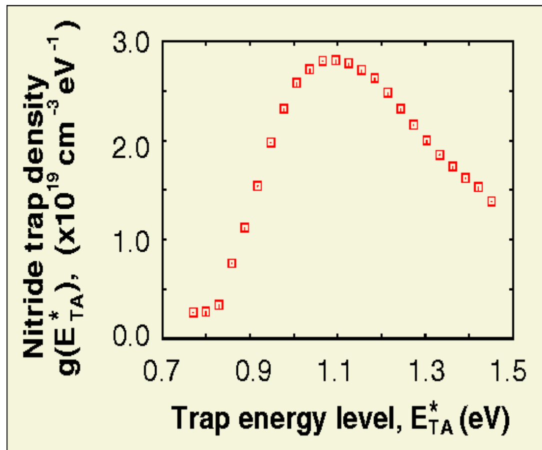

Figure 6 Nitride Trap Density versus Energy for a Scaled SONOS NVSM device with a silicon-rich nitride [13].

3. MEASUREMENT TECHNIQUE

Retention measurements at elevated temperatures are performed at the wafer level. As in the experiments of Yang and White, we use a hot chuck, ring probe stand, oscilloscope and an analog circuit [3,14] controlled by a desktop PC. The PC controls the oscilloscope through a GPIB interface with programs written in a LabVIEW™ environment. Fig. 6 illustrates a block diagram of the experimental set-up for dynamic measurements. These measurements include Erase/Write, data retention and endurance measurements as a function of temperature. If we include radiation performance, then these tests are the ultimate tests for NVSM devices from a user's standpoint.

The FPGA-based measurement system in Fig. 7 can execute all of these measurements. The function generator is designed and simulated with XILINX Foundation Software. The bit-streams are generated and downloaded to the FPGAs through a parallel download cable. The analog detection circuit, under the control of the specific erase/write/read pulses sets the operational modes to the SONOS device under test (DUT) and determines the change of the memory-state of the SONOS nonvolatile memory transistor. The TEK460 oscilloscope digitizes the analog threshold voltage output and sends the latter to the computer (PC). The data is filtered and averaged with a LabVIEW™ program on the computer and displayed on the monitor in real time.

The SONOS retention characteristics are monitored by applying programming pulses to the device, waiting a certain time t_r, and then forcing a constant current through the device and measuring the source voltage of the device as shown in the analog Detection Circuit of Fig. 8.

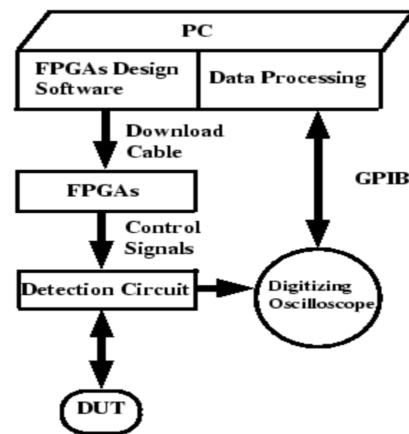

Figure 7 A Block Diagram of the Experimental Setup for Dynamic Erase/Write/Read Measurements [3].

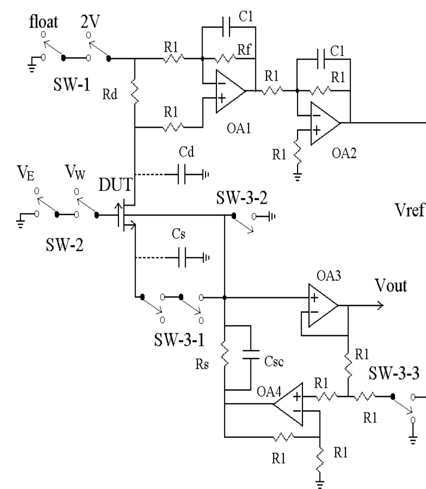

Figure 8 A constant-current, threshold-voltage detection circuit implemented with switches (SW) controlled by FPGAs[3,14]. The threshold voltage is monitored at Vout.

The measurements are performed on a hot chuck, which controls the temperature of the measurement environment and the wafer, as shown in Figs. 9 and 10.

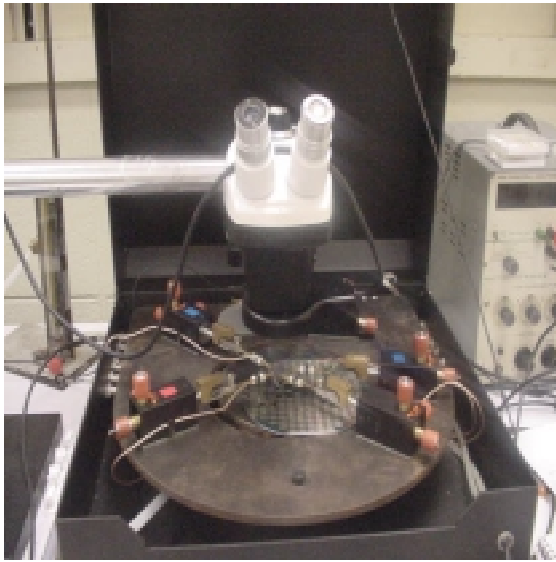

Figure 9 SONOS Wafer & Hot Chuck

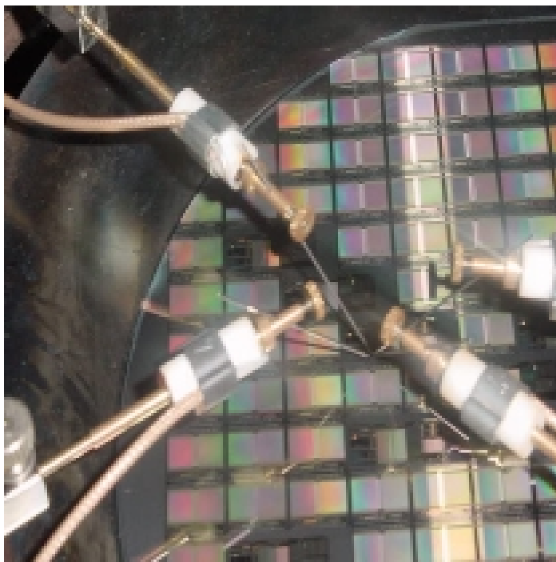

Figure 10 Close-up View of Hot-Chuck Probes on Wafer

The hot chuck is held at temperatures of 22 C, 80 C, 150C, and 250 C. The hot chuck used to collect this data has been operated routinely at temperatures up to 400 C. Due to this wear on the hot chuck, the surface where the wafer is placed is no longer planar. This created some difficulty in making good contacts with the probes onto the terminals of the device. When the device is heated and cooled, there is a degree of vibration associated with the operation of the hot chuck. When the temperature is increased to 125 C, the probes, which make contact on the device expand, and often slide off of the contact windows, scratching the device, and losing contact with the appropriate device terminals – especially for long-term retention measurements to 10^4 seconds. We compensate for these effects with special expansion probes and using smaller sections of the wafers. The smaller pieces are not affected by the hot chuck surface or by vibrations in the laboratory.

4. EXPERIMENTAL RESULTS

In this section, we describe retention measurements at Lehigh University on SONOS devices from the Northrop Grumman Corporation 0.8 um CMOS/SONOS 1M EEPROM project. The 'oxynitride' storage dielectric contrasts with devices fabricated with a 'silicon-rich' nitride. The thermally activated SONOS retention model is applied using Eqns. 1-4 to the retention data of 'oxynitride' SONOS devices taken at elevated temperatures to extract the energy distribution of the electron traps in the nitride. The retention measurements are performed, as described above, at temperatures of 22, 80, 150, and 250 C. A hot-chuck probe stand regulates the temperature. The SONOS devices are programmed with a 7V pulse applied to the gate for 2.5msec and erased with a –7V pulse applied to the gate for 7.5msec. The threshold voltage of the device is read for times ranging from 10^{-7} to 10^3 seconds.

The threshold voltage of the device in the Write and Erase states at elevated temperatures is shown in Fig. 11. The results demonstrate the decay rate of the written state is affected by increasing the temperature.

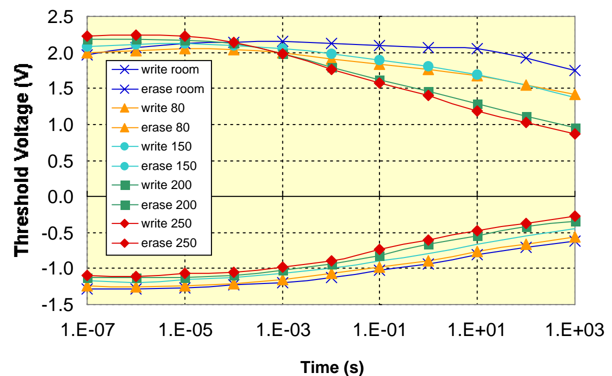

Figure 11 – V_{TH} vs time at various temperatures for an Oxynitride SONOS NVSM Device. The Write (excess electron) state of the device is affected by temperature. In contrast, the Erase (excess hole) state displays very little temperature sensitivity.

The Write state threshold voltage decay rate increases as the temperature increases. The Erase state decay rate is virtually unchanged. These trends are the same for both the 'oxynitride' [Fig. 11] and 'silicon-rich' nitride films [Fig. 3]. In both films we observe, for Write and Erase states, a small initial shift of the threshold voltage with increasing temperature.

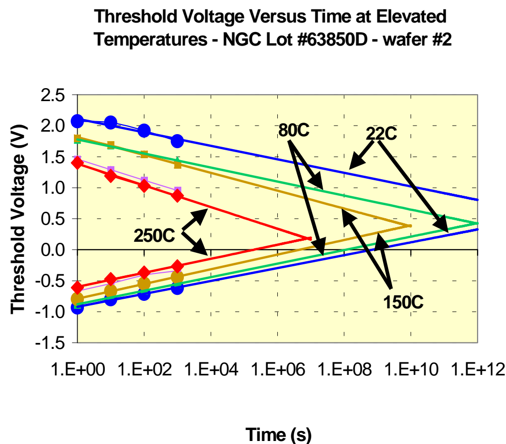

Figure 12 – Extrapolated V_{TH} vs Temperature

Long-term retention with temperature and radiation is of concern for space and military applications. The retention data has been extrapolated as shown in Fig. 12. At $3x10^8$ sec (10 years) and room temperature (22C) we have a 1.2V window. At 80C the window has decreased to 0.8V at 10 years and at 150C the window decreases to 0.3V. The data indicates these SONOS devices should be acceptable for 7 V programming and 10 year memory retention applications for operating temperatures below +125 C. Further optimization is continuing for the 1Mb SONOS EEPROM project.

The trap density in the nitride layer of the SONOS device is determined as a function of trap energy using Eqns. 1-4. Eqn. 3 is used to calculate the energies of the traps in the nitride layer. At 250 C the trap energy ranges from 0.6 eV to 1.43 eV. Eqn. 2 is used to calculate the density at points along the threshold voltage curve. The change in threshold voltage divided by the logarithm of the change in time is calculated at each decade of time. The electron trap density, $g(E_{TA})$, is plotted versus trap energy, E_{TA}, as shown in Fig. 13.

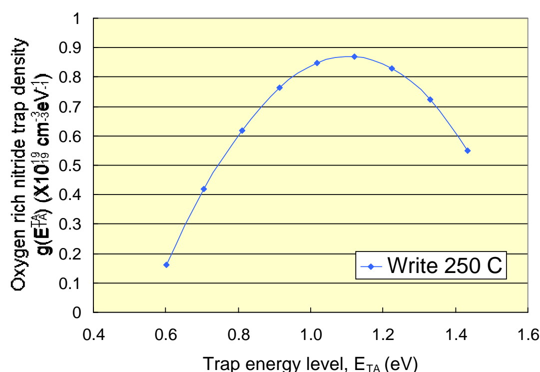

Figure 13 – SONOS Oxynitride Trap Density, $g(E_{TA})$, vs trap energy, E_{TA}, for the Write (excess electron) state.

The electron trap density for the 'oxynitride' film peaks at 1.1 eV below the edge of the nitride conduction band - similar to the 'silicon-rich' nitrides film shown in Fig. 6. The trap density of the 'oxynitride' film is less than the 'silicon-rich' nitride film. This expected as the presence of oxygen will 'tie-up' silicon dangling bonds, which cause the memory traps in the nitride.

5. CONCLUSIONS

The temperature effect on the threshold voltage of scaled (7V programming) SONOS 'oxynitride' NVSM devices has been investigated. At elevated temperatures, the Write state threshold voltage decay rate, $\partial V_{TH}/\partial \log(t)$, of 'oxynitride' and 'silicon-rich' nitride SONOS devices increases with increasing temperature, while the Erase state threshold voltage decay rate remains unchanged. We see from Fig. 12 the extrapolated memory retention window at 3×10^8 sec (10 years) and 22C is 1.2V, a 0.8V window at 80C, and a 0.3V window at 150C. We will take longer-term retention data in the future to see if there is a change in the decay rates, since the electric fields will be modified in the device with the loss of memory charge.

The nitride trap density is extrapolated from the decay rate of the Write state at 250 C. This allows us to see the trap distribution within the 'oxynitride' band gap. In previous studies of elevated temperature affects, Yang and White [13] have extrapolated the electron trap density for a SONOS device with a 'silicon-rich' nitride layer at 175 C as shown in Fig. 6. The trap density for a silicon-rich nitride layer is roughly three times greater than the density for an 'oxynitride' layer as shown in a comparison chart of Fig. 14. The 'oxynitride' and 'silicon-rich' nitride trap densities peak at the same activation energy, 1.1 eV.

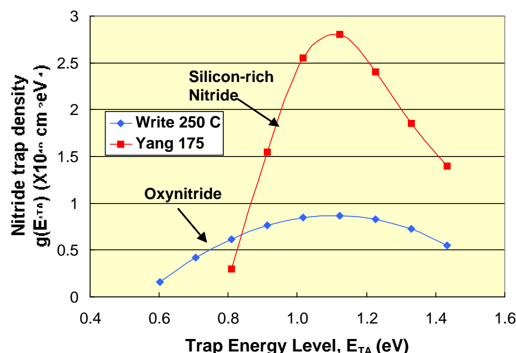

Figure 14 – A Comparison of Trap Densities in 'silicon-rich' and 'oxynitride' SONOS NVSM devices.

These preliminary measurements on scaled SONOS NVSM devices support the validity of high temperature screening measurements in the determination of long-term retention.

6. ACKNOWLEDGEMENTS

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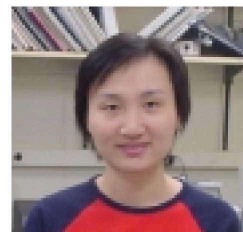
7. REFERENCES

[1] H.A.R. Wegener, A. J. Lincoln, H. C. Pao, M.R. O'Connel, and R. E.Oleksiok, "Metal Insulator Semiconductor Transistors as a Nonvolatile Storage", 1967 IEEE International Electron Devices Meeting (IEDM), Abstract 59, Washington, D.C.
[2] D. Adams, J. Murray, and M.H. White, "SONOS Nonvolatile Semiconductor Memories for Space and Military Applications", NVMTS, San Diego, CA, 2001.
[3] J. Bu and M. H. White, "Design Considerations in Scaled SONOS Nonvolatile Memory Devices", Solid-State Electronics, 45, 113 (2001).
[4] M. H. White and J. R. Cricchi, "Characterization of Thin-Oxide MNOS Memory Transistors", IEEE Trans. Electron Devices, ED19, 1280 (1972).
[5] L. Lundkvist, I. Lundstrom, C. Svensson, "Discharge of MNOS Structures", Solid State Elect, 16, 811(1973).
[6] A. Roy and M. H. White, "Determination of the Trapped Chare Distribution in Scaled Silicon Nitride MONOS Nonvolatile Memory Devices by Tunneling Spectroscopy, Solid-State Electronics, 34, 1083 (1991).
[7] Y. Kamagaki, S. Minami, H. Kato, "A New Portrayal of Electron and Hole Traps in Amorphous Silicon Nitride, J. Appl. Phys., 68, 2211, (1990).
[8] Y. Kamigaki, S. Minami, T. Hagiwara, K. Furusawa, T. Furuno, K. Uchida, M. Terasawa, and K. Yamazaki, "Yield and reliability of MNOS EEPROM products," IEEE J. Solid-State Circuits, 24, 1714 (1989).
[9] Y. Hu and M. H. White, "Charge Retention in Scaled SONOS Nonvolatile Semiconductor Memory Devices – Modeling and Characterization", Solid-State Elect., 36, 1401 (1993).
[10] S. L. Miller, "Effect of Temperature on Data Retention of SNOS transistors", 8th IEEE NVSM Workshop, Vail, Co. August 1986.
[11] P.J. McWhorter, S. L. Miller,T. A. Dellin, "Modeling the Memory Retention Characteristics of Silicon-Nitride – Oxide Silicon Nonvolatile Transistors in a Varying Thermal. Environment, J. Appl. Phys, 68, 1902 (1990).
[12] L. Lundkvist, C. Svennsson, B. Hansson, "Discharge of MNOS structures at Elevated Temperatures", Solid-State Elect., 19, 221 (1976).
[13] Y. Yang and M.H. White, "Charge Retention of Scaled SONOS Nonvolatile Memory Devices at Elevated Temperatures", Solid State Elect., 44, 949 (2000).
[14] A. Roy, F. R. Libsch and M. H. White, "A Microcomputer-controlled Multichannel Programmable Pattern Generator", IEEE Trans., on Instr. and Meas., IM-36, March 1987.

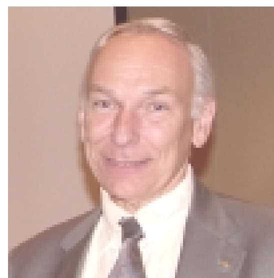
8. BIOGRAPHIES

Stephen J. Wrazien was born in Windsor, Connecticut on May 7, 1978. He received a B.S. degree in Electrical Engineering from the University of Scranton in 2000, and is currently pursuing an M.S. degree in Electrical Engineering from Lehigh University to be completed in June of 2002. He is currently working as a research assistant at Lehigh University's Sherman Fairchild Lab and studying SONOS nonvolatile memory devices.

Jonathan M. Faul was born in Bethlehem, Pennsylvania on February 15, 1981. He is currently pursuing a B.S. in Physics with a concentration in Astrophysics at the Harvey Mudd College, to be completed in May 2003. As part of Lehigh University's Summer Physics Program 2001, Jon worked at the Sherman Fairchild Lab with graduate students focusing on SONOS device characterization.



Yijie Zhao was born in Shanghai, China on July 24, 1977. She received her B.S. in Communication Engineering from Shanghai Jiao Tong University in 1999. She joined Lucent Technologies Optical networking in China after graduation, where she worked as an electrical engineer for two years. She enrolled as a graduate student at Lehigh University in September of 2001, and is pursuing her M.S. in Electrical Engineering as a research assistant at Lehigh University's Sherman Fairchild Laboratory. She is conducting research focusing on SONOS nonvolatile memory devices.



Marvin H. White was born in the Bronx, New York on September 6, 1937. He received an A.S. degree in Engineering from the Henry Ford Community College (1957) a B.S.E. degree in Physics and Math (1960), M.S. degree in Physics (1961) from the University of Michigan and a Ph.D. degree in Electrical Engineering (1969) from the Ohio State University. In 1961 he joined the

Westinghouse Solid-State Laboratory in Baltimore, MD, where he worked on advanced military and NASA imaging systems. From 1961 - 1981 he worked at Westinghouse as an Advisory Engineer in the design of low-power, custom integrated circuits with technologies of CMOS, Bipolar, MNOS and CCDs. During this period he was an adjunct Professor at the Electrical Engineering Department of the University of Maryland and a visiting Fulbright Professor at the Catholique Universite' de Louvain in Louvain-la-Neuve, Belgium.

In 1981, he became the Sherman Fairchild Professor in Solid-State Studies and Electrical Engineering at Lehigh University. At Lehigh he has developed a graduate program in microelectronics with research on SONOS nonvolatile memory devices, CMOS device modeling, studies of the Si-SiO_2 interface, SiC devices, and custom integrated circuits and sensors. He has graduated 25 Ph.D. students in microelectronics. He has served as a Visiting Researcher at the Naval Research Laboratories (1987) and a Program Director in Solid- State and Microstructures at the National Science Foundation (1995-96). In 1997 he received the Eleanor and Joseph Libsch Research Award at Lehigh University. He is currently the Director of the Sherman Fairchild Center for Solid-State Studies.

Prof. White is an IEEE Fellow (1974) and the recipient of the J. J. Ebers Award (1997) and the Masaru Ibuka IEEE Consumer Electronics Award (2000). He is also a member of the National Academy of Engineers (2001). In 1982 he was the IEEE Electron Devices Society (EDS) National Lecturer and is presently a Distinguished EDS Lecturer. He has served on IEEE/EDS committees, in particular, membership, and education. He is a member of Eta Kappa Nu and Sigma Xi.

Dennis A. Adams is a Consulting Engineer in the Northrop Grumman Corporation Silicon Technology department. He joined Northrop Grumman Corporation (nee Westinghouse Electric) in 1976 after receiving a BSEE degree from Northwestern University in Evanston, Illinois. He completed his MSEE at the University of Maryland in College Park, Maryland in 1979.

During his 25year career at Northrop Grumman, Mr. Adams has been involved with all aspects of development of digital, analog and memory silicon integrated circuits for avionics and space applications. His work has included bipolar, CMOS and CCD technologies on both bulk silicon and silicon on insulator (SOI) starting materials. He has successfully served as technical director for numerous products including 16K/64K SRAMs, 64K/256K EEPROMs, 10K/20K/60K CMOS Gate Arrays, 30K Custom ASICs, 45K SOS 1750A CPU, 4K FPGAs and various BiCMOS smart-power devices. He has specialized in radiation-hardened technology and has personally been responsible for several process integration innovations that have led to the current company portfolio of 100 Krad to 1 Mrad technologies.

Mr. Adams chairs a Yield Enhancement Task Force that is responsible for resolving manufacturing issues and improving product yields for all NGC silicon products. He is also involved in new process technology development. Current activities include 5V/ 15V/40V/ 100V BiCMOS, 0.5 μm BiCMOS (with SiGeC HBT's), submicron (0.12 μm / 0.5 μm) CMOS/SOI and radiation hard 0.8 μm CMOS/SONOS.

Mr. Adams has authored over 35 technical papers and made 20 conference presentations in the area of digital and memory integrated circuit technology for avionics and space applications. He has received 7 patent disclosure awards.

James R. Murray was born in Mt Clemens, Michigan on August 6, 1960. He received the B.S. and M.S. degrees in electrical engineering from Texas A&M University in 1982 and 1983, respectively. In 1984, he joined Sandia National Laboratories, Albuquerque, NM where is currently a Principal Member of Technical Staff. From 1984 to 1988 he was involved in the design of radiation hardened mixed signal ASICs. Since 1988 he has been involved in the design of radiation hardened nonvolatile memories. He is currently working on a radiation hardened 1Mb EEPROM, cache memories for a radiation-hardened microprocessor, and a radiation-hardened FPGA.