



The 2nd Annual, Non-Volatile Memory Technology Symposium

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Europa Orbiter Mass Memory Requirements & Status

Study Contributors:

Wayne Arens

Taher Daud

Dan Karmon

Alan Nicholson

Karl Strauss

Why am I here?

- Tell you about the Europa Orbiter Mass Memory requirements
- Tell you about our current status
- Challenge you to come and talk to us regarding alternative solutions.





The challenge of the mission to Europa.

Memory shall meet all performance specifications after being exposed to a radiation TID of:

- 20 Mrad (10 Mrad environment, RDF = 2) inside the S/C bus, but not enclosed in an IFDP electronics chassis; **Or**,

- 1 Mrad (500 Krad environment, RDF =2) if enclosed in the Avionics chassis

50 Krads (25 Krad environment, RDF = 2) if enclosed in an IFDP electronics chassis and shielded by the equivalent of an IFDP tungsten vault.

Memory shall be designed for a 15 year life

Need Dates.

EM TO JPL DEC. 2004

FLT to JPL March 2005

Other requirements on the list.

Any device chosen shall not latch-up when exposed to the single events effects environments specified for EO.

The uncorrectable data error rate shall not exceed 10^{-10} bit errors per day.

The memory shall be capable of operating at the continuous read or write rate of 20 Mbits/second.

The memory shall be capable of having data written into each storage location a minimum of 100,000 times.

Memory assembly mass shall not exceed 20 kg. As a goal, the mass shall be no greater than 11 kg.

Power consumption of the memory assembly shall not exceed 15 Watts. As a goal, the power required shall be no greater than 10 Watts.

If power is to be supplied by the spacecraft primary power bus, the memory shall operate nominally over an input voltage range of 22-36 VDC.

Baseline Size Requirements

1/4/01 study identified the baseline memory requirements:
0.9 Gbits of non-volatile memory and 3.6 Gbits of volatile memory

Memory storage requirements (EDAC not included)

Data Type	Non-Volatile CBE	Non-Volatile Allocation	Volatile CBE	Volatile Allocation	Margin ¹
S/C Flight Software	0.268 Gb (32 MB)	0.670 Gb			60%
Sci. Instr. Flight Software			0.268 Gb (32 MB)	0.670 Gb	60%
Orbital Engineering Data	0.121 Gb ²	0.173 Gb	0.518 Gb	0.741 Gb	30%
Orbital Science Data			1.496 Gb ³	2.200 Gb	32%
S/C State Data	TBD [64 KB]	TBD [164 KB]			60%
Total ⁴		0.843 Gb		3.611 Gb	
Write Cycles	15500, est. 12/99	Limit 100K Lifetime 150K			

Notes:

1. Margin = (allocation - CBE) ÷ allocation
2. 14 days of 100 bps data
3. 3 days of science data
4. If all storage is non-volatile, Total = 4.281 Gb because non-volatile engineering data (0.173 Gb) is a subset of the volatile engineering data allocation (0.741 Gb) (to simplify memory management).

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Implementation Considered

- Considered a divergent set of technologies:
 - DRAM, SRAM, Flash, Disk
 - FeRAM, MRAM, Chalcogenide
 - Cassini-style BAIL board
 - EEPROM, ROM

Candidate Technologies Summary

Type	Cap'y	Volatile	Rad Tol (kRads)	Clamshell?	notes
DRAM	256 Mbit	Y	Lo (30-60)	N	
SRAM-RH	4 Mbit	Y	Very Hi	N	>1024 devices req'd
Flash	256 & 512 Mbits	N	Very Lo (7 – 30)	Y	
EEPROM	1Mbit	N	Hi (300)	N	
Disk	1 GByte	N	Lo ? (30?)	Y	In test
FeRAM	256K – 4 Mbit	N	Hi – Very Hi	N	Needs Development
GMRAM	1 Mbit	N	Very Hi	N	Needs Development
C-RAM	1 – 16 Mbit	N	Very Hi	N	Needs Development

Prime Technologies & Methodology

- 5 Technologies were chosen for further study: DRAM, SRAM, EEPROM, Flash, Disk Microdrive
- Mass-power-volume-cost counterpoint analyses were generated for each.
 - Interfaces were studied. Ease of use determined. Cost and development schedule estimated. Risk of success qualified.
- At first, technologies were studied “stand alone.” Later, technologies were blended to see if a synergy developed. *It did*

A quick Discussion of the Primes

- DRAM and SRAM offer ease of use, but also present inherent risk in that a Power Bus Fault could occur
- DRAM has remarkably high density, but can exhibit ‘SEFI’ conditions (Single Event Functional Interrupt: Single event mode change)
- Too little is currently known about the Microdrive to either Rule In or Rule Out
 - under Investigation
- Flash standalone is not currently considered viable for this mission, however, if Flash is blended with DRAM -- **A Reasonable, Low Cost Solution Emerges**

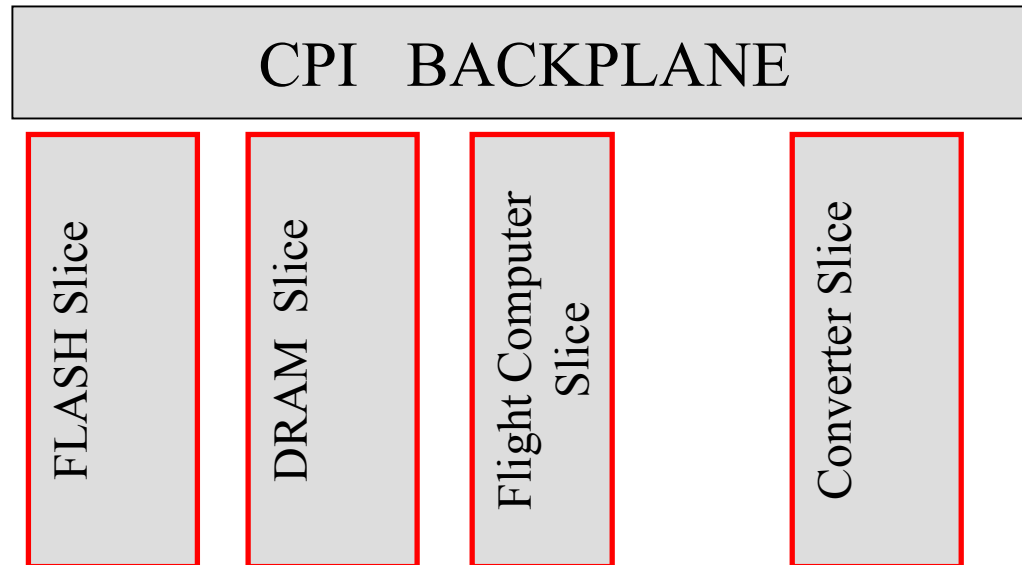
Proposed Solution (DRAM + Flash)

Current Europa Baseline

- A solution utilizing existing X2000 Flash Memory Cards (SEAKR) + developing a new DRAM card was considered
 - very low risk, lowest cost, fastest development

Proposed Implementation (DRAM +Flash)

cCPI Backplane Implementation



The Flash Part

- Flash memory would be used for computer boot and FSX storage; OFF for >95% of the time.
- In this mode, the Flash devices achieve a Total Dose tolerance of ~ 30 kRads* --- this is roughly equivalent to the TID for the DRAMs used on the SFC

*(50 - 70 kRad regime if no writes occur past 10-12 kRad exposure)

Non-Volatile Memory

Contractor: SEAKR

Functionality:

Bulk Data memory

Specs:

Mass: With Clamshell: 1.6 Kg; Without Clamshell: 0.34 Kg

Power: 2.3 W (max) @ 3.3V operating voltage

Radiation: With Clamshell: TID: 30 Krad, 1Mrad ASIC

SEE: 3.7 E^{-14} word errors/day

Without Clamshell: TID: 8-12 K Rad

SEE: No Latch Up

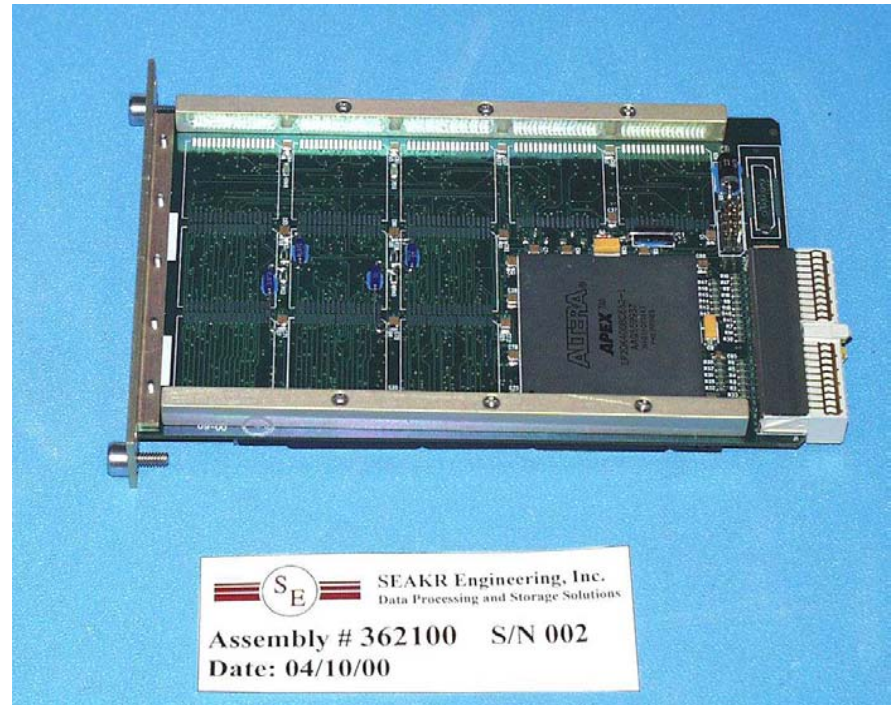
Interfaces: PCI Interface

Mechanical Form: Double Sided 3U Compact PCI Card

Features: 256 Mbytes Data capacity

Data Rate: 4 kb Burst Rate 200Mbit/sec

Option: Removable Clamshell



PT Non-Volatile Memory Slice

The DRAM card

- A new DRAM card would be developed-- this card would be boot-loaded with active program(s), and/or science, engineering, and telemetry data
 - Very simple design

Other Bits and Pieces- BUT not the end

- Additional variations on the subject where outlined-not reported here. The principle remains the same.
- IBM Microdrives are currently under test
- *We are still looking for a solution. A viable solution for mass memory, non-volatile and other, is needed by all missions.*
- Given that the Flash, DRAM, and Microdrive components are Commercial Off The Shelf, the very real possibility exists that parts tested and acceptable *today* may not be available *tomorrow*

