Challenges in Implementing Commercial Non-Volatile Memory in Spacecraft Solid State Recorders

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Abstract— SEAKR Engineering produces a variety of Solid State Data Storage and Processing Systems for use in applications from avionics to deep space. Power requirements for deep space missions require the use of non-volatile storage system. For the JPL X2000 program, SEAKR selected FLASH memory for use in the PCI Non-Volatile Memory Slice (NVMS). While FLASH Memory offers a significant power advantage for interplanetary missions, there are several constraints intrinsic to FLASH memory devices that must be resolved by the system design. These features include; radiation sensitivity, slow read/write speed, bad memory blocks, limited write cycles, and electro-magnetic noise. This paper describes how these features were resolved and the tradeoffs that were made to accommodate the use of FLASH memory in an interplanetary environment.

TABLE OF CONTENTS

1. INTRODUCTION

SEAKR Engineering provides solid state memory systems, digital signal processors, and memory boards to the international space and avionics communities. SEAKR Engineering now has over 21 successful on-orbit memory systems supporting missions ranging from low Earth orbit to interplanetary spacecraft.

The interplanetary environment presents special challenges to the use of solid state memory. Of primary concern is limited power availability. Limited power drives the need for the use of a non-volatile system as a non-volatile system uses no power unless it is undergoing a read/erase/write cycle. Environmental radiation is the second major concern. Since interplanetary spacecraft are not shielded by the earth's magnetic field, the memory system must survive a high level of natural radiation. The capabilities of memory devices must be evaluated under these conditions to ensure a successful mission.

SEAKR Engineering is working with JPL's X2000 program to developing a non-volatile PCI memory card, the Non-Volatile Memory Slice (NVMS), for use on multiple interplanetary missions.

The SEAKR Engineering NVMS FLASH Memory Card is a multi-capacity memory storage module conforming to the Compact PCI architecture. The NVMS card consists of up to eight memory banks, with each containing up to 256 MB of memory.

2. NON-VOLATILE MEMORY SELECTION

SEAKR Engineering generally builds Non-Volatile memory cards using commercial FLASH memory. However, considering the requirements of the X2000 program, several other types of non-volatile memory were considered. A brief description of the non-volatile memory technologies considered are listed below.

FRAM (Ferroelectric RAM) uses the ferroelectric effect for a storage mechanism. A FRAM memory cell is made by depositing a film of ferroelectric material in crystal form between two electrode plates to form a capacitor. Data is stored within the crystalline structure. FRAMs have a design similar to other RAM devices in that it reads and writes simply and easily, but differs as no applied power is required to hold the data state. FRAM data is read using a switched charge that determines the state of the ferroelectric memory. In the process of reading the data, the data is changed; therefore, additional circuitry must be used to re-write the original data back to the memory cell. FRAM uses a direct 5V supply. FRAM generally shows high tolerance to both Single Event and Total Dose Radiation effects. FRAM is capable of a high number (~10 billion) read/write cycles. FRAM is an emerging memory technology and is available from a few sources as low-density (256 **K**bit) parts

GMRAM, or Giant Magnetoresistive RAM, is an emerging technology that uses magnetic spin to record data bits. GMRAM has the potential for densities similar to SRAM with comparable read/write cycle times. For all it's promise, GMRAM still has some technical difficulties to work through; reducing drive currents, eliminating cell instabilities due to magnetization vortices, and improving operations at nanometer densities. The biggest problem for use on the X2000 data recorder is availability of parts. It will be several years before GMRAM is available in economic quantities.

FLASH Memory uses floating gate technology for the non-volatile memory cell. Reading and writing to FLASH requires more complicated programming than DRAM, resulting in slower performance. FLASH usually contains a low number of bad blocks when manufactured and can develop additional bad blocks over the lifetime of the part. FLASH is susceptible to radiation effects and can generate electro-magnetic noise that can interfere with other spacecraft instruments. FLASH memory is widely available from several commercial sources in densities up to 256 Mbit.

After an evaluation of these devices, FLASH memory was selected for use in the X2000 NVMS memory board. This decision was based mainly on part density and availability.

3. FLASH CHALLENGES

The non-volatile aspect of FLASH memory is accomplished by using floating gate technology. A floating gate cell consists of a FET with an insulated floating gate located between the control gate and the substrate. An embedded state machine controls each cell. One of the more interesting things about FLASH memory is that the cells can only be changed from 0 to 1 state by an erase operation and can only be changed from a 1 to a 0 state by a write operation. Therefore, reprogramming usually requires an erase cycle followed by a programming cycle. This requirement results in a slower read/write cycle than that required for an equivalent capacity DRAM.

Radiation capability of FLASH Memory is mixed in regard to Single Event Upset (SEU), Single Event Latchup (SEL), and Total Ionizing Dose (TID). FLASH devices are relatively immune to SEU as the devices are only susceptible to SEU when the device is undergoing a read/write/erase cycle. Since FLASH is not powered during most of it's life, the opportunity for a SEU event is very small. Destructive SEL is a concern. The susceptibility of FLASH memory to SEL is highly dependent on the component's design and the manufacture's processes. SEAKR has seen wide differences between different manufacturers in regard to SEL. TID is also a concern for FLASH memory. In continually biased FLASH memory systems total TID tolerance can be less than 5 Krads. If the FLASH is unbiased when not in use, the TID tolerance is greatly improved, into the 35 to 50 Krad range[1].

Commercial FLASH memory is supplied with bad blocks. Rather than screen out devices with defective memory blocks, FLASH memory manufacturers have elected to sell devices with a limited number of bad blocks. This reduces the need for redundant circuitry to ensure the entire memory can be utilized within a device. The location of each bad block is provided by information written to each part. It is considered more cost effective to manage the bad memory locations than produce parts that have 100% good memory. Commercial specifications typically permit up to 20 bad blocks in a 2048 block device. While this philosophy works well in the commercial world, it leads to unnecessary memory waste in spaceflight systems.

FLASH devices require a high current during write and program cycles. This current generates a significant electromagnetic field that can inject noise into the system. For most applications this noise goes unnoticed, but in space probes this EMI can affect nearby sensitive scientific instruments.

The number of Write/Erase cycles is limited for FLASH memory. This is due to gate oxide damage that can accumulate during each cycle. The limit is often improved as the manufacturer's process matures. In mature products, the published limit on write/erase cycles may be due to the inability to accumulate enough test cycles to prove the actual physical limit.

4. FLASH TRADE-OFFS ON X2000

The NVMS design had to account for each of the challenges presented by the selection of FLASH devices as our storage media.

Writing to multiple FLASH devices (10) simultaneously minimized the speed limitations. In addition, the X2000 NVMS design includes two banks of memory, each with a dedicated 2-Kbyte First-In First-Out (FIFO) buffer, that can be alternately written allowing both banks to be programmed simultaneously.

Radiation concerns were satisfied by a series of SEL and TID testing on devices from several manufactures. This testing found the Samsung 128 Mbit FLASH provide the greatest imunity to SEL and TID[1]. The TID radiation performance limitation was handled by enclosing the FLASH memory devices inside a 0.25 inch Tungsten shell. This shell increases the TID tolerance by approximately a factor of four (4). In addition, the NVMS design includes a power switching capability for the FLASH devices allowing operational planning to further increase the FLASH TID tolerance by powering down the devices when not in use.

To reduce the number of bad blocks in spaceflight the NVMS, SEAKR selects parts using tighter criteria than commercial processes. FLASH memories for space systems include additional screening of the devices to "cherry pick" parts that have fewer bad blocks. This process reduces the lot yield but increases available memory. Past experience has show low yield loss for devices with 15 or less blocks. The X2000 NVMS maximized available memory by screening devices to 10 blocks or less.

SEAKR selects FLASH devices only from mature product lines minimizing read/write cycle limitations. The effects of wear-out are further mitigated by software leveling routines. These routines control the wear on a given block by distributing the data evenly throughout the device. Thus exercising the entire device and not just one area. Though effective in wearing the device evenly, it is still subject to the fundamental limited life problem intrinsic in the FLASH technology.

Careful consideration must be given to power and ground plane noise immunity. FLASH devices exhibit a fairly high instantaneous current during write and program cycles, generating considerable noise in the system. This problem can be reduced by PCB layer placement, routing techniques, and decoupling capacitors. Power and ground planes are used in the NVMS. Loop area is kept to a minimum. Large and small bypass capacitors are used and placed very close to power and ground pins of the devices. This offers low impedance to ground in different frequency domains as well as charge storage. PCB layer placements are such that every signal layer has a reference plane.

5. CONCLUSIONS

A well-designed non-volatile memory system based on FLASH memory can meet the requirements of interplanetary science missions. Design of this system must compensate for FLASH's shortcomings in speed, radiation tolerance, noise, and read/write cycle life. Compensation for these shortcomings does result in cost to the mission in complexity, weight, performance and dollars.

These costs could be avoided if a non-volatile memory was available that performed similar to standard DRAM. The FRAM and GMRAM considered for use on X2000 continue to hold promise. Newer technologies such as chalcogenide based RAM and battery backed up SRAM are also being considered for future designs. SEAKR will incorporate these new technologies into our PCI NVMS when it becomes technically and economically feasible.

By understanding the advantages and limitations of FLASH memory, SEAKR Engineering is able to construct a PCI Non-Volatile Memory System suitable for interplanetary missions using currently available technology.

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[1] D. R. Roth, J. D. Kinnison, et al, "SEU and TID Testing of the Samsung 128 and the Toshiba 256 Mbit FLASH Memory", 2000 IEEE Nuclear and Space Radiation Effects Conference.