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Title: **Radiation Test Results of the *Virtex* FPGA and ZBT SRAM for Space Reconfigurable Computing**

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Radiation Test Results of the *Virtex* FPGA and ZBT SRAM for Space Reconfigurable Computing

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Overview

- **Motivations**
- **Candidate Technologies**
- **Radiation Testing and Results**
- **SEU Mitigation Plans**
- **Thermal Considerations**
- **Summary**

Motivations for Reconfigurable Computing

- **High density / high performance system on a chip capability on orbit**
- **On orbit reconfiguration / application evolution**
- **Digital signal & image processing in real time of remote sensing data**
  - **Assumption: Occasional loss of data is a tolerable trade for increased processing capability**

Candidate Technologies

- Focus on refinement of state-of-the-art COTS to tolerate the space environment
  - Xilinx SRAM based FPGA
  - Micron, IDT, or Motorola Synchronous SRAM
- Utilize Non-Volatile, Rad-tolerant Controller
- Assure total dose tolerance and latch-up immunity through proper selection of foundry
- Characterize SEU in order to develop mitigation strategy
- Emphasize thermal management for packaging reliability

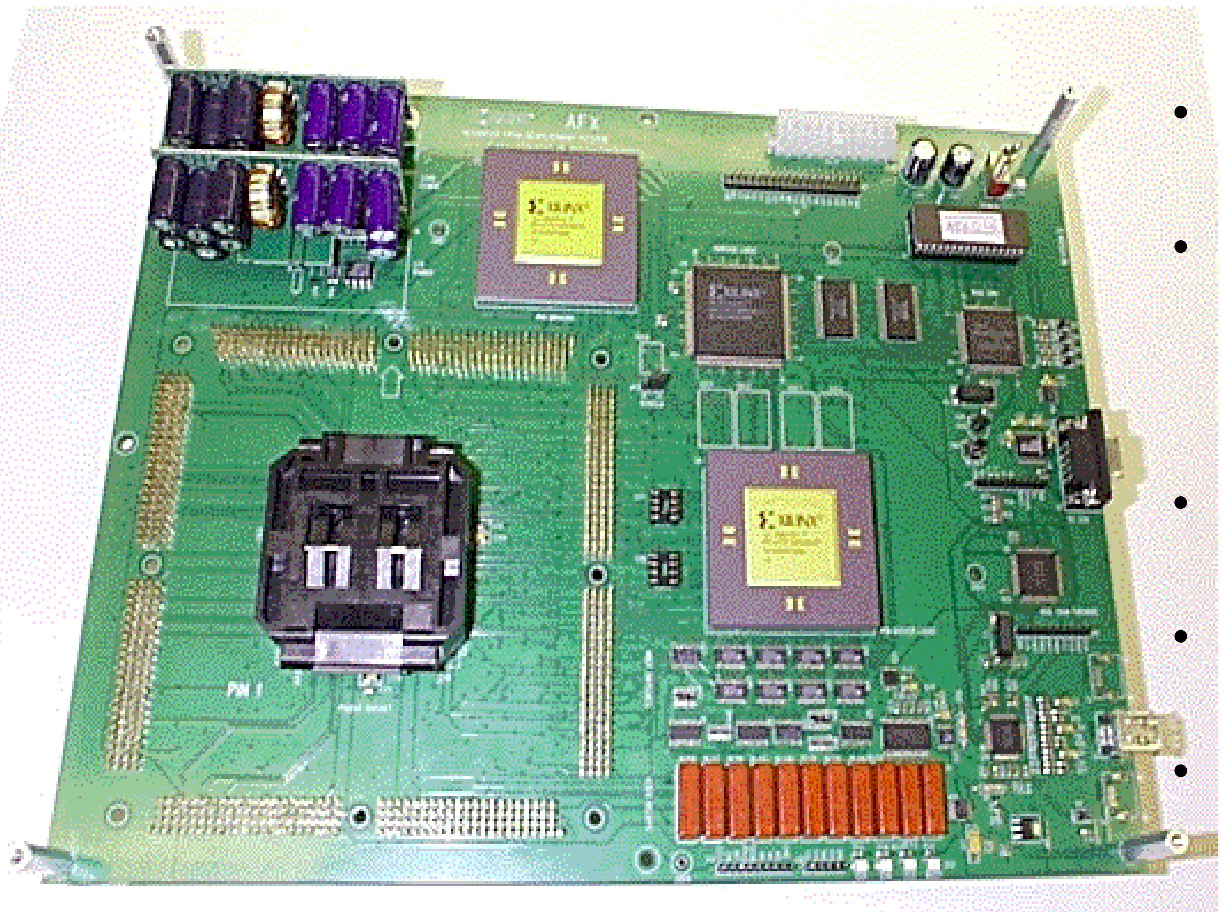
Virtex FPGA from Xilinx

- **System gates range from 50,000 to 1,000,000**
- **Xilinx measured total dose tolerance greater than 50krads(Si)**
- **XQVR300 used for SEE Characterization**
- **Architecture:**

		XQVR300 bits
• Array of Configuration Logic Blocks	CLBs	6,144
• Programmable I/O Blocks	IOBs	948
• Look up tables	LUTs	98,304
• Block SRAM	BRAM	65,536
• Delay lock loops	DLLs	
• Configuration / Interconnection by routing bits		1,579,860
• Equivalent system gates		322,970

- **Technology is SRAM based, 0.22μ CMOS on epi with 5 metal layers**

FPGA Test Fixture: Xilinx AFX



- On/Off board power supply
- Configuration & readback in concert with PC controller
- Set/read all IO
- Multiple package support
- Developed by Xilinx

Test Strategy

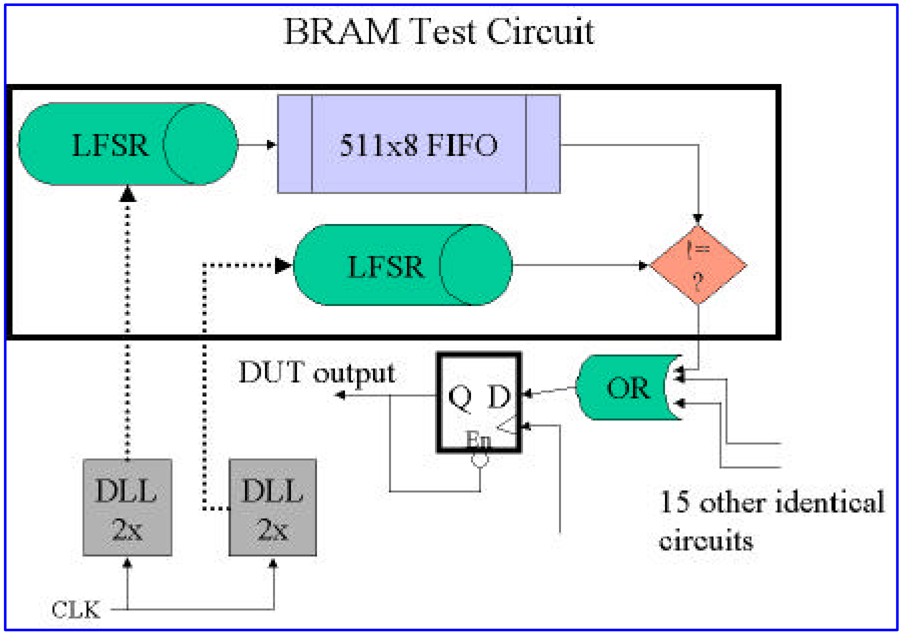
- **SEL**
  - **External current monitor**
  - **Reconfigure to investigate contention vs. latch-up**

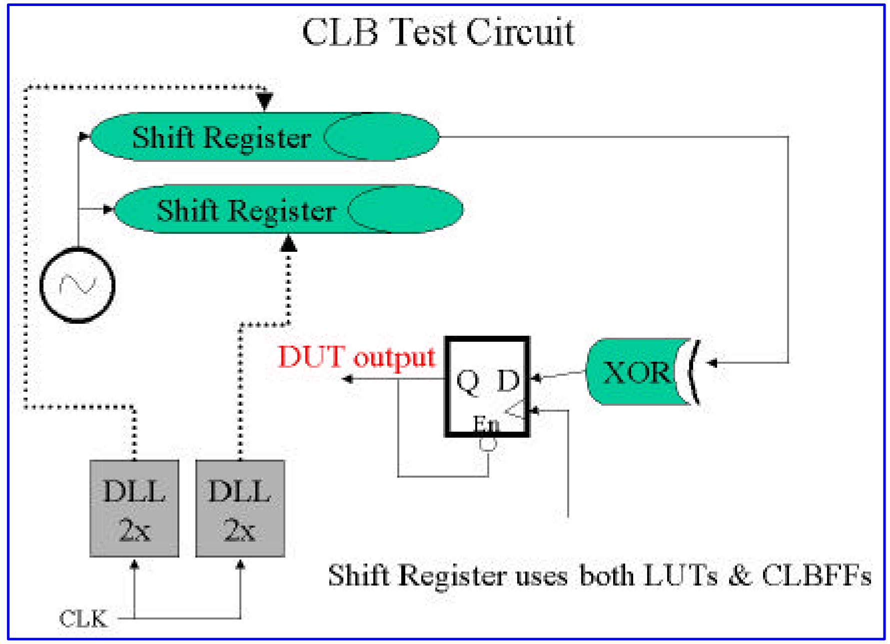
- **Static SEU**
  - **Configure and readback all bits via serial scan**
  - **Measure upset sensitivity of bit types**
  - **Monitor current**

- **Dynamic SEU**
  - **Create different designs to highlight blocks of technology**
  - **Vary frequency of operation from 5MHz to 80MHz**
  - **Measure fluence to dynamic upset**
  - **Readback configuration serially to monitor upset bits**

- **Functional Interrupt**
  - **Monitor upset signature**

Dynamic Test Circuits





Device Utilization:

Slices	24%
BRAM	100%

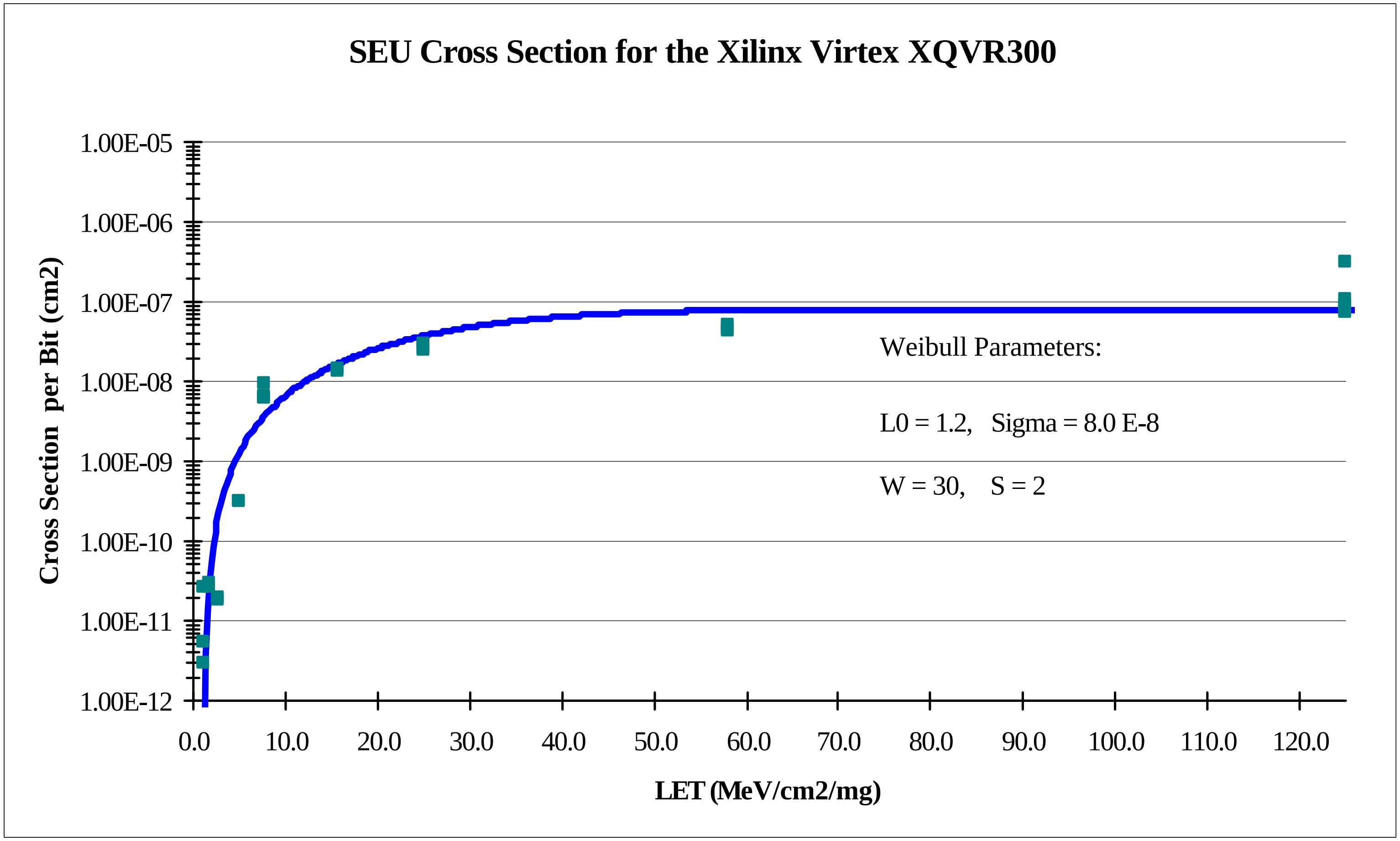
Device Utilization:

Slices	95%
BRAM	0%

SEE Test Results

- **ZBT SRAMs**
  - **Latch-up observed on all samples at an LET of 60 MeV-cm^2/mg**
- ***Virtex* FPGA**
  - **No latch-up to an LET of 125 MeV-cm^2/mg**
  - **Static upset characteristic measured on the FPGA**
  - **Dynamic upset contributions observed**
  - **Configuration register upset mode investigated**

Virtex FPGA Static SEU Sensitivity



Comments on Observed SEUs

- **Static upset sensitivity varied only slightly across latch types**

	L_0	Sigma
• CLB	5.0	6.5 E-8
• LUT	1.8	2.1 E-7
• BRAM	1.2	1.6 E-7
• Routing bits	1.2	8.0 E-8

- **Dynamic upsets were observed**
  - **Transient or combinatorial logic upsets observed - adds to cross-section**
  - **Routing bit upsets recorded (8 or more) but did not contribute to functional upset - subtracts from cross-section**

- **Upset in configuration control logic register observed**
  - **Observed threshold LET between 8 and 16 MeV-cm^2/mg**
  - **Small device cross-section measured at 1 E-5 cm^2 for this mode**
  - **Small probability of occurrence based on measured cross-section**

On-Orbit SEU Detection and Mitigation

- **GEO orbit upset estimate = 4 E-6 upsets per bit day**

- **Detection and recovery of static bit upsets**
  - **Configuration readback feature allows for continuous monitoring for static bit upsets**
  - **Detection and repair is rapid**
  - **Partial reconfiguration capability allows for recovery without interruption of function**

- **Mitigation requires redundancy techniques**
  - **Some redundancy capability on-chip**
  - **Full redundancy requires multiple chip solution**

Thermal Reliability Considerations

- **High pin count packaging combined with high power dissipation results in significant reliability challenges in space**
- **FPGA packaging options include:**
  - **560 pin ceramic Column Grid Array (CGA)**
  - **560 pin plastic Ball Grid Array (BGA)**
- **Potential assembly wear-out due to thermal cycling (TCE mismatch)**
- **Heat dissipates via package top, not the PC board contact**
- **Power dissipation is application dependent up to 7 watts per part**

Summary

- **ZBT SRAMs are TID tolerant but SEL sensitive**
- ***Virtex* FPGAs are SEL immune and TID tolerant**
- **Frequency of upsets can be tolerated with a combination of detection & recovery and system level mitigation**
- **The performance of the *Virtex* FPGA makes it an good candidate for remote sensing applications and allows for reconfigurability on orbit**
- **Thermal considerations are key to long term reliability**