

## 1999 MAPLD Conference

# SEU Mitigation Techniques for Virtex FPGAs in Space Applications

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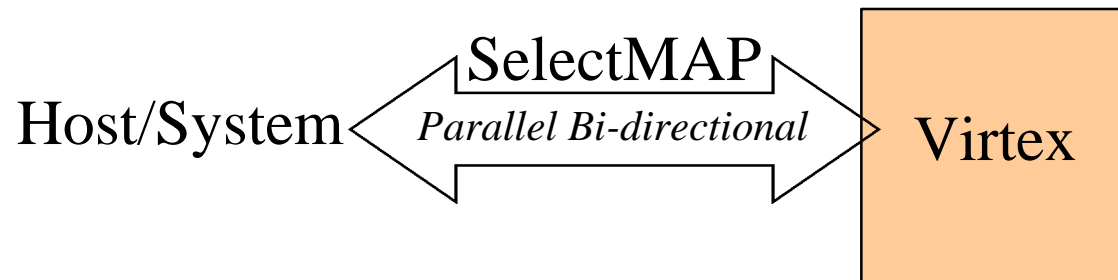
# Radiation Tolerant Virtex FPGAs

- ◆ Re-configurable Logic Devices
  - Remote Hardware Changes and Functional Evolution.
  - Fast SEU Detection and Correction
  
- ◆ SEU Protection Design Techniques
  - SEU Detection and Correction
    - Full design verification in 20ms
    - SEU correction in 3 $\mu$ s without functional interrupt
  - SEU Mitigation
    - SEU Resistant Mitigation Circuit
    - Module and Logic Node Redundancy and Mitigation
    - Logic Partitioning for Mitigation
    - Dual and Triple Device Redundancy and Mitigation

# Rapid SEU Detection and Correction



## Advanced Configuration Interface



- ◆ SelectMAP Configuration Interface
  - 400Mbit/s transfer rate
  - 8 bit bi-directional synchronous bus
  - Non-interfering
  - Partial Re-configuration

# SEU Detection in Virtex

- ◆ Readback and Verify Configuration Data
  - Read entire memory contents
  - Byte for Byte comparison.
  - Count number of frames to upset.
  
- ◆ Readback Verification Cycles (Full)
  - XQVR1000: 6.27Mbits => 15.7ms
  - XQVR300: 1.7Mbits => 4.25ms

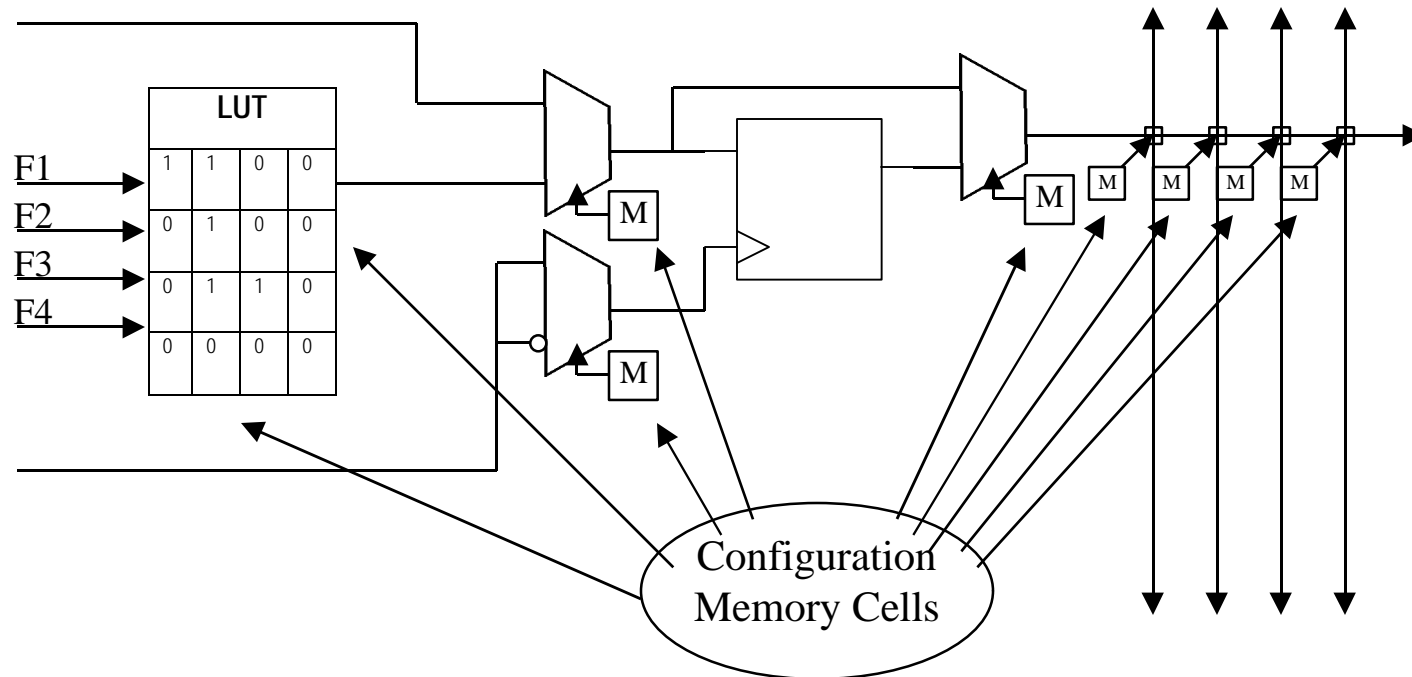
# SEU Correction

- ◆ Re-configuration (Traditional FPGAs)
  - Repairs all static upsets
  - Momentary loss of service
- ◆ Partial Configuration (Virtex only)
  - Repair single upsets in individual Frames
  - No loss of service
  - No functional disruptions
- ◆ Partial Configuration Cycles (Single Frame)
  - XQVR1000 (frame=1248 bits) => 3.1μs



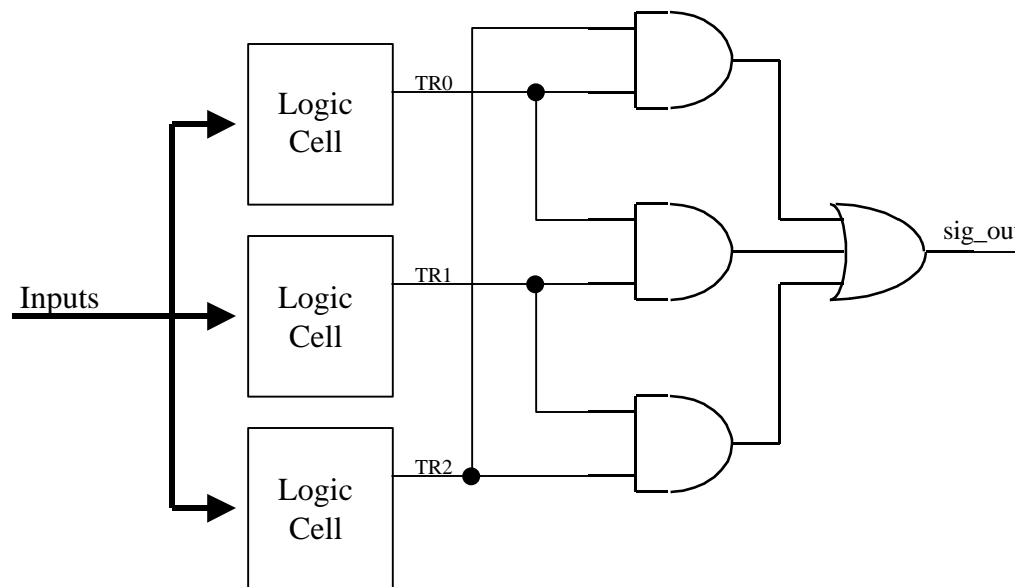
# Single Event Upsets in Static RAM Based Programmable Logic Devices

- ◆ Design functionality is defined by configuration SRAM contents.
- ◆ Single Event Upset may alter design functionality.
- ◆ Transient upsets may induce undesired logical conditions.



# Traditional SEU Mitigation with Triple Module Redundancy and Voter Circuit

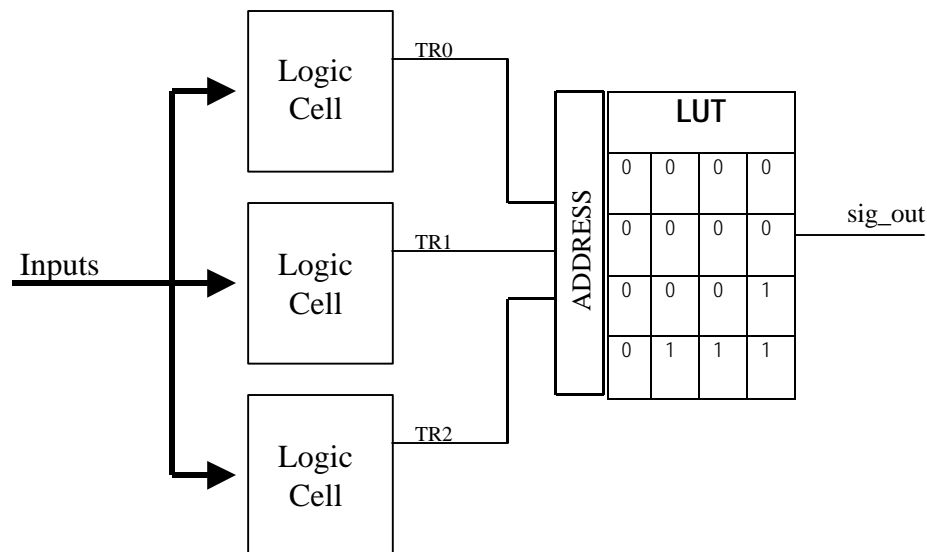
- ◆ Single Event Errors are mitigated through a majority vote circuit.
- ◆ A majority vote circuit requires multiple upsets for a logical error to occur.
- ◆ Assumes that voter circuit itself will not upset.



SEU Mitigation Truth Table			
TR0	TR1	TR2	sig_out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

# SEU Mitigation Voter circuit in Traditional SRAM FPGAs

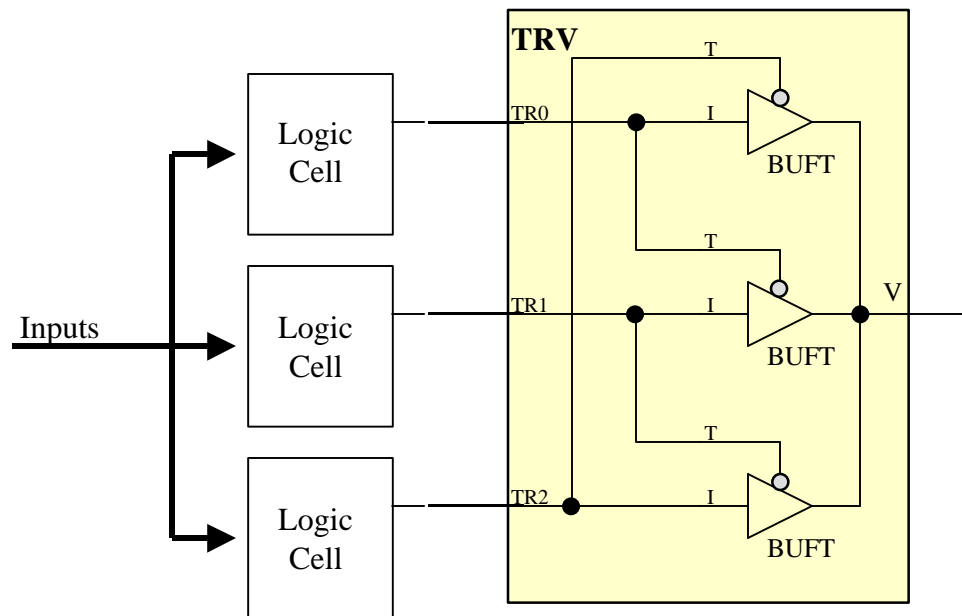
- ◆ Voter implemented in LUT.
- ◆ Susceptible to Single Event Upsets.



SEU Mitigation Truth Table			
TR0	TR1	TR2	sig_out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

# Creating a “Voter” in Virtex using BUFTs

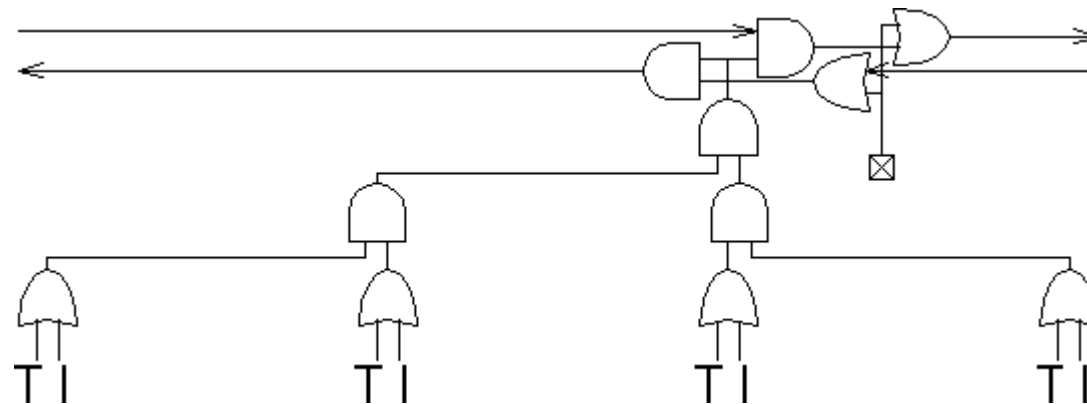
- ◆ Instantiate BUFTs in design as shown.
- ◆ Circuit is SEU immune.
- ◆ Doesn't use any CLB (Logic) resources.
- ◆ Abundant and free.



TR0	TR1	TR2	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

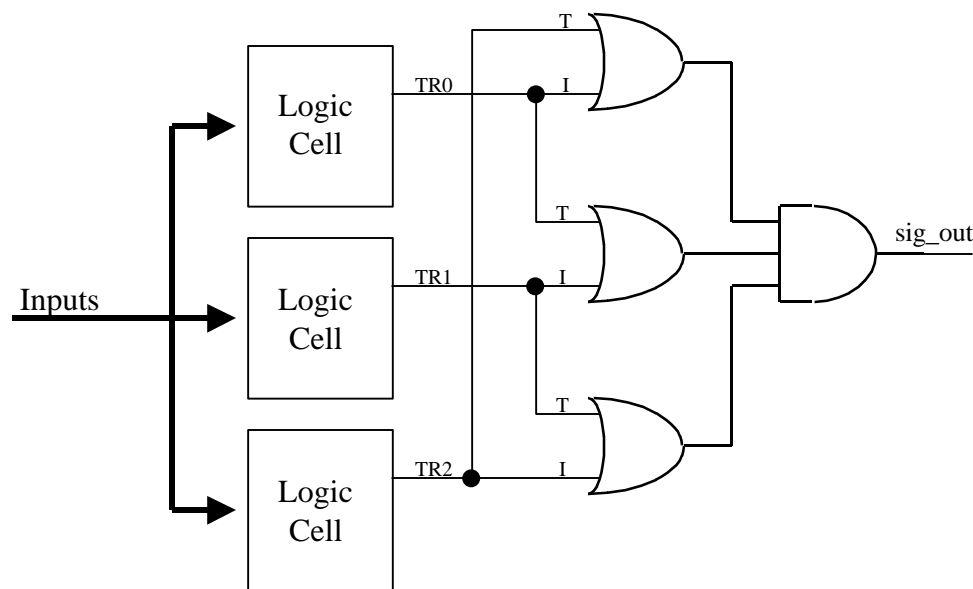
## SEU Mitigation with Virtex BUFTs

- ◆ Virtex BUFTs are hard-wired OR-AND Gates, not LUTs.
- ◆ Segmented into groups of four BUFTs.
- ◆ Functionality is not dependent on configuration memory cells.
- ◆ Configuration cells only used for routing pips.
- ◆ Two BUFTs per CLB.
- ◆ Four Bus channels per CLB row.



# Voter Function with OR-AND Structure

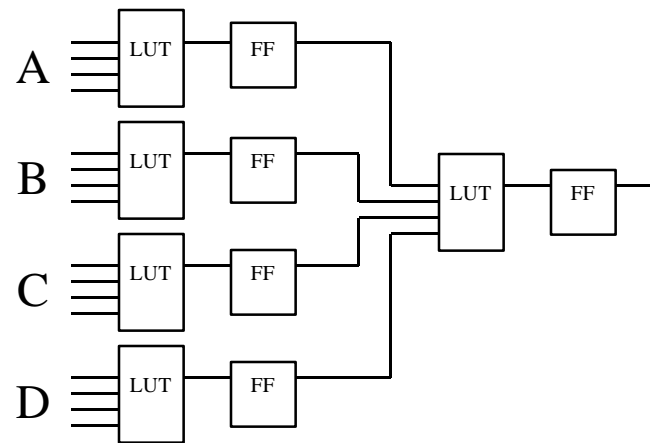
- ◆ Same Boolean function as AND-OR structure



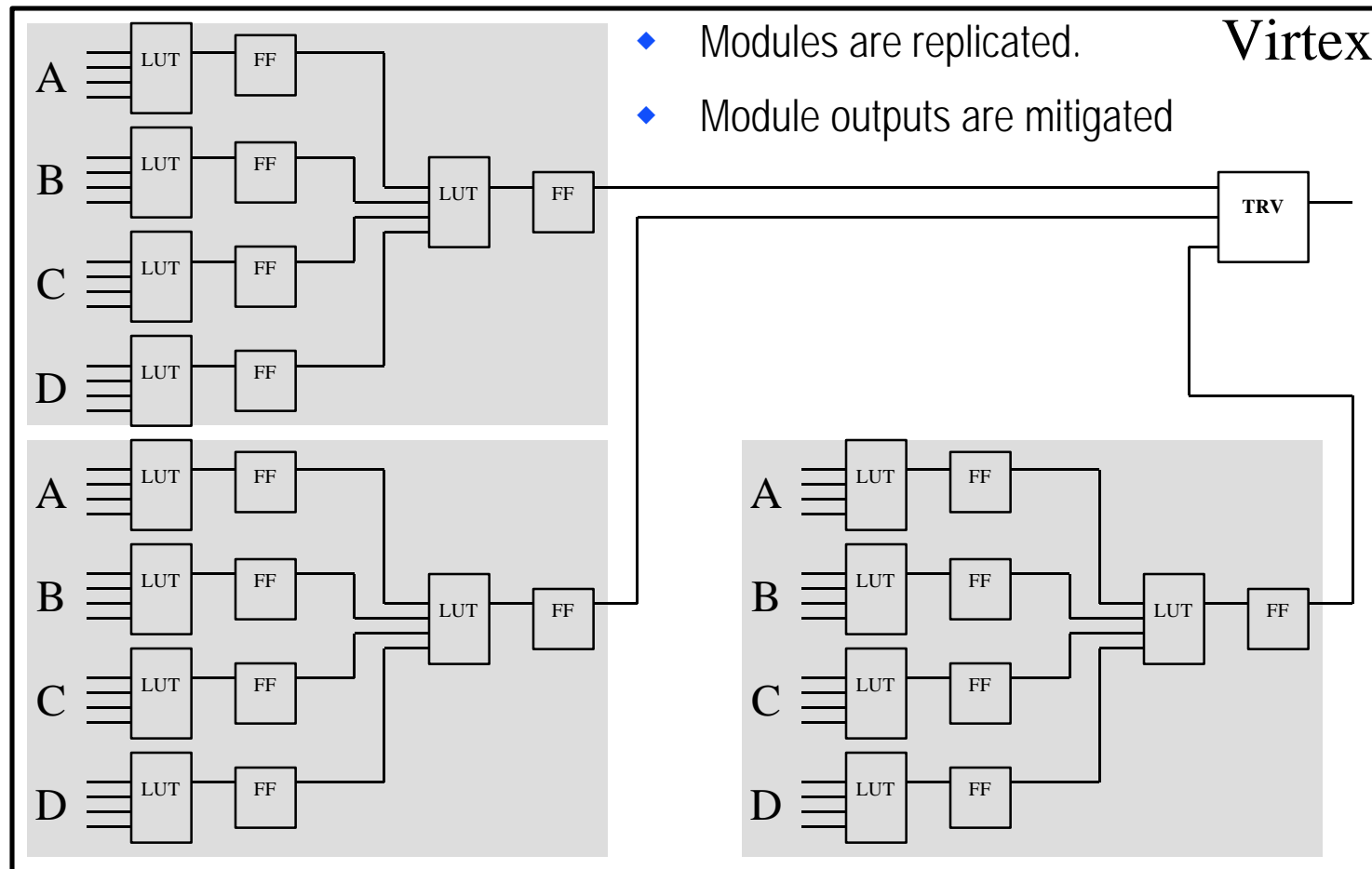
SEU Mitigation Truth Table			
TR0	TR1	TR2	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

# Simple Logic Module

- ◆ Combinations of 4-input boolean functions to implement any logic equation.
- ◆ Pipelined register stages are a typical performance enhancement.
- ◆ LUTs and FFs are susceptible to SEUs.
- ◆ Interconnect is susceptible to transient upsets.



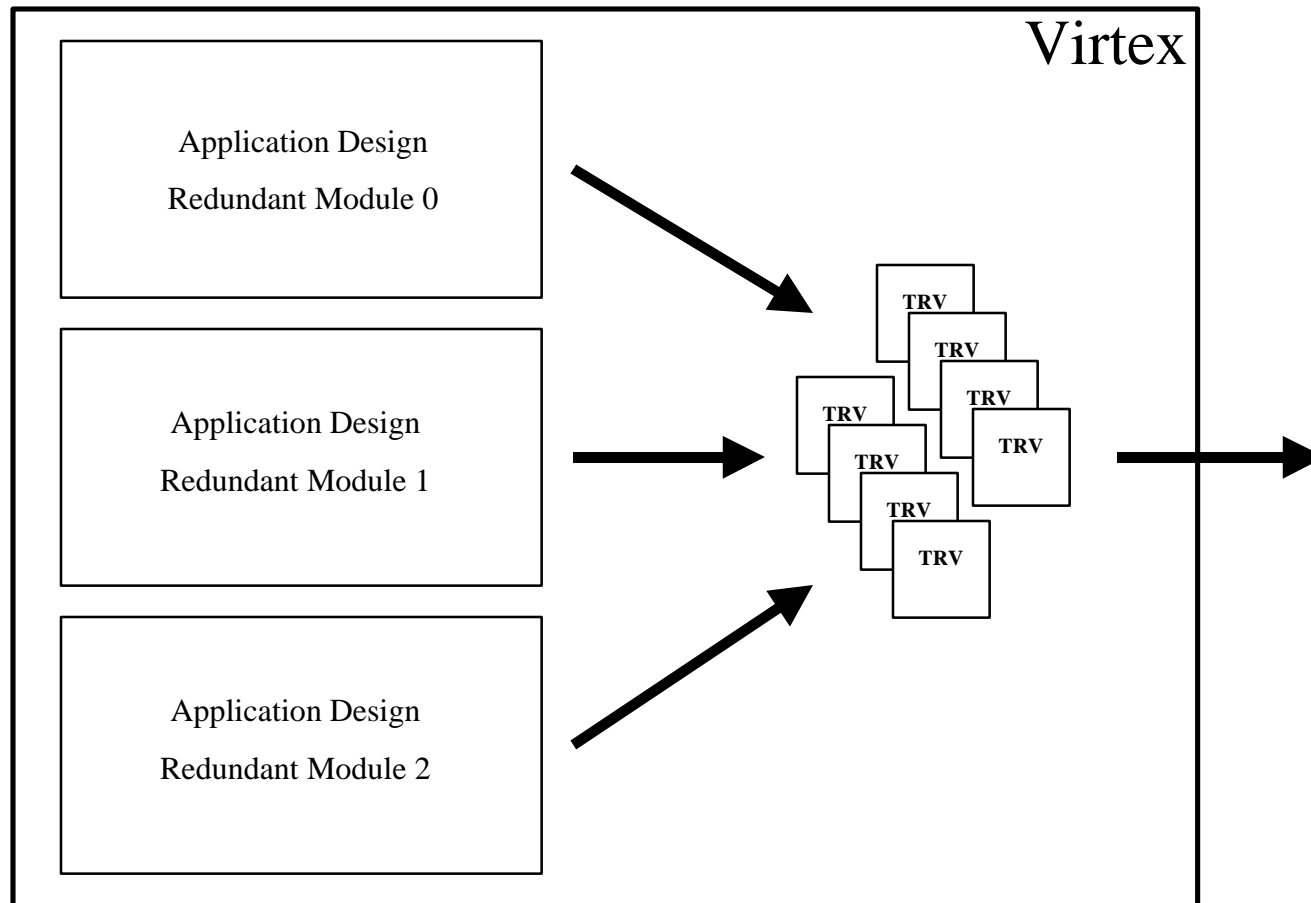
# Module Redundancy and Mitigation



# Single Chip Redundancy and Mitigation

- ◆ Single application <30% device resources.
- ◆ V300 design implemented with full mitigation in one V1000.
- ◆ Highly Resistant to SEUs.
- ◆ Some SEFI susceptibility.

# Module Redundancy and Mitigation on a Single Chip



# Single Event Functional Interrupts



- ◆ Power On Reset (POR) Upset
  - 4 susceptible cells out of 6.27M (V1000)
  - Upset Re-Initializes FPGA memory
  - Observed at fluence above  $10^5$  ions/cm<sup>2</sup>
  
- ◆ Probabilities of Upset to POR
  - 1 chance out of 3 million per ion per cm<sup>2</sup>
  - LEO: 1 static upset per hour.
    - One POR upset per 85.6 years

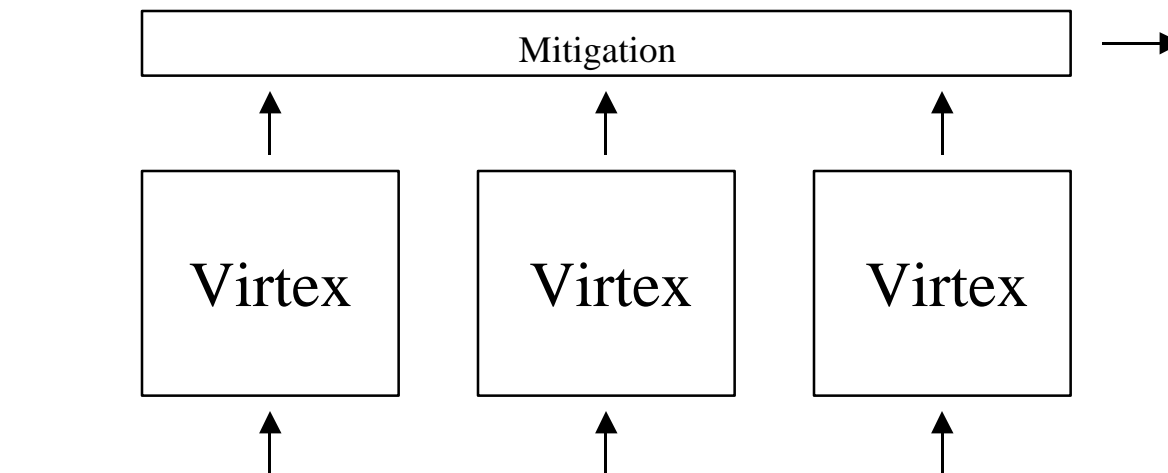
# Single Event Functional Interrupts



- ◆ Boundary-Scan (JTAG) TAP Controller
  - 4-bit Binary encoded state-machine
  - Upset can jump TAP to Update-IR
  - 1 out of 13 Million chance per ion per  $\text{cm}^2$
  - EXTEST turns I/Os into active outputs
  - LEO (1 upset/hour): 1 upset per >700 years
- ◆ Preventative Measures & Recovery
  - Load IR with ones <11111> (ByPass)
  - Hold TMS High and clock TCK continuously
  - 5 cycle (max) @ 33MHz => 150ns recovery

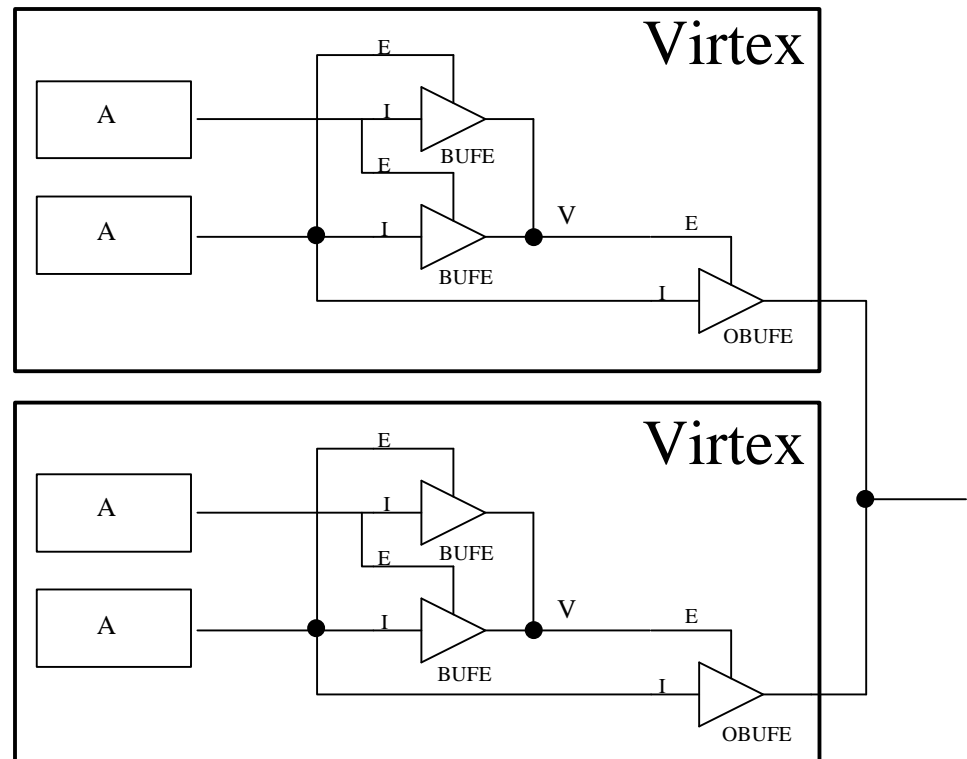
# Triple Module Redundancy

- ◆ Most reliable safeguard for total device failure.
- ◆ Requires external mitigation device.
- ◆ Combined with internal mitigation and rapid detection and correction, SEU immunity is comparable to any in-orbit device.



# Dual Voting Double Redundancy

- ◆ Reliable safeguard against total device failure.
- ◆ Operates without external mitigation device.
- ◆ No single point susceptibility.
- ◆ Independent I/O mitigation.



# Summary of Features

- ◆ SEU Immune
  - SEU Detection, Correction and Mitigation
- ◆ SEFI Immune
  - Device Redundancy
- ◆ SEL (Latch-Up) Immunity
- ◆ Re-Programmable Capabilities
  - Last minute changes
  - Post-Launch hardware flexibility