Field Programmable Mixed Signal Arrays for Space Applications

(open,unclassified presentation)

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Introduction

The ability to use a radiation-tolerant programmable digital logic part in hardware intended for high reliability missions can provide significant cost savings. The savings result from shorter design cycles and lower risk, but mostly from reduced parts acquisition and qualification costs. Without these parts, many projects would be unable to afford custom gate array implementations, and would be forced to resort to discrete designs with the accompanying increase of system size, mass, and power consumption.

A similar situation exists in the mixed-signal field today. Almost all spacecraft and military systems contain numerous circuits that require moderate-performance analog and digital processing and I/O. These circuits are widely distributed throughout the system hardware, used for applications such as status monitoring, motor and temperature control, and signal conditioning and processing. This is illustrated in Figure 1, which is a simplified block diagram of a scientific satellite that has been annotated to indicate where such circuitry is typically used.

Until now, these mixed-signal circuits have been implemented almost exclusively using discrete parts, because the cost savings are not significant enough to justify a custom ASIC design. However, the resources used by such circuits, including mass, power, and volume, add up very quickly. The ability to implement such designs using a general-purpose, programmable mixed-signal array (FPMA) would be very welcome. The advantages of using an FPMA would be similar to those of an FPGA, namely much lower parts acquisition and qualification costs, higher levels of integration, lower power, and fast turn-around design cycles. It would also provide an improvement in overall reliability.

The Space Department of the Applied Physics Laboratory, with funding from NASA's Advanced Technology Development program, is engaged in a development effort that will culminate in commercially available FPMA parts of benefit to the entire space community. This paper provides an overview of the FPMA development program as well as a simulated application example.

Development Plan

Figure 2 lists our development steps, and indicates our progress to date. The selection of the FPMA architecture is intimately involved with commercial partnering and access to technology. We have already established a commercial partnership with Actel Corporation and selected an FPMA architecture based on anti-fuse technology.

In addition we have completed the design of a small test chip hosting a 4 by 3 array of programmable analog modules, the associated programming circuitry, and test structures. If all goes well we will begin testing first silicon in the December 1999 time frame.

Although it is still relatively early in the development process (step 6 in Figure 2), we are optimistic that we can realize our goal of getting the FPMA technology into the space community on a “commercial” development schedule. Some iteration may be necessary, so while the test chip is being fabricated, we will proceed with the development of programming hardware and software to aid in testing the prototypes.

FPMA Architecture

Field programmable analog arrays are not a very new idea, and various architectures have been investigated [1]. The architecture of an FPMA is largely determined by the type of programmable interconnection technology, and the configuration storage technology. Most digital CMOS processes are limited to MOS switches for the programmable interconnect, and volatile SRAM configuration storage, although EPROM and EEPROM are sometimes available for nonvolatile configuration staorage. FPMA architectures based on MOS switches are naturally suited to implementing switched capacitor [2], or switched current [3] analog circuits.

Anti-fuse interconnection technology provides an exciting alternative to MOS/SRAM based architectures. An anti-fuse provides a low resistance programmable connection and nonvolatile configuration storage in a structure the size of a via. An FPMA architecture based on anti-fuses can implement continuous time analog circuits, as well as discrete time circuits (since MOS switches can still be implemented where needed). The programmable analog modules can be much more area efficient, because anti-fuses occupy much less area than a MOS switch. In addition, the anti-fuse has a lower interconnect resistance and no extra configuration storage circuitry is required.

We have chosen to pursue the anti-fuse based FPMA strategy by entering into a partnership with Actel Corporation, a recognized leader in anti-fuse technology, as well as the dominant supplier of radiation tolerant FPGAs suitable for space applications. Actel provides our development effort with access to a radiation tolerant CMOS process with anti-fuse interconnect. Moreover, having Actel as a commercial partner provides a vehicle for making FPMA technolgy widely available to the space electronics community as a standard product which is compatible with digital FPGAs.

Our present FPMA architecture adds an array of analog modules (AMODs) to a standard FPGA as shown in Figure 3. All digital functions are implemented in the digital array, and analog functions are implemented in the analog array. Some special analog I/O cells will also be added to provide buffered outputs, voltage references, and so forth.This architecture provides for a common programming interface compatible with digital FPGAs, so that the FPMA “looks like” an FPGA with some extra AMOD resources and some special analog buffers (AinBufs AoutBufs and RefBufs).

The AMOD architecture is based on a fully differential opamp with associated MOS capacitor and poly resistor arrays, as well as some MOS analog switches for implementing switched circuits. One difficulty with the digital FPGA process is the lack of a linear capacitor option; however, we are employing special design techniques to work with accumulation mode MOS capacitors[4]. The detailed architecture is discussed in more detail in reference 5. A high level schematic is shown in Figure 4, which actually depicts a stack of three AMODs to illustrate local and global interconnection schemes in the present prototype.

In the next section we present an application example where a particle instrument shaping chain is implemented with 4 AMODS.

Application Example

As previously mentioned, we have designed a test chip which hosts a 4 by 3 array of AMODs. During the design process we created a particle instrument shaping chain example as a test case for evaluating the analog performance of the AMOD. The AMOD opamp is designed to have a DC gain of around 60dB, a unity gain frequency of 20MHz, and be unity gain stable (with a phase margin of at least 70 degrees when driving a typical on-chip load of 1pF). Figure 5 is a schematic of a fully differential implementation of a shaping chain including a singel-ended to differential differentiator stage (which would take as its input the singel-ended output of a charge sensitive preamplifier), followed by two fully differential integrator stages, and a differential to single-ended integrator which produces the shaping chain output pulse.

The AMOD opamp and capacitor layout was extracted (including parasitics) and used as a subcircuit to implement the 4 stages in Figure 5. A transient analysis was performed with SPICE, and the output waveforms are shown in Figure 6. A useable shaping chain is predicted, although we will need to investigate the temperature dependence of the shaping time constants.

Summary

We believe that our FPMA program is an exciting technological development which will benefit both the commercial and government space programs. The multi-year funding by NASA and the up-front commercial participation by Actel Corporation give this effort an excellent chance producing a real product that is available to the whole space community in the near future.

References

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Figure 2. FPMAA Development Plan

1. Select viable interconnect technology (anti-fuse).
2. Establish commercial partnership.
3. Study target applications.
4. Develop an analog module architecture and specifications
5. Simulate applications to ensure viability
6. Design and fabricate test chip * (we are here)
7. Design analog I/O cells *
8. Conduct performance, environmental and radiation testing *
9. Develop software tools and programming infrastructure.
10. Support commercialization of FPMA products

* Indicates iterative processes

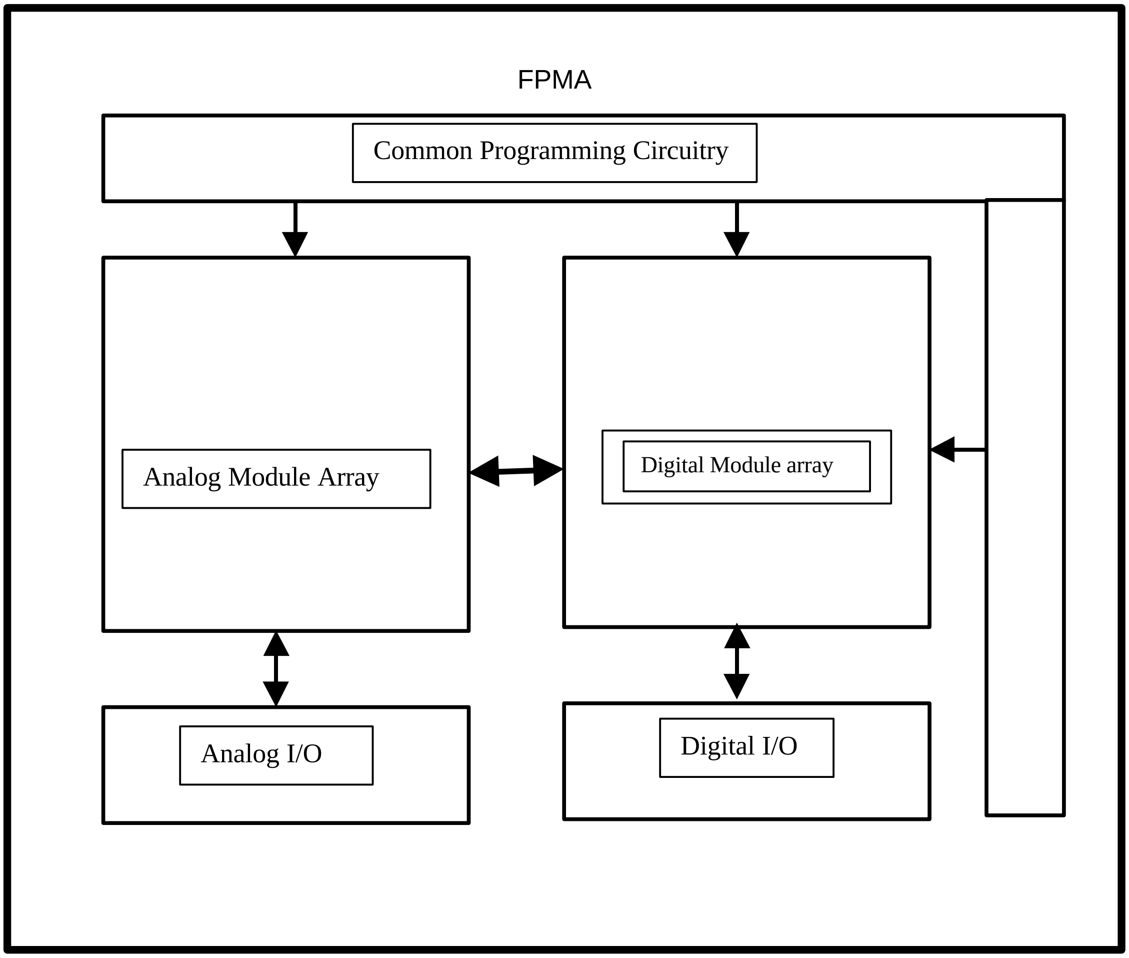

Figure 3. Anti-fuse FPMA architecture.

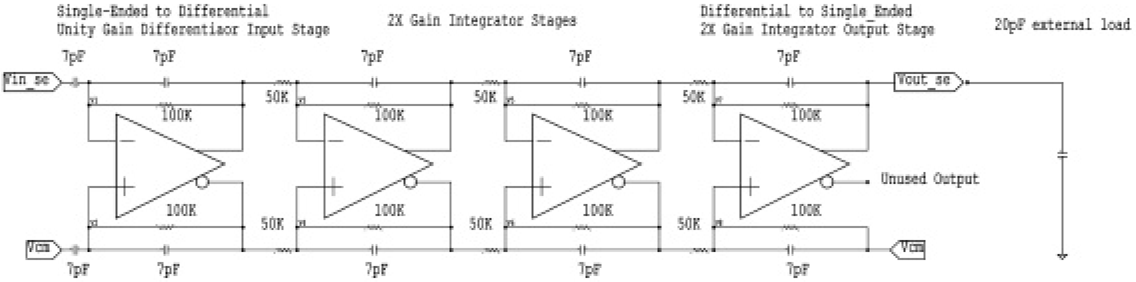

Figure 5. FPMA Particle Instrument Shaping Chain Example