

Application Examples: How to Use FPGA's In Satellite Systems

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1.0 ABSTRACT

Field-Programmable-Gate-Arrays(FPGA) are used to provide simple and complex digital logic functions. However, when the FPGA is used in a product in a Radiation Environment (e.g. Satellite), there are additional factors, which must be considered.

1.1 KEYWORDS

FPGA, Satellite, Aerospace

2.0 INTRODUCTION

Field-Programmable-Gate-Arrays (FPGA) are commonly used in products which exist in radiation environments (e.g. Satellites, Avionics, etc). The FPGA's are very attractive since they provide a large number of logic gates (high-density) of logic in very small physical spaces (size and weight). Generally, all standard digital design practices taught in the Universities and used in standard commercial environment products, can be applied to the FPGA's used in the products destined to exist in the radiation environment. However, when an FPGA is design-into a product which must exist in a radiation environment, there are additional factors which must be considered. These additional factors are application dependent, and are not obvious.

This paper will show a few digital logic applications, and highlight the additional factors that must be considered by each circuit. Once these factors are realized and accounted for, the FPGA can be reliably used in products, which will exist in a radiation environment.

2.1 RADIATION CONSIDERATIONS FOR EVERY APPLICATION

When an FPGA (or any electronics circuit) is used in a product, which will exist in a radiation environment, the effects of radiation must be considered and accounted for. At the digital logic design level, the effects of radiation must be accounted for in two main areas, referred to as "factors" above. These two categories of radiation effects are listed below.

1) FIRST ORDER EFFECTS:

First order effects are the effects that the radiation will directly have on the FPGA components themselves.

2) SECOND ORDER EFFECTS:

Second order effects are the effects that the "other" non-FPGA circuits place back onto the FPGA, as a result of the effects that the radiation has on the non-FPGA circuits.

2.2 RADIATION TYPE and CATEGORY

Although this paper refers to "radiation" generically, it should be noted that there are multiple types and quantities of radiation, and these are unique to each physical environment. In other words, an Airplane (in an Avionics environment at 60,000 feet) will be irradiated by a totally different type and quantity of radiation than a Satellite (in a Low-Earth-Orbit).

Since the FPGA designer is typically a digital logic designer, and the phenomena of radiation is very complex, Actel recommends seeking the advice of a qualified space radiation effects engineer to understand how radiation will effect the FPGA and the surrounding circuitry in your specific application.

3.0 APPLICATION EXAMPLES

In this section, two digital logic applications will be shown. These two applications demonstrate that there are additional factors, which must be considered in each application. Since each circuit is different, the additional factors of how radiation affects each specific circuit are different, and these factors will be highlighted and addressed.

The first example (Application Example#1) shows how to use an FPGA to drive a heavy load, using external circuitry. The radiation effects on this overall circuit are discussed, and also the effects by that the external circuitry places back onto the FPGA.

The second example (Application Example#2) shows how to use FPGA's in circuits that require redundancy. Redundancy can increase the reliability and life of a product, since it can effectively have a second identical redundant (or backup) circuit to continue operation if the first circuit is not functioning properly, eliminating a fault due to a single point of failure.

3.1 APPLICATION EXAMPLE# 1: DRIVING A HEAVY LOAD

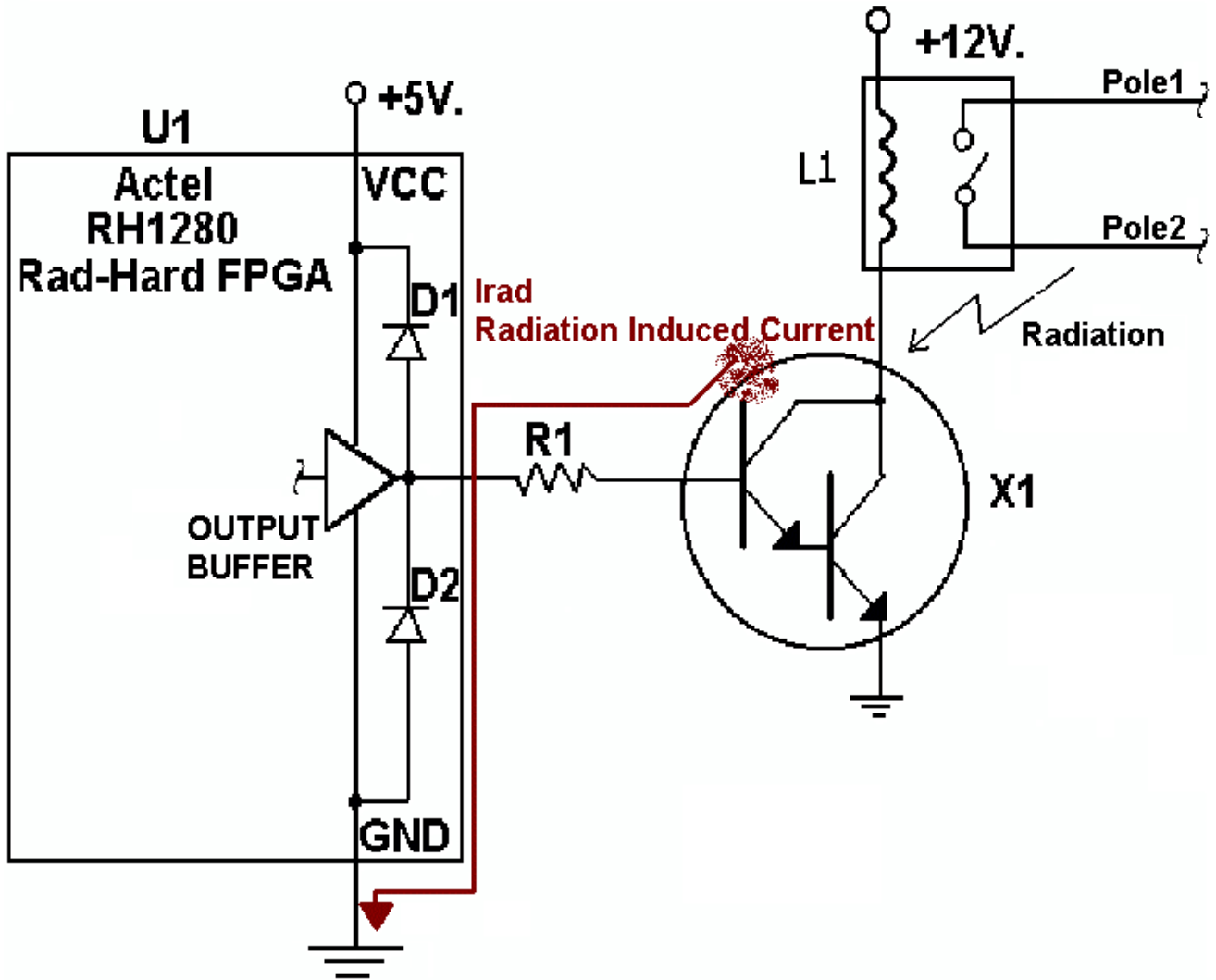
Field-Programmable-Gate-Arrays have a very large number of gate (high-density) of logic gates internal to the FPGA. In order to access the FPGA's internal logic gates, signals are input into the FPGA, and signals are output out of the FPGA. Since FPGA's are digital logic devices, they interface to external logic devices with standard TTL or CMOS logic levels. The FPGA can interface directly to external digital logic devices, such as Microprocessors, Memory devices, Peripherals, and various other TTL and CMOS logic devices. When the FPGA has to drive an external device/load that has a voltage or current requirement outside of the rated specifications of the FPGA's TTL or CMOS output drive capability, additional circuitry is required to drive this heavier load.

Since satellite systems commonly use relays for their ability to provide a single switch function, with no electrical coupling between one circuit (call it circuit#1) which is controlling a relays coil and the circuit receiving the relays contacts (call it circuit#2), and because of their inherent radiation tolerance. Relays are used for many functions on a satellite.

3.1.1 CIRCUITRY FOR DRIVING THE LOAD:

Although there are a variety of relay types, satellites typically use the mechanical dry-contact style. The mechanical dry-contact relay has some inherent radiation tolerance. It has 2 sections: A relay which controls the state of the relay outputs and the output contacts themselves. Since most relays do not typically have coils which can be driven by an FPGA's TTL/CMOS digital output signal, special circuitry is required. A very common and generally accepted method to interface a digital logic device (like the Actel FPGA) to a heavy load (like a relay coil) is to use a Darlington transistor. A circuit diagram (in black color) is shown below.

FIGURE 1



In general, this circuit has two states, and these two states are listed below in TABLE 1.

TABLE 1

FPGA OUTPUT LEVEL	State of X1	State of L1	State
Logic "0"	Off	Off	Oper
Logic "1"	On	On	Clos

3.1.2 SPECIAL CONSIDERATIONS DUE TO RADIATION EFFECTS:

Although the circuit shown in Figure 1 is a very common and generally used design technique to increase the drive strength of the FPGA, when this circuit is used in a product destined to be in a radiation environment, all of the potential effects of radiation must be considered. As described in section 2.1, we need to check the First and Second order effects that radiation can have on the FPGA, labeled U1 in Figure 1.

The first order effects in this example are such that the FPGA's inherent radiation tolerance is greater than the radiation that will irradiate the FPGA component.

The second order effects in this example are checked by considering how the external circuitry: resistor R1, transistor X1, and relay coil L1 can effect the FPGA, when R1, X1, and L1 are irradiated. In this example, a problem has been found. To

be more specific, when the external transistor, labeled X1 in Figure 1 receives radiation, it will generate radiation-induced currents to flow (labeled “Irad” in Figure 1). This radiation-induced current can flow back into the FPGA’s transistors (inside of the FPGA’s output buffer), and can flow back into the FPGA’s clamping diodes (labeled D1 and D2 in Figure 1). If this current exceed the FPGA’s maximum allowed clamp diode current, the FPGA could be damaged.

In summary, this example has shown that although the radiation did not damage the FPGA directly, the radiation did cause a current to flow in an external component, and this very current in turn could damage the FPGA. This is a “special factor” that must be realized when using this circuit.

3.2 APPLICATION EXAMPLE# 2: INTERFACING REDUNDANT CIRCUITS

Since Satellite systems are expensive and not economically serviceable, their design goals include the requirement for a very high level of reliability. This reliability not only implies using highly reliable components, but also implies that the circuit design techniques must be highly reliable. One circuit design technique that provides an increase in reliability is for the satellite to include redundant circuitry.

3.2.1 REDUNDANT CIRCUIT BENEFITS

Redundant circuitry can refer to various design techniques: a) redundant logic designed into in a single component, or b) using redundant components that contain the identical logic design. Each of these techniques provides its own advantages and disadvantages. The advantage of using redundant components (technique b) is: the system can be made immune from a single point of failure. In this case, two (2) identical FPGA’s will exist on a single satellite, so that if one FPGA goes bad, the other FPGA can be used instead, so that the satellite will continue operation. The disadvantage of using redundant components (technique b) are: the component cost is higher (buying 2 FPGA’s), and the total weight of the components is higher (using 2 FPGA’s). Since reliability on a satellite is paramount above all other concerns, using redundant components that contain the identical logic design is the design technique that is discussed below.

3.2.2 REDUNDANCY BY USING DUPLICATE COMPONENTS

Since a satellite that was designed required a very high degree of reliability, it used the design technique of using redundant components. This technique requires all of the following items to be solved.

First, the FPGA component itself must be able to withstand the incoming radiation. A qualified space radiation effects engineer should select the Actel FPGA that can tolerate the radiation.

Second, the circuit designer has to ensure that redundant FPGA’s can work together correctly. Since there are two FPGA’s, there are two power sources that have to be applied. There are four possible combinations of power being applied, and two major modes of operation. Mode#1 only has the power applied to the FPGA being used (not the inactive circuit too), whereas Mode#2 has power applied to both the primary and secondary FPGA at all times. The two major modes are listed in Table #1 below.

TABLE#1

Mode of Operation	Circuit With Power Applied		Circuit Being Used	
	Circuit#1	Circuit#2	Circuit#1	Circuit #2
Mode #1-Primary	X		X	
Mode #1-Backup		X		X
Mode #2-Primary	X	X	X	
Mode #2-Backup	X	X		X

Since satellites have limited capacity power sources (typically batteries), it is desirable for every circuit to reduce its power-consumption. Because of this, it is obvious that “Mode#1-Primary” and “Mode#1-Backup” listed in Table #1 are the desired modes of operation, since only one circuit needs to be powered up during operation (rather than supplying

additional and un-necessary power to the backup circuit not in use). In “Mode#1-Primary”, only Circuit #1 containing FPGA#1 has power applied to it. In “Mode#1-Backup”, only Circuit #2 containing FPGA#2 has power applied to it.

3.2.3 USING FPGA’s IN REDUNDANT CIRCUITS: SHARING IO’s

All Actel FPGA’s have some form of input protection diodes on all Input/Output (IO) pins. In a normal application, the voltages of the signals that are input into the FPGA’s input pins should be limited to $VCC+0.3v$ and $GND-0.3v$ (as specified in the “Electrical Specifications” section of each FPGA’s datasheet). However, if the voltage of the signals input into the FPGA exceeds $VCC+0.5v$ or $GND-0.5v$, the FPGA’s input protection diodes will protect its internal circuitry by clamping the input voltages present on the IO pins to remain within 0.5 volts of the FPGA’s power supply pins ($V_{diodeforward}=0.5v$). When the input signals have excessive undershoot or overshoot, these protection diodes typically clamp these voltages to protect the FPGA. Although these diodes are generally helpful, they present a problem when the IO pins of redundant FPGA’s are to be connected directly together.

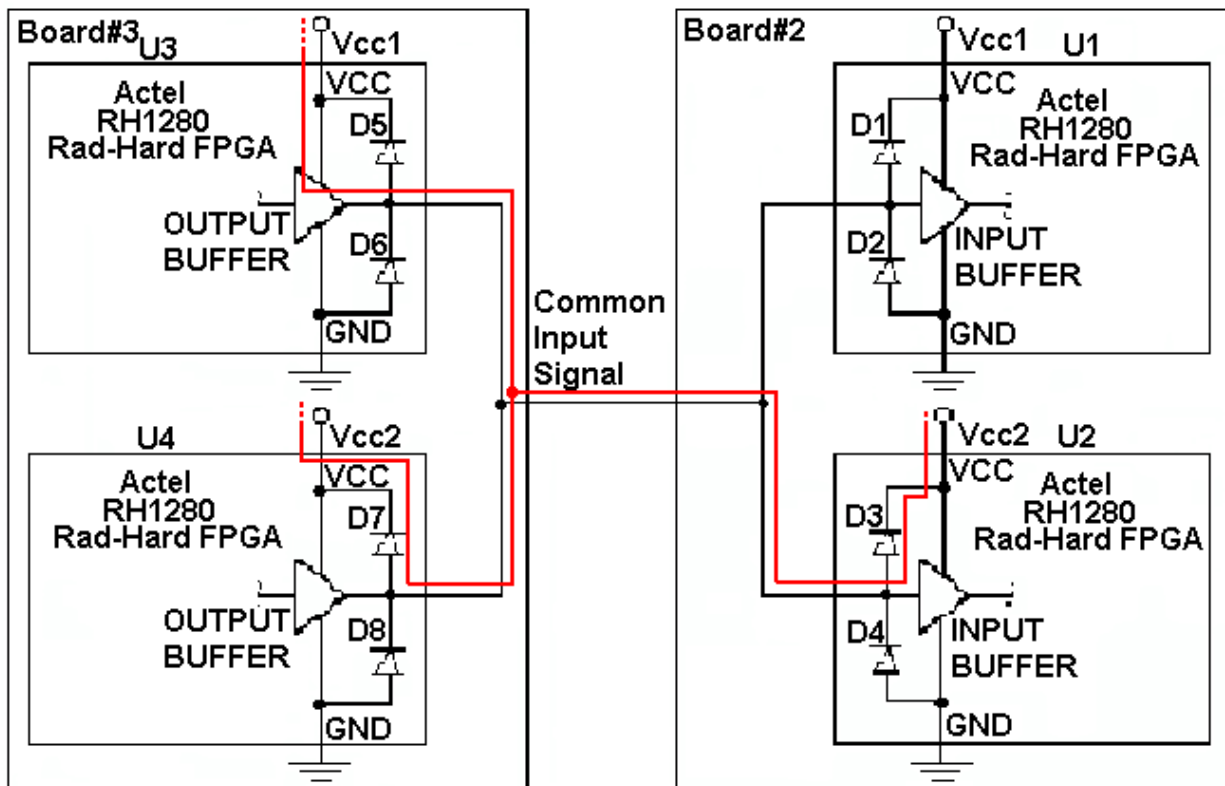
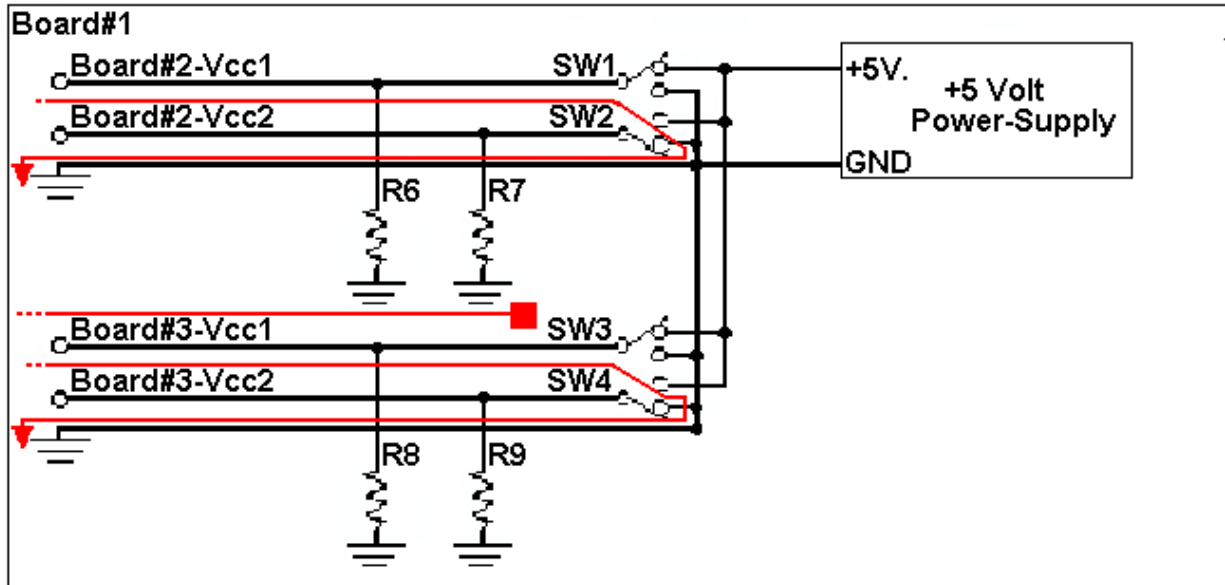
In order to accomplish redundancy, all signals have to connect to both of the redundant FPGA’s (example: U1 pin 1 is connected to U2 pin 1, U1 pin 2 is connected to U2 pin 2, and so on). As listed in Tabel#1 above (Mode#1), if one of the FPGA’s is powered-up (acting as primary at this point in time), and one of the FPGA’s is powered-down (either acting as backup FPGA or maybe shut-down if it has failed), the input protection diodes of the powered-down FPGA present a potential conflict. The potential conflict is that if a single input signal was connected to an input pin on two redundant FPGA’s, then the protection diode in the powered-down FPGA inadvertently could provide a shunt current path from the input signal to its VCC or GND. Therefore, this common input signal is invalid, since it can no longer maintain a valid TTL or CMOS voltage level to drive the input of the active (powered-up) FPGA. Furthermore, this diode may draw excessive current which may exceed the “Absolute Maximum Ratings”, and permanently damage the FPGA.

3.2.4 USING FPGA’s IN REDUNDANT CIRCUITS: EXAMPLE of PROBLEM

As an example, we will observe the diode effects when the common input signal to both FPGA’s is a logical “1” or high. This example uses 3 boards: Board#1 is the power-supply board, Board#3 outputs a signal, and Board#2 inputs this signal into redundant circuitry. The theory of this circuit is: Board#3’s FPGA outputs a signal to Board#2’s FPGA input. Board #1 and Board#2 will each only have 1 component powered-up at any point in time.

In this case, on Board#3, say U3 is the Primary FPGA and it is powered-up, and U4 is the Backup FPGA that is powered-down. On Board#2, U1 is the Primary FPGA and it is powered-up, and U2 is the Backup FPGA that is powered-down. In this case, when U3’s output is driving a logic “1” state onto the common input signal. This common input signal is input into Board#2, into both U1 and U2. In this circuit, we would like to have the “Common Input Signal” simply drive the input of U1 (the Primary FPGA) to be driven to a valid voltage level. However, since U2 is powered-down, and could have its VCC2 connected to GND in the powered-down state, we can see that protection diode D3 (inside powered down U2) will clamp the “Common input signal” such that in could never rise above the forward biased voltage drop of D3 (which is $GND+0.5V$). The current flow of this path is shown in the color red in FIGURE 2, below. [Since U4 on Board#3 is also powered-down, and could have its VCC2 connected to GND in the powered-down state, we can see that protection diode D7 (inside powered down U2) will also clamp the “Common input signal” such that in could never rise above the forward biased voltage drop of D7 (which is $GND+0.5V$). The current flow of this path is also shown in the color red in FIGURE 2, below]. Since $GND+0.5V$ is not a valid CMOS or TTL voltage level, the “common input signal” going to the powered FPGA cannot meet the minimum input voltage for a logic “1”. This is a “special factor” that must be realized when using this circuit.

FIGURE 2:



3.2.5 USING FPGA's IN REDUNDANT CIRCUITS: EXAMPLE of SOLUTION

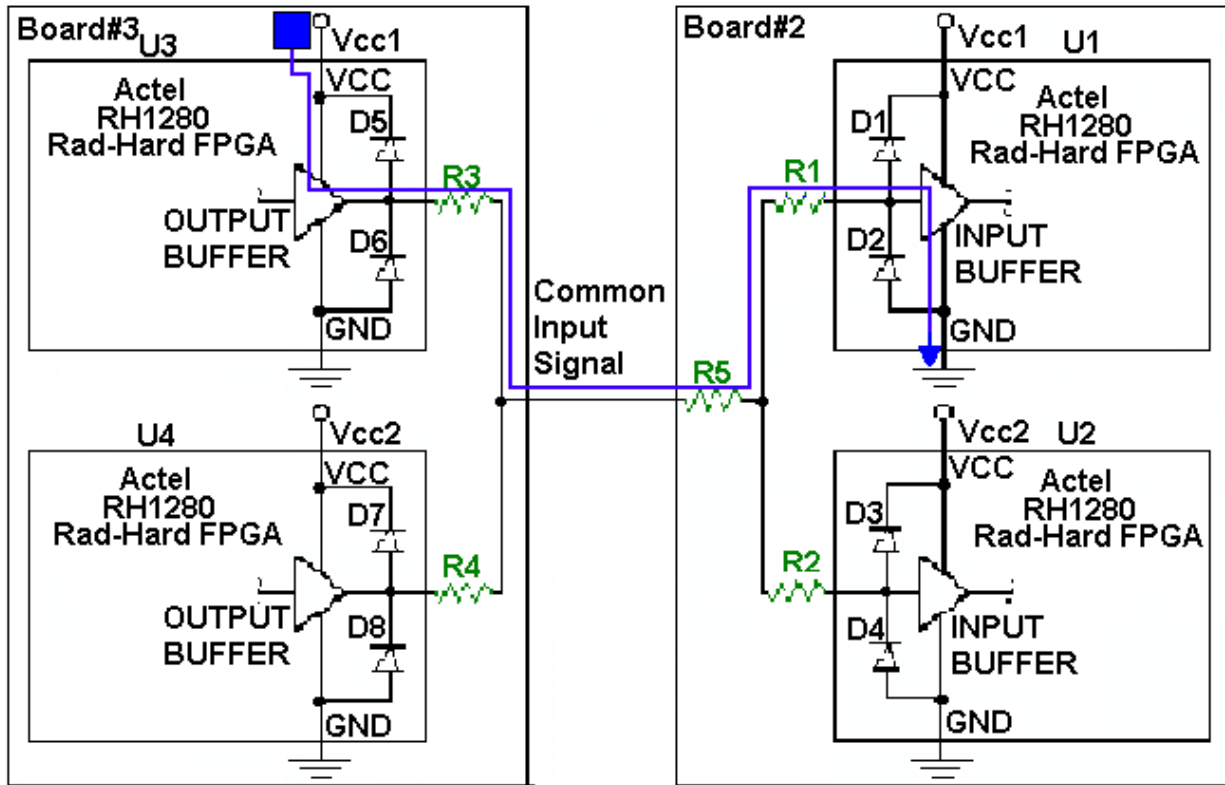
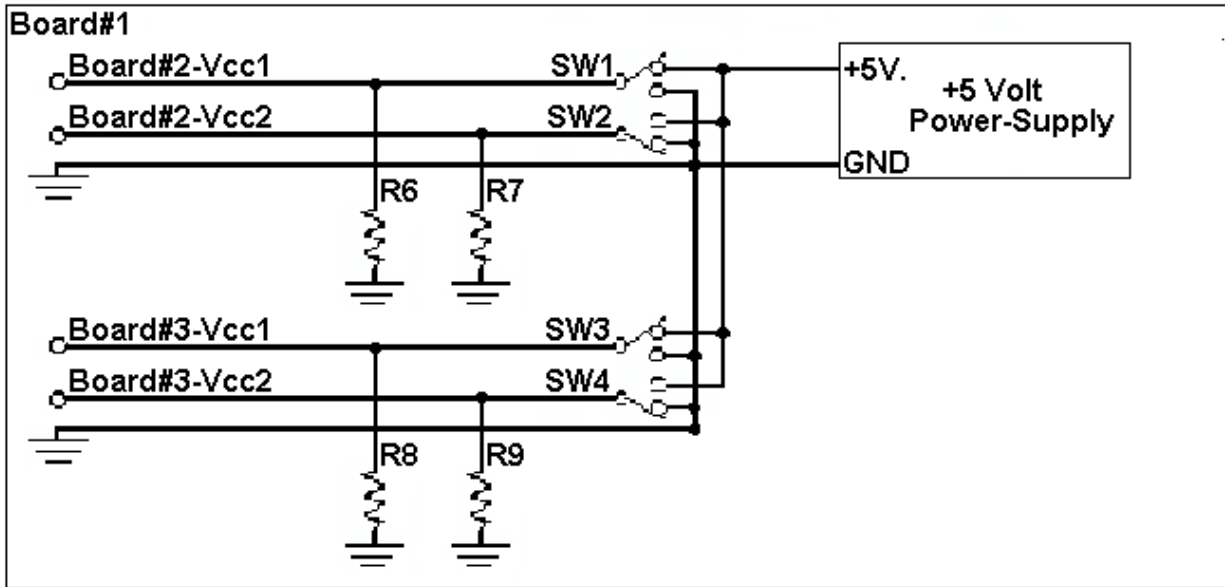
In order to use redundant FPGA components, the conflict discussed above needs to be solved. A solution to this conflict is to modify the original circuit by applying a special circuit, called "Resistive Cross Trapping", which consists of 4 or 5 inexpensive and physically small resistors. An example of this is shown in FIGURE 3.

The circuit in Figure3 is different from that in FIGURE2 due to the following reasons. The "common input signal" is connected to both of the redundant output FPGA's and input FPGA's through the "Resistive Cross Trapping" circuit. This circuit is described below.

- 1) On Board#3, U3's output FPGA passes through the series resistor R3 before it connects to "Common Input Signal". R3 prevents the voltage limiting diode effects of D5 from limiting U4's output voltage when its driving a logic "1".
- 2) On Board#3, U4's output FPGA passes through the series resistor R4 before it connects to "Common Input Signal". R4 prevents the voltage limiting diode effects of D7 from limiting U3's output voltage when its driving a logic "1".
- 3) On Board#2, the "Common Input Signal" passes through R5.
On Board#2, resistor R5 is optional. This additional series resistance can provide additional resistance to help select standard values of resistors for R1, R2, R3, and R4.
- 4) On Board#2, U1's input signal passes through a series resistor R1 before it connects to the "Common Input Signal". R1 prevents the voltage limiting diode effects of D1 from limiting U3 and U4's output voltage when either is driving a logic "1".
- 5) On Board#2, U2's input signal passes through a series resistor R2 before it connects to the "Common Input Signal". R2 prevents the voltage limiting diode effects of D3 from limiting U3 and U4's output voltage when either is driving a logic "1".

This circuit consists of 4 or 5 resistors (highlighted in Green color), which ensure that the primary (active and powered-up) FPGA will receive a valid signal, and that the backup (inactive and powered-down) FPGA will no invalidate the common input signal. The series resistors in the path accomplish this, by isolating the protection diodes clamping effect on the common input signal. The main current flow of the "common input signal" path is shown in the color blue in Figure 3, below.

FIGURE 3



APPENDIX A

The presence of protection diodes/clamping diodes on the IO pins of all Actel antifuse based FPGA's has been documented in the FIGURE A.1 below. (Since all of Actels antifuse technology FPGA's inherently have some level of radiation tolerance, and are used in Aerospace applications, all families have been included).

FIGURE A.1

FAMILY	PROTECTION DIODE^{1,2,3} with respect to GROUND	PROTECTION DIODE^{1,2,3} with respect to POWER
ACT1	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
ACT2	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
1200XL	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
3200DX	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
ACT3	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
ACT3BP	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
RH1020	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
RH1280	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCC"
SX	Yes, Parasitic clamping DIODE wrt "GND"	No, no clamping to any voltage exists.
RTSX	Yes, Parasitic clamping DIODE wrt "GND"	No, no clamping to any voltage exists.
SX16P	Yes, Parasitic clamping DIODE wrt "GND"	Yes, Parasitic clamping DIODE wrt "VCCR"
SXA	Yes, Parasitic clamping DIODE wrt "GND"	Yes, clamping DIODE wrt "VCCI", when diode is programmed to be on/present(3.3V PCI mode) No, no clamping DIODE to any voltage exists, when the diode is programmed to be off.

NOTE:

- 1) The notation "wrt" means "With Respect To"
- 2) The notation PROTECTION DIODE (in Figure A.1) equally is referred to as a clamping diode, and these terms both refer to the clamping diode effect, which acts on the digital IO signals. Although we refer to these as protection diodes or clamping diodes as individual components, we are really referring to a clamping diode effect. This clamping diode effect is produced by one of the following methods:
 - A) Diode effect produced by the parasitic diode effect in the IO pins' output buffers' output pull-down and pull-up transistors. As an example, when an input signal exceeds VCC+0.5V on an RH1280, the P-channel pull-up output transistor (which is connected to this IO pin) is reverse biased and acts as the input protection diode.
 - B) Diode effect produced by an individual clamping diode that has been intentionally designed-into the device. These diodes are designed in to Actel devices for the purpose of performing the PCI clamping diode requirements on the Actel FPGA devices that are PCI compliant.
- 3) The clamping diode effect is totally separate from and unrelated all Electro-Static-Discharge (ESD) protection circuitry, which also exists on every IO pin on every Actel FPGA.