

A FOUNDATION ARCHITECTURE FOR ELEVATING DSP IN FPGAS

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ABSTRACT

Commonly Military equipment has always desired more performance from their systems than technology has been able to provide. This covers all areas from the defense systems themselves to the test equipment that is used to prove these systems. These systems require the processing of increasing data sets and accelerating bandwidth originating from applications such as radar, sonar and imaging. Additionally multi-sensor fusion further accentuates the increases in the data processing demands of modern systems.

Traditional DSP processor architectures have only been capable of performing low complexity image processing functions in real time and this is still the case even with the very latest DSP processors from the Texas Instruments and Analog Devices. Furthermore the relatively short life of any processor makes the DSP a less than ideal solution in military system.

The advent of the FPGA back in the late 80's shone a new light on to the data processing possibilities. Nallatech saw the growing capabilities of the FPGA and was one of the first adopters to build systems that harnessed the FPGA as a coprocessor to various DSPs and Microprocessors.

These ideas were demonstrated in HardWare In the Loop, HWIL, systems proving equipment. This early equipment was used to generate simulated 3D target imagery to test British Aerospace's Rapier Weapon systems. The FPGAs were initially used to perform simple Gain and Offset control and Filtering functions at the pixel processing level. This partitioning of multiple FPGAs and multiple Microprocessors in the system allowed Real Time Image processing functions at a very low latency to be achieved.

Through the 90's the FPGA's increased in capacity and speed thus redefining the partitioning of FPGAs and Processors enabling more of the heavy processing requirements normally performed on the DSP to be moved across to the FPGA. Also, HWIL technology has progressed with the advent of the Thermal Picture Synthesizer, TPS, which generates a thermal image using an array of resistors that are individually heated. The Applied Physics Laboratory at JHU is currently utilising an earlier generation of Nallatech's hardware in the form of a British Aerospace Scene Generator that provides real time rendered 3D images to the TPS.

Over the last two years Nallatech has been consolidating its expertise in the field of DSP implementation in FPGAs. One result of this consolidation has resulted in a new module standard that has been created to form the foundation of building future high performance data processing systems that benefit from FPGAs as a key processing element. This module standard is labeled DIME, an acronym for Dsp and Image processing Module for Enhanced fpgas.

During the development of DIME there were several key performance criteria that Nallatech wanted to be able to achieve with this architecture. One of the criteria was to meet the demands of higher performing Image processing systems, The following lists details the requirements of such a system.

1. Image Resolution - 1024 x 1024
2. Image Generation Oversampling to Minimize Aliasing - 4 x 4 (effective resolution of 4096 x 4096)
3. Image Pixel Dynamic Range - 16 Bits
4. Frame rates - > 100Hz (>200Hz at 14bit Range)
5. Frame Latency - <1 frame

A simple calculation of these figures yields a data throughput of: -

$$\text{Data Throughput} = 4096 * 4096 * 2(16 \text{ bits}) * 100 = 3.36 \text{ GIGABYTES PER SECOND}$$

This is equivalent to a pixel clock frequency of 1.67 GHz. Even the latest top performing microprocessors such as the DEC Alpha or TMS320C6x do not attain these speeds. The performance problem is further emphasised using conventional microprocessor architectures as image processing operations are generally performed with more than one clock cycle. This results in further scaling of the required clock speed leading to unimaginable clock frequencies being required to attain the performance required by these HWIL imaging systems.

This paper discusses why it is timely to have a board level standard for building multi-FPGA based systems, the performance and bandwidth gains over standard processor architectures and the HWIL applications that it is being used in, with a particular emphasis on HWIL testing platforms for military systems.

THE ARCHITECTURE PLAYING FIELD IS CHANGING

The DSP Processor has been at the heart of a vast array of DSP processing tasks for over a decade now. With the advent of the FPGA companies have made use of this flexible hardware for minor coprocessing tasks as indicated in Figure 1.

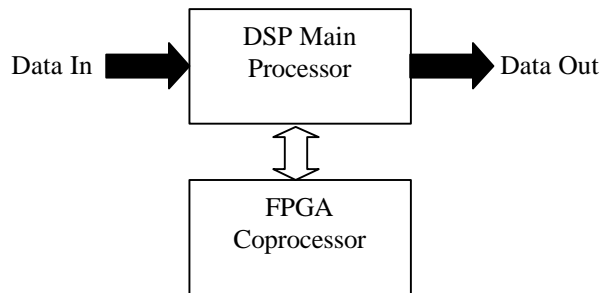


Figure 1 - Traditional Hardware Architecture

Today it is possible for the FPGA to become central to the DSP processing that has to be performed on the Data. Hence it is fair to assume a role reversal where the FPGA becomes the Main DSP Processor and the DSP processor becomes the Coprocessor. The DSP cannot be currently removed because it is still considered that certain parts of a DSP task are still best performed in the traditional DSP processor. Figure 2 depicts this architecture that is achievable today.

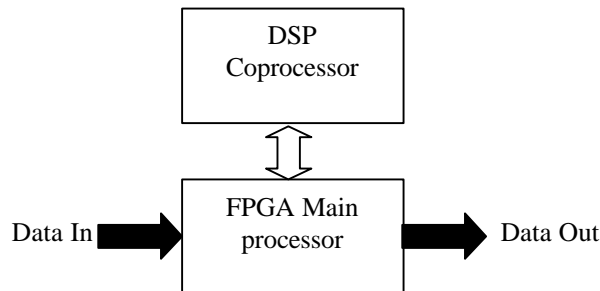


Figure 2 - FPGA Central to the DSP Function

Finally as FPGAs get ever larger it will not be too far ahead before the traditional DSP processor will be a thing of the past and the FPGA will absorb the whole DSP function. I.e. algorithms will be directly compiled to hardware. Figure 3 depicts the future architecture that we will see.



Figure 3 - Future - Algorithms will be compiled directly to the FPGA

The obvious difference between the first FPGA DSP architecture shown in Figure 1 and the emerging architectures in Figure 2 and Figure 3, is that the Data path is now passing through the FPGA and not the DSP processor.

Traditional DSP suppliers are recognising that the FPGA is required to play an increasingly important role in their products and they have therefore been developing products, that include FPGAs, based around the traditional DSP architecture. These suppliers typically utilise module standards have been prolific in the DSP world where they facilitate the development of Multiprocessor systems. The DSP module standards that have been around over the last 15 years include:-

- TRAM - First Generation **TR**Anspu**ter M**odule
- HTRAM - Second Generation **H**igh Speed **TR**Anspu**ter M**odule
- TIM40 - **T**exas **I**nstru**M**ent **S**tandard for the **C40** Family of DSPs
- SHARCPAC - Analogues Devices Module Standard for the SHARC family of DSPs

These module standards have always been tightly coupled to the DSP that they are associated with and they provided the ability to easily scale a parallel processing system with the number of processors to perform any given task. These standards have also been extended to support many different I/O capabilities in such systems that have made it possible to easily construct systems that are suitable for a wide variety of applications.

The problem is that these module standards do not facilitate the architecture shift that has been described above. Therefore Nallatech concluded that a new module standard was required to both support this architecture shift as well as additional problems that new technology has brought to the scene, such as the ramp down in core voltages. This new module standard is now commonly known as DIME.

THE BASIC DIME MODULE

The DIME Module standard was developed to address this step change in the technology arena. The main focus of the DIME standard has been that it is a general purpose module standard based around the FPGA rather than any specific Microprocessor or DSP. The DIME module is based on a multi-level standard. At the lowest level, Level 0¹, it defines the physical format and the essential pin connections. The higher level, level 1, defines the system level. There can be several different system Level standards for different applications. The “Video Processing” Level 1 standard² has been utilized for this architecture.

The basic DIME module layout is depicted in Figure 4. It can be seen that the positioning of the “module to motherboard” connectors and the FPGA are such that they aid the Pipeline flow of the video data. This layout yields exceptionally short PCB traces and this aids the ability to run the video data at very high frequencies.

The design of the module also allows for additional I/O connectors at the top of the module that provide easy access for external signals such as video leads or Fibre optic links when the module is populated onto its motherboard. This module design is also beneficial for Compact PCI Systems that utilise the VME form Factor. Here the positioning of the I/O connectors allow easy access to the aluminium front panel in these systems.

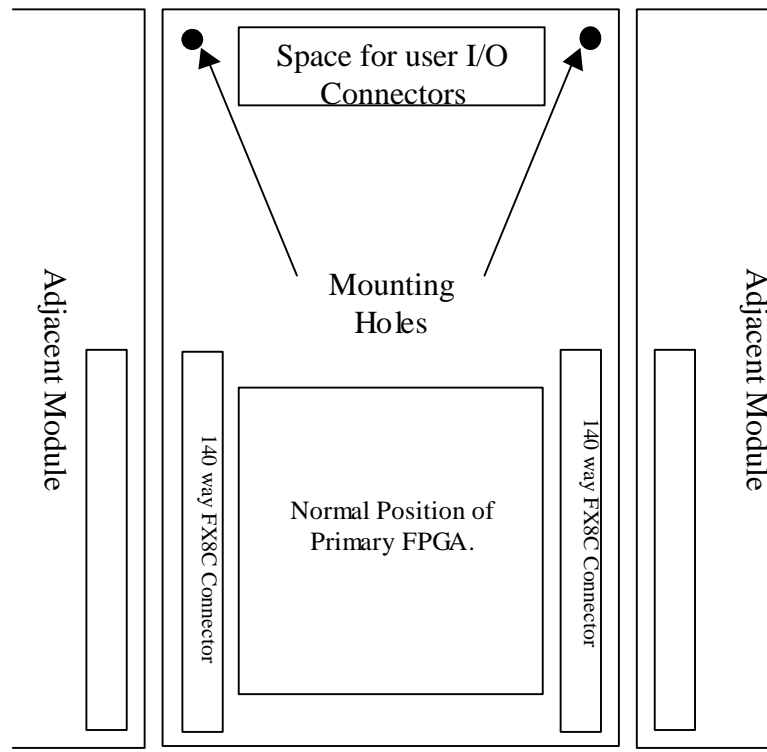


Figure 4 – DIME Module Basic Outline

The DIME architecture has been designed to accommodate PCB level Pixel clock frequencies of greater than 128MHz. Careful attention to design of the architecture was required to be able to attain such frequencies.

The other Key factor in the definition of the DIME standard was that the Module had to be very generic so that it could easily be adapted to many different applications and benefit from the flexibility offered by FPGAs which is unavailable with standard processors. The standard has the two levels of abstraction. The first Level is known as "Level 0 - The Physical Level" and the second level is known as "Level 1 - The Virtual Level".

DIME Level 0 - The Physical Level

The Physical Level specifies the basic mechanical and electrical properties of the module. It also defines two independent JTAG Boundary Scan chains for the modules. The first is used for configuring the modules FPGA's and the second is in place for DSP and Microprocessor "In Circuit Emulator" support, if these devices are designed onto the module. FPGA configuration in this manner ensures that the module standard is 100% compatible with a wide variety of FPGAs from different vendors and is compatible with standards such as Xilinx's JBits technology. Further to this, there are over 200 unspecified I/O lines between the module and its motherboard.

DIME Level 1 - The Virtual Level

The Virtual Level then provides a rigid application focussed definition of the Unspecified I/O Pins. For example common busses can be defined between modules that include specific communication protocols. The standard can support many different Level 1 standards. Ideally all of the I/O on a module will be routed into its FPGA. Therefore all modules designed to the standard will be compatible with any Level 1 standard simply by a firmware update to the FPGA. Only DIME carrying motherboards will need to be designed to specifically support the different level 1 standards.

Nallatech has currently specified a DIME Level 1 standard for Distributed Image processing systems. This defines deterministic video busses as well as a multi-processor communications network that is based around Analog Devices HammerHead SHARC family.

DYNAMIC RECONFIGURATION OF MULTIPLE FPGAs IN A DIME SYSTEM

One of the fundamental assumptions of any DSP processing system is that it can easily be configured with a users latest application without the need for a soldering iron or any electronics knowledge. Although the FPGA is far closer to the pure hardware layer of abstraction than a DSP this same ease of use must be implemented to make any system based on FPGAs both viable and acceptable for the user.

Therefore at the concept stage of DIME it was decided that the modules must be of a Plug'n'Play nature. This would ensure that users could simply populate the modules of interest into their system and be up and running with the modules in a matter of minutes. This plug and play approach is supported by Nallatech's unique software that both detects DIME modules in a system and configures these modules with the users bitstreams in a matter of seconds. The diagram below shows the GUI that the user can utilise during algorithm development.

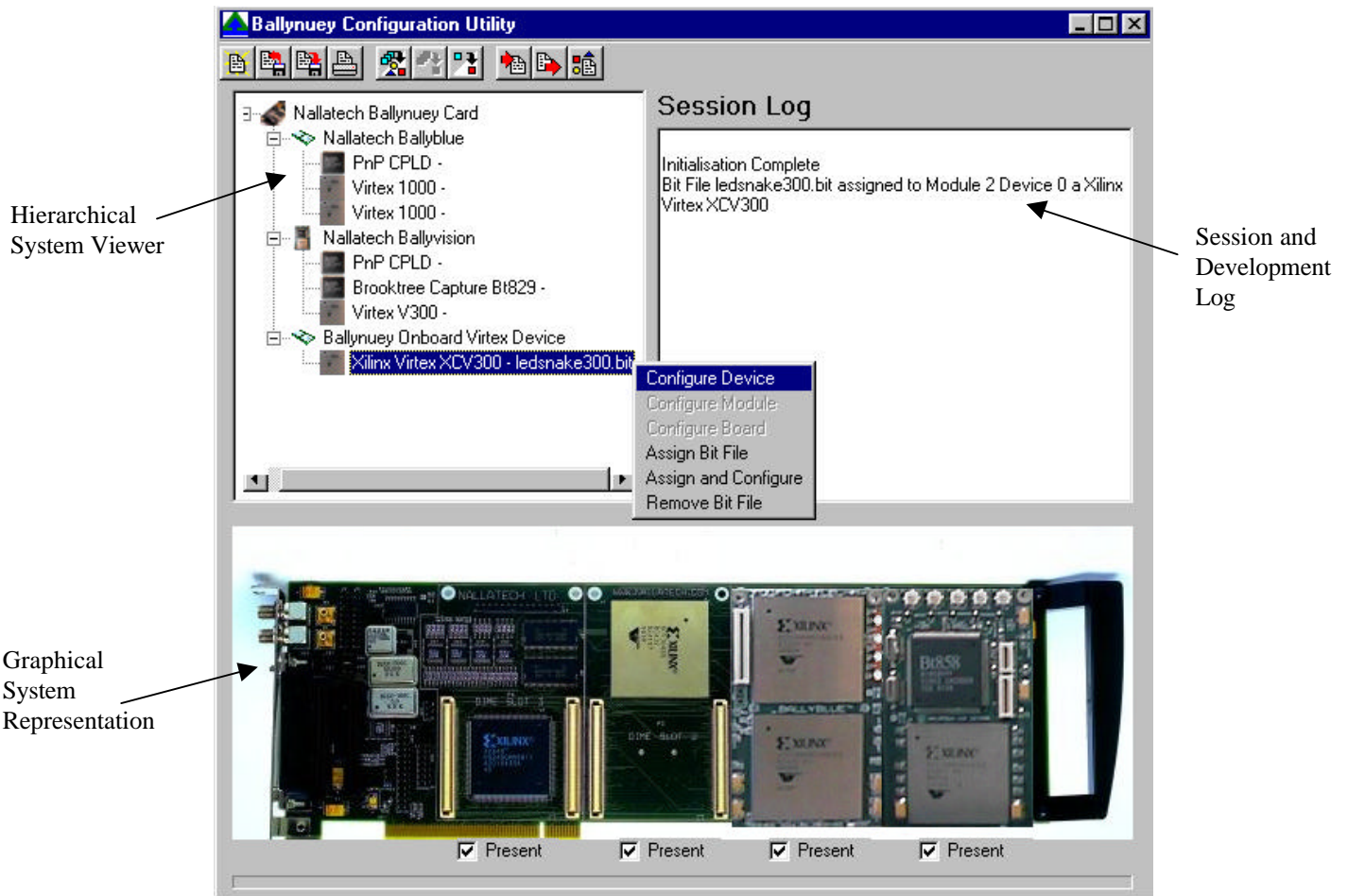


Figure 1 shows the three key elements of the DIME configuration application. The hierarchical system viewer identifies the DIME motherboards, the installed DIME modules and JTAG enabled devices, which are dynamically detected in the plug and play scan that is incorporated in the software and supported by the hardware infrastructure. The session log is provided for

tracking development, detailing the configuration process applied to the DIME system and the status of the configuration. Additionally, the graphical representation displays a dynamic image of DIME modules that have been detected and their positions on the Ballynuey board.

Configuration of Virtex devices is facilitated through the GUI. The hierarchical system viewer provides a typical explorer style interface that can be expanded to show the individual devices detected. The viewer allows for selection of configuration bit-files for individual Virtex devices and subsequently configuration with the selected files. Options are provided to either configure all Virtex devices on the selected board, all devices on a selected module or an individual selected Virtex device. This hierarchical system view substantially simplifies configuration of multiple Virtex devices and configuration times are significantly reduced through the use of cable-less configuration over the PCI bus.

DIME MODULE CONFIGURATIONS AND APPLICATIONS

SHARC DIME Module – The Ballysharc

Figure 5 shows a block diagram of the SHARC DIME Module. Two DSP Processors share the floating point computing load and feed into the FPGA processing to carry out the pixel manipulations.

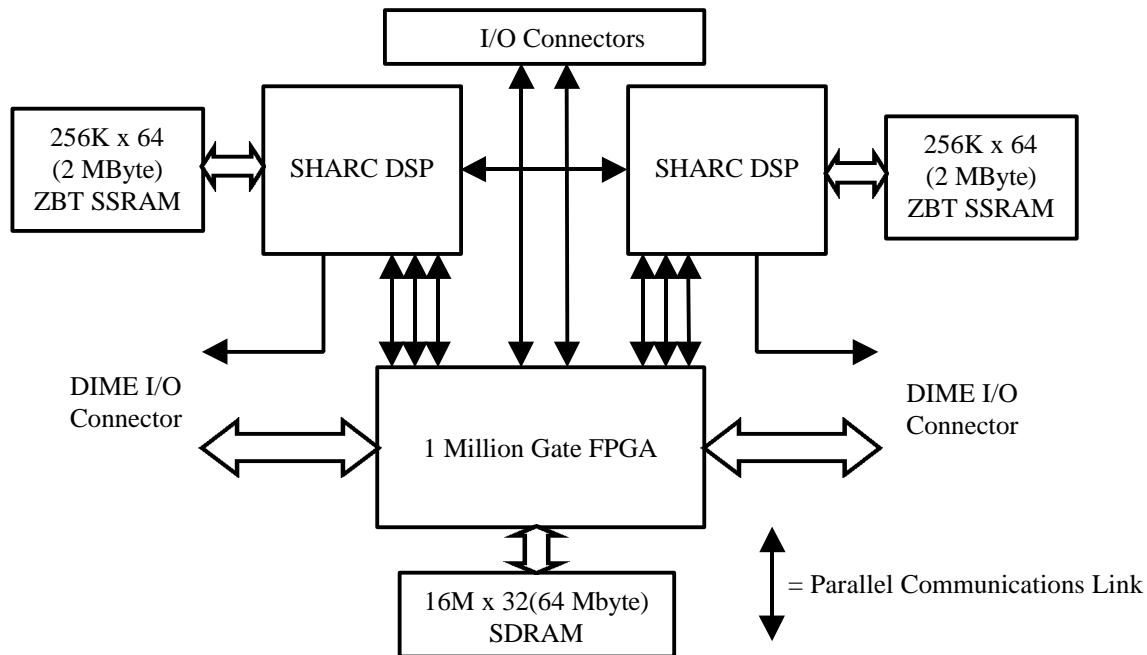


Figure 5 – SHARC DIME Module Block Diagram

The block schematic shows the significant data paths. Parallel digital video external to the module is input directly to the Virtex FPGA and output from it. Coupling from the two processors to the FPGA is carried out via four of the six 8 bit communication channels of the SHARC. This gives a net data rate from each SHARC to Virtex of 400Mbytes/second. The remaining two channels are used for communications to the rest of the system and to the other on board processor. The SHARC processors are tightly coupled to local memory stores used for instructions and data. The maximum data rate on this bus is 700Mbytes/second. The two SHARC processors are directly connected through a communication channel providing a 100Mbytes/sec bandwidth for parameter passing and synchronization.

Dual 1 Million Gate FPGA DIME Module – The Ballyblue

This DIME module has been designed to conquer those complex two dimensional image processing problems that have been the main stay of the DSP microprocessor technologies and dedicated ASICs to date. Examples of Image processing functions that this module can easily perform in real time include: -

- 2D Convolution
- 2D Correlation
- Image Generation using the Particle Method

The addition of independent banks of SDRAM memory and a FIFO increase the ability of this module to solve many different types of computationally intensive Image Processing Algorithms.

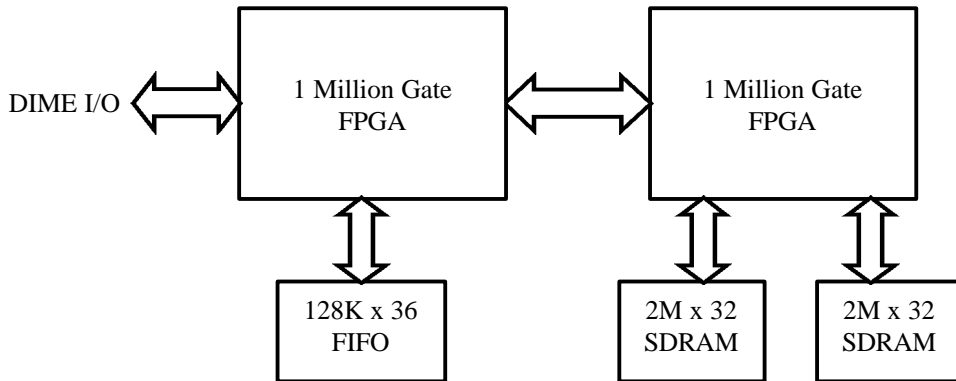
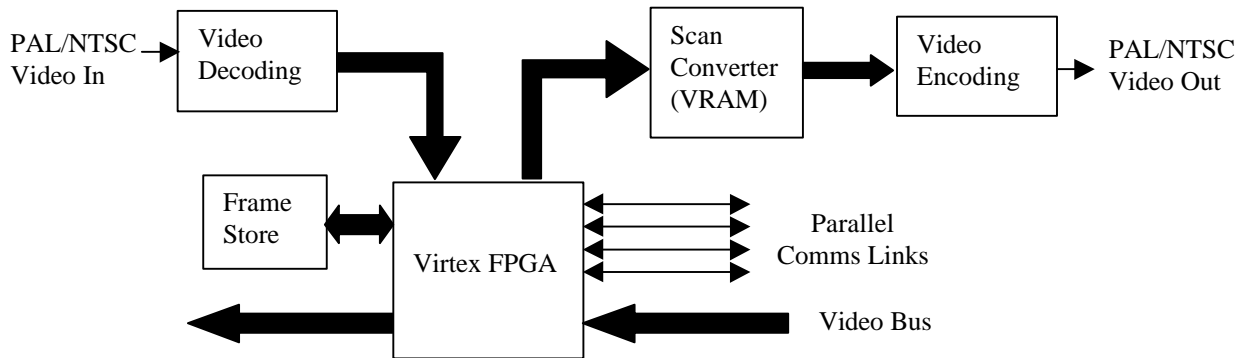


Figure 6 – Dual 1 Million Gate FPGA DIME Module Block Diagram

Analogue Video I/O DIME Module – The Ballyvision

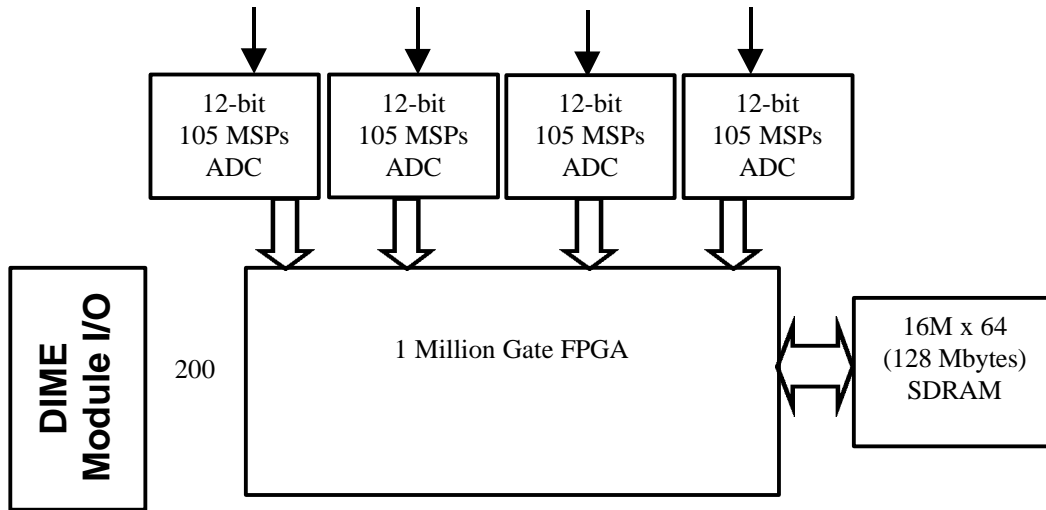
This analogue Video I/O module allows for the input and output of video data in NTSC or PAL using Composite or Y/C formats. This module includes a scan converter that can convert non standard frame rates to that required by PAL and



NTSC, thus allowing non-standard images which may be generated by the system to be viewed and recorded on standard video equipment. A framestore has also been included in this module that allows images to be captured for slower post processing.

Four Channel 12bit, 100MSPS A/D Converter DIME Module – The Ballyriff

This DIME module provide the ability to capture a vast range of different types of analogue inputs. This can range from simple sensory inputs all the way up to the capture of RF data. The figure below shows the basic architecture of this DIME module.



REAL TIME TARGET GENERATION FOR HWIL APPLICATIONS

Typical Target Scene Generator, TSG, systems are based on an architecture as shown in figure 7. The generation is broken into component parts as dictated by the problem. In general IR images may be separated into background, target and obscurations such as plume and flares. A processing section is allocated to each component and pipelined on a pixel by pixel basis to minimise latency. Typically therefore a pixel generated in the background block is modified added to or replaced by subsequent operations in the following blocks and is output from the video stage after only a 3 or 4 line delay.

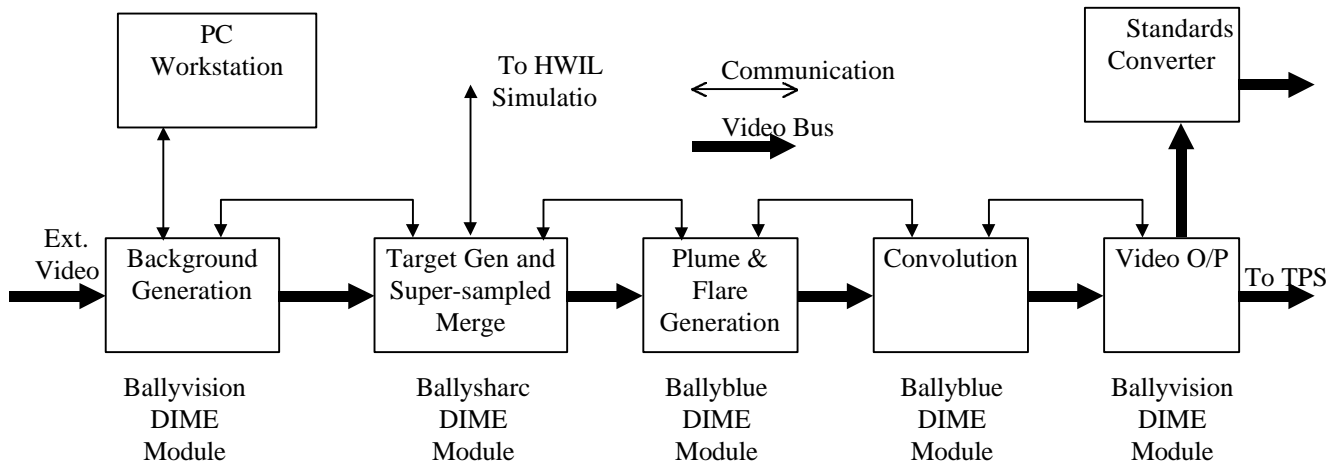


Figure 7 - Typical HWIL Image Generation System

Each of the elements in the simulator can be implemented in a separate DIME module. The Video Input, Background Generation and Video Output are performed in a single DIME module in this application. Therefore a total of four DIME modules are enough to perform this very complex HWIL function. These four DIME modules can reside on a single Local PCI

plug in card that fits into one PCI slot of a standard PC. The PC provides the man machine interface to the simulator making this a very compact solution to this HWIL problem.

Every function is performed in real time with a very low latency. These functions were previously unachievable without large racks of hardware or dedicated ASICs and DSP's have nowhere near the performance capabilities to even come close to the amount of processing that is required here.

CONCLUSION

This paper has demonstrated that with the latest generation of FPGAs we can perform serious DSP processing tasks with these devices. It has also highlighted the lack of architectural support for this new type of DSP system in a modular and scalable format.

The DIME module standard was introduced and proposed to be an excellent Scaleable, modular system that puts the FPGA as the centre of the DSP processing function rather than the DSP processor. Several types of modules have been discussed and it has been shown how these have been utilised in a real world HWIL application.

It is therefore fair to say that the DIME module standard elevates the ability to use FPGAs in a DSP environment. This has also been achieved without the need for DSP engineers to always start at the component level. The configuration tools provided with DIME allow the developer to quickly test new implementations without the need to have any knowledge of how FPGAs are configured.

1. DIME Module, Physical Level 0 Specification, Nallatech Ltd, NT301-0001
2. Video processing, implementation Level 1 of the DIME Module, Nallatech Ltd, NT301-0002