Reconfigurable, System-on-Chip, High-Speed Data Processing and Data Handling Electronics

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Performance requirements for spaceflight electronics have been increasing as detectors produce greater amounts of data at higher resolutions. Concurrently, there is an increasing need to produce spacecraft electronics in shorter periods using less spacecraft resources.

The objective of this research is to develop, demonstrate, and refine architectural techniques and tools for gate arrays to permit rapid, reliable development of high-speed processing and data handling functions, integrated onto a single chip. This research will provide designers with the ability to target either ASICs or Field Programmable Gate Arrays (FPGAs). Gate arrays and one-time programmable (OTP) devices may be configured quickly from mission to mission; reprogrammable FPGAs may be reconfigured in-flight.

This technology will produce a design environment permitting the engineer to design in an efficient and familiar manner, effectively reusing prior work, and minimizing the labor intensive, error-prone parts of the task. Design knowledge will be embedded into the tool, allowing easy application of the techniques and their implementations developed in the course of this work, with components optimized for the specific application. Existing computer aided engineering tools do not have the power to implement this; a unique solution blending the use of software and hardware-oriented tools, exploiting the benefits of each, are used to create the design environment.

The more general ideas present in this technology were formulated approximately 15 years ago; today, with available technologies what was considered theoretical university work is now practical and realizable. Indeed, over the past year, we have been implementing this technology in our R&D program with very good success. Some of the results of this work will be shown with the screen shots being "live" operational development systems.

We have found over the years that common functions tend to be redesigned repeatedly by independent teams; in fact, we have seen even small teams redesign the same function. This obviously is inefficient and costly in both development and verification time. We have systematically developed approaches to cut development time while increasing reliability through re-use; the techniques are considered state-of-the-art. As we move to more complex, high-performance systems with lower budgets and shorter development times, one could ask, "how fast can we design an efficient high performance system that meets requirements?"

The technology described in this paper shows a methodology, framework, and tool set to drastically reduce both costs and schedule. We have been developing the technology over the past year and a half. The areas of research have included user interfaces, links between design generation and verification, performance assessment, division of labor, and IP generation blocks. Some of these blocks have been running for over 6 months and have already been used, experimentally, for several real problems as a form of benchmarking. Certain design tasks that might have taken weeks to get *any* answer have been optimized in hours with little engineering time; previous engineering, embedded into the tools, has been re-used. This enables the design engineer to focus on the problem and algorithms for its solution, freeing him from re-doing lower level tasks.

Our current job assignment is for the development of microelectronics and signal processing solutions for space-flight scientific instruments and the work was originally done for that "target." However, the solutions are more generally applicable to many spacecraft control and data handling functions. One active area of development from our R&D team is extensible, modular processors that are high performance, efficient, and easily modified from mission to mission. We have explored various options with prototype code and development is moving quickly ahead.