

TOTAL DOSE AND SEE OF METAL-TO-METAL ANTIFUSE FPGA

J. J. Wang¹, Brian Cronquist¹, John McCollum¹, Frank Hawly¹, Donald Yu¹, Richard Chan¹,
Rich Katz², and Igor Kleyner³

¹Actel Corporation, Sunnyvale, CA 94086

²NASA/GSFC, Greenbelt, MD 20771

³Orbital Sciences Corporation, Greenbelt, MD 20771

Abstract

The development of RT/RH54SX, a new radiation tolerant/hard antifuse FPGA family, is introduced. It employs a metal-to-metal antifuse technology and sea-of-modules architecture. Total dose and SEE data will be presented and discussed in detail. Main results include achieving 100 krad (Si) tolerance in a commercial foundry, designing SEU-hard flip-flop, and designing SEDR-immune antifuse materials.

1.0 RT/RH54SX

Actel 54SX family employs a metal-to-metal antifuse switch and sea-of-modules architecture. The family uses 0.5, 0.35, and 0.25 μm CMOS technologies for various products. The RH/RT products will have 0.5 and 0.25 with 3.3/5.0V and 2.5/3.3V DC power supplies. The antifuse switch is shown in Figure 1. It acts as a nonvolatile switch between the top metal layers. The sea-of-modules architecture is shown in Figure 2. Tiles of logic modules and embedded SRAM (in some of the devices) are built on silicon and interconnected with the first few metal layers. There are two types of logic module, C and R-cells. A C-cell can implement most of the x-input combinational functions. The R-cell is basically a dedicated flip-flop (FF), or a register on which the name is coined which has selectable clock polarity and a dedicated enable. There is a global fast clock to be directly connected to the FF for high-speed and a routed clock network for flexibility. IEEE 1149.1 JTAG is also implemented. However, the ramification of SEE on the JTAG state machine was not fully realized in the early version of the device. This led to a redesign that employs a dedicated pin to hard reset the TAP controller (state machine) in all the later versions.

2.0 TOTAL DOSE

Since 0.5 μm and 0.25 μm are quite different technologies, their total dose effects are quite different and discussed separately.

2.1 0.5 μm

0.5 μm -54SX is fabricated by two foundries. LMFS employs a QML-qualified, radiation-hard process for TID tolerance no less than 300 krad(Si). This proprietary process can deliver the RH tolerance (> 100 krad(Si)) for almost any devices and is monitored lot-to-lot. No further discussion will be given on devices coming from LMFS. The other 0.5 μm foundry is MEC. The fabrication process uses a more conventional LOCOS isolation process. The TID induced leakage current flow in the silicon of the isolation area limits the tolerance. Static I_{CC} is the parameter that determines the tolerance in all cases so far measured. A noninvasive modification of the baseline process improved the tolerance to 100 krad(Si). Figure x shows the I_{CC} of three lot-split conditions. The middle split is chosen for the future process after doing a trade-off between TID tolerance and programmability.

2.2 0.25 μm

0.25 μm devices are fabricated by MEC using shallow-trench isolation (STI). Figure x shows a cross section of STI. The TID induced edge and field leakage in STI seems better than LOCOS. In spite of its much smaller dimension, the preliminary data (Figure x) indicates a relatively tolerant process. One major rationale is that in deep sub-micron process, high doping was implemented to reduce the off-state leakage. This processing trend also improves the TID induced leakage. Further improvement of the tolerance is ongoing and the data will be reported in time for the conference.

3.0 SEU

54SX family has very solid design for combating SEL. It has been measured SEL immune ($LET_{TH} > 120 \text{ MeV-cm}^2/\text{mg}$) for both 0.5 and 0.25 μm . The most significant SEEs are upset and dielectric rupture.

3.1 0.5 μm

The dedicated FF, i.e. R-cell, was extensively tested. Figure x shows the resulting cross section versus LET threshold data. The upset rates in the GEO environment is simulated as xxx by using the Space Radiation 4.0 software. This performance does not meet a radiation-hard criterion ($LET_{TH} > 37 \text{ MeV-cm}^2/\text{mg}$). Two improvement schemes are being implementing. A user defined FF composed of two C-cells can push the LET_{TH} to $> 40 \text{ MeV-cm}^2/\text{mg}$ while keeping the cross-section approximately the same as a R-cell (Figure x). The other scheme employs a TMR FF cell, which will have upset rates well below the other upset mode (e. g. combinatorial logic upset). Clock upset was not found in 0.5 μm devices. Combinatorial logic upset, although not fully tested, is considered not an issue as far as upset rate of 10^{-10} upset/bit-day is concerned. Both heavy ion testing and simulation indicate the transient pulses generated at the sensitive junction won't propagate for $LET_{TH} < 50 \text{ MeV-cm}^2/\text{mg}$.

The initial version of the device had a soft reset on the JTAG TAP controller (state machine). Heavy ion tests show that a loss of control occurs when the state machine, which contains 4 flip-flops, has SEUs. Resetting the state machine by a free running clock eliminates, in almost all cases, the loss of control but leaves a temporary soft-error mode (Figure x). A redesign by implementing a dedicated JTAG reset pin in the new version of devices proved by heavy ion testing that the loss of control as a result of TAP controller upset was totally eliminated.

3.2 0.25 μm

The heavy ion testing data done on the R-cell is plotted as cross-section versus LET (Figure x). These data are collected from the pre-production materials. The interesting point is that the saturation cross-section is about the same of 0.5 μm . This may be due to the smaller V_{CC} (2.5V) enhancing the sensitivity of the active junctions, or new error mechanisms such as the combinatorial logic inside the cell causing upset too. Preliminary simulation results showed combinatorial upset can occur for LET_{TH} as low as $10 \text{ MeV-cm}^2/\text{mg}$. The increased sensitivity poses a potential show-stopper for the SEU hardening design. Further testing is planned to fully test the combinatorial upset.

Single strike multiple upset (SSMU) [ref] also becomes a very important upset mode in 0.25 μm devices because the spacing between two active junctions is shrunk dramatically. Redundant designs such as TMR and DICE cell can become much less effective. Table 1 illustrates this point by simulating the upset rates of a 0.25 μm memory cell design. A straightforward implementation will not improve the SEU performance by more than two orders or magnitude. The other issue about SSMU is testability. The range of ion energies of the SEU facilities is not penetrative enough to test at shallow angles.

3.3 SEDR

To almost everybody's surprise, if not designed properly, a Metal-to-Metal (M/M) antifuse switch can still have a SEDR failure mode. Comparing to the ONO antifuse device, the operational voltage is lowered down from 5.0V to 3.3V. The dielectric thickness is larger, 100Å in ONO and 800Å in M/M. This results in more than an order of magnitude reduction in electric field strength across the M/M antifuse. The conjecture why M/M antifuse still ruptures is that it composes of mostly amorphous silicon, which is more defected than ONO, has lower melting point, and also has a narrower band gap.

Figure x shows the static I_{CC} jump when a M/M antifuse is ruptured by heavy ions. It is approximately 10 to 20 mA, about ten times higher than that of ONO. The consequence of a M/M rupture is thus more severe. However, antifuse redesign was done and we successfully found recipes to build M/M antifuse completely immune to SEDR (Table 1).