

Designing Space Applications Using Synthesizable Cores

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Abstract

Very high integration levels of microelectronics will be required to fulfill the ever-increasing demands on performance in terms of processing speed, mass and power. With an increasing number of available gates on silicon, the functionality being implemented will move away from the use of traditional components to more advanced and complex systems within a single device. To develop such complex circuits the design methodology will have to change from being gate-level oriented to the integration of complex building blocks. The designers will have to rely on preexisting building blocks with already verified functionality, with documentation and production test vectors being available, which have ultimately been validated on silicon.

This paper will concentrate on how such building blocks are developed in VHDL and how they are purchased, distributed and used in the scope of European Space Agency activities, ranging from in-house developments to contractor work and from simple Field Programmable Gate Arrays (FPGAs) to complex System-On-a-Chip (SOC) designs. The paper will also give examples of good and poor design methodologies when developing FPGAs, based on real flight developments. As a comparison to what is achievable in FPGA technology, a current complex SOC development will be presented.