

A FOUNDATION ARCHITECTURE FOR ELEVATING DSP IN FPGAS

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ABSTRACT

Commonly Military equipment has always desired more performance from their systems than technology has been able to provide. This covers all areas from the defense systems themselves to the test equipment that is used to prove these systems. These systems require the processing of increasing data sets and accelerating bandwidth originating from applications such as radar, sonar and imaging. Additionally multi-sensor fusion further accentuates the increases in the data processing demands of modern systems.

Traditional DSP processor architectures have only been capable of performing low complexity image processing functions in real time and this is still the case even with the very latest DSP processors from the Texas Instruments and Analog Devices. Furthermore the relatively short life of any processor makes the DSP a less than ideal solution in military system.

The advent of the FPGA back in the late 80's shone a new light on to the data processing possibilities. Nallatech saw the growing capabilities of the FPGA and was one of the first adopters to build systems that harnessed the FPGA as a coprocessor to various DSPs and Microprocessors.

These ideas were demonstrated in HardWare In the Loop, HWIL, systems proving equipment. This early equipment was used to generate simulated 3D target imagery to test British Aerospace's Rapier Weapon systems. The FPGAs were initially used to perform simple Gain and Offset control and Filtering functions at the pixel processing level. This partitioning of multiple FPGAs and multiple Microprocessors in the system allowed Real Time Image processing functions at a very low latency to be achieved.

Through the 90's the FPGA's increased in capacity and speed thus redefining the partitioning of FPGAs and Processors enabling more of the heavy processing requirements normally performed on the DSP to be move across to the FPGA. Also, HWIL technology has progressed with the advent of the Thermal Picture Synthesizer, TPS, which generates a thermal image using an array of resistors that are individually heated. The Applied Physics Laboratory at JHU is currently utilising an earlier generation of Nallatech's hardware in the form of a British Aerospace Scene Generator that provides real time rendered 3D images to the TPS.

Over the last two years Nallatech has been consolidating its expertise in the field of DSP implementation in FPGAs. One result of this consolidation has resulted in a new module standard that has been created to form the foundation of building future high performance data processing systems that benefit from FPGAs as a key processing element. This module standard is labeled DIME, an acronym for **D**sp and **I**mage processing **M**odule for **E**nhanced fpgas.

During the development of DIME there were several key performance criteria that Nallatech wanted to be able to achieve with this architecture. One of the criteria was to meet the demands of higher performing Image processing systems, The following lists details the requirements of such a system.

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| 1. Image Resolution | - 1024 x 1024 |
| 2. Image Generation Oversampling to Minimize Aliasing | - 4 x 4 (effective resolution of 4096 x 4096) |
| 3. Image Pixel Dynamic Range | - 16 Bits |
| 4. Frame rates | - > 100Hz (>200Hz at 14bit Range) |
| 5. Frame Latency | - <1 frame |

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A simple calculation of these figures yields a data throughput of: -

$$\text{Data Throughput} = 4096 * 4096 * 2(16 \text{ bits}) * 100 = 3.36 \text{ GIGABYTES PER SECOND}$$

This is equivalent to a pixel clock frequency of 1.67 GHz. Even the latest top performing microprocessors such as the DEC Alpha or TMS320C6x do not attain these speeds. The performance problem is further emphasised using conventional microprocessor architectures as image processing operations are generally performed with more than one clock cycle. This results in further scaling of the required clock speed leading to unimaginable clock frequencies being required to attain the performance required by these HWIL imaging systems.

The DIME architecture has been designed to accommodate PCB level Pixel clock frequencies of greater than 128MHz. Careful attention to design of the architecture was required to be able to attain such frequencies.

The other Key factor in the definition of the DIME standard was that the Module had to be very generic so that it could easily be adapted to many different applications and benefit from the flexibility offered by FPGAs which is unavailable with standard processors. The standard has the two levels of abstraction. The first Level is known as “Level 0 – The Physical Level” and the second level is known as “Level 1 – The Virtual Level”.

DIME Level 0 – The Physical Level

The Physical Level specifies the basic mechanical and electrical properties of the module. It also defines two independent JTAG Boundary Scan chains for the modules. The first is used for configuring the modules FPGA's and the second is in place for DSP and Microprocessor “In Circuit Emulator” support, if these devices are designed onto the module. FPGA configuration in this manner ensures that the module standard is 100% compatible with a wide variety of FPGAs from different vendors and is compatible with standards such as Xilinx's JBits technology. Further to this, there are over 200 unspecified I/O lines between the module and it's motherboard.

DIME Level 1 – The Virtual Level

The Virtual Level then provides a rigid application focussed definition of the Unspecified I/O Pins. For example common busses can be defined between modules that include specific communication protocols. The standard can support many different Level 1 standards. Ideally all of the I/O on a module will be routed into its FPGA. Therefore all modules designed to the standard will be compatible with any Level 1 standard simply by a firmware update to the FPGA. Only DIME carrying motherboards will need to be designed to specifically support the different level 1 standards.

Nallatech has currently specified a DIME Level 1 standard for Distributed Image processing systems. This defines deterministic video busses as well as a multi-processor communications network that is based around Analog Devices HammerHead SHARC family.

The final paper will discuss why it is timely to have a board level standard for building multi-FPGA based systems, the performance and bandwidth gains over standard processor architectures and the HWIL applications that it is being used in, with a particular emphasis on HWIL testing platforms for military systems.