Radiation test results of the Virtex FPGA and ZBT SRAM for Space Based Reconfigurable Computing

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Abstract

We at Los Alamos National Laboratory are designing a high performance reconfigurable computing module for high-speed digital signal processing and on-orbit signal analysis. In order to achieve in excess of 100 MegaSample/sec processing performance and the capability for on-orbit reconfiguration, we must adapt COTS technology to the hostile space environment. The availability of the *Virtex* SRAM-based FPGA by Xilinx, Inc., which provides 1 million system gates on a single chip, provides a unique opportunity to develop a system with this capability. The system also requires high speed SRAM and is being designed with ZBT SRAMs available from Micron, IDT, or Motorola. There are three broad challenges for this design. The first is whether the components will survive the radiation environment. The second is how to design for the expected high single event upset rate. The last concerns package and printed circuit board reliability in a thermal cycling environment.

The ionizing dose tolerance and heavy-ion single event effects (SEE) performance of these technologies will be presented along with the radiation test methodologies. These 0.35µ and 0.25µ COTS technologies have demonstrated up to 100k rad(Si) dose tolerance, making them ideal candidates for many space applications. Discussion of SEE test results will include latch-up performance of the epi-based FPGA and an in-depth analysis of the upset characteristics. There will be a discussion of the bit-upset sensitivity of the part in both a static mode and dynamic operation. During operation, the device under test may experience additional contribution to upset sensitivity from ion interaction with combinatorial logic. We will also discuss our investigation of the upset sensitivity of the JTAG TAP controller.

Given the fact that these components will upset frequently, system design strategies become essential to achieve reliability. With SRAM based FPGAs, the actual configuration will be susceptible to upset in addition to user memory cells. We will discuss the challenges of working with volatile components and present preliminary detection, mitigation and recovery techniques.

Assembling high-density packages to printed circuit boards in a reliable fashion will be challenging. High-density packages are critical to achieving the bandwidth required for reconfigurable signal processing. We will present our concerns about CTE matching and package options, as well as review some earlier pioneering studies on high density package reliability.

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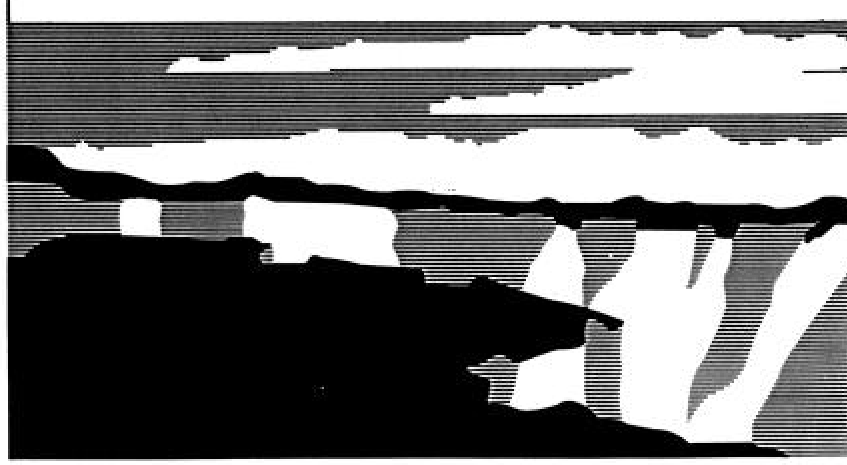

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