

## SEU Induced Anomalous Operation of Voted Ripple Clocks

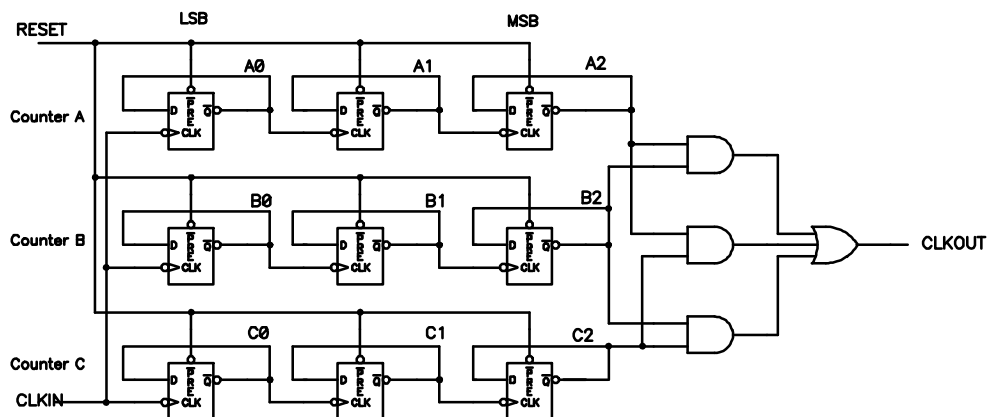
Dr. Rod Barto  
3312 Moonlight  
El Paso, Texas 79904  
915-755-4744  
email: rod.barto@worldnet.att.net

**Abstract:** The effects of single-event upsets (SEUs) on a particular type of voted ripple clock are examined. A mathematical theory is developed from which the probability of correct operation of the clocks is calculated.

### 1. Introduction

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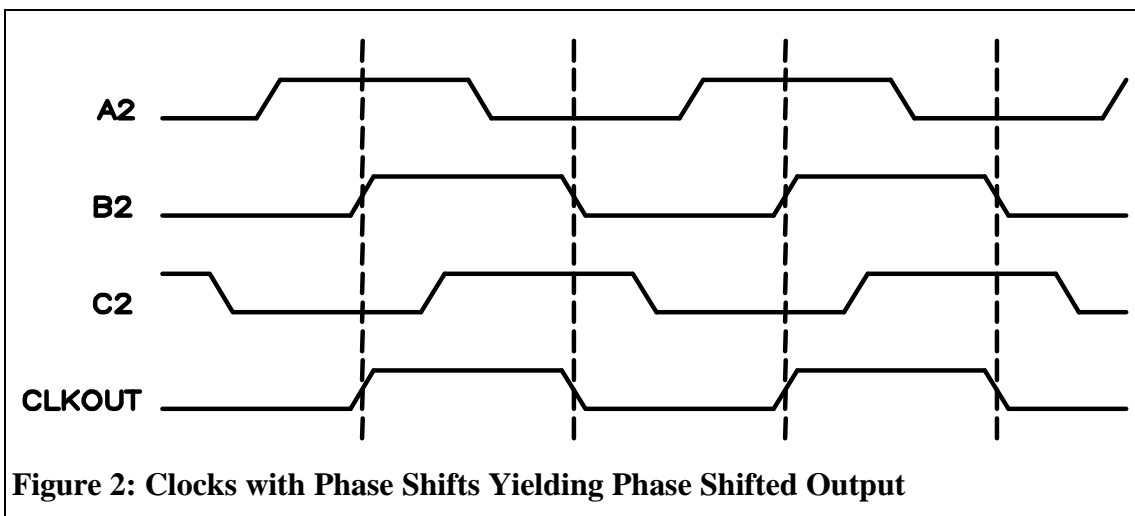
In order to make the circuitry inside FPGAs less SEU sensitive, a voting scheme is used in which 3 flip-flop outputs are voted together. One application of this is found in counter divide chains, an example of which is shown in Figure 1. Here, 3 counter chains A, B, and C, each of which divide the input clock CLKIN, have their MSBs voted together by an AND/OR network to produce an output clock CLKOUT. Note that each chain constitutes a ripple counter and that each chain is independent. The voting takes place only at the output (MSB) flip-flop. A counter in which the voting was performed at each stage would require considerably more gates, but would be more SEU immune.



**Figure 1: Three Bit Voted Ripple Counter**

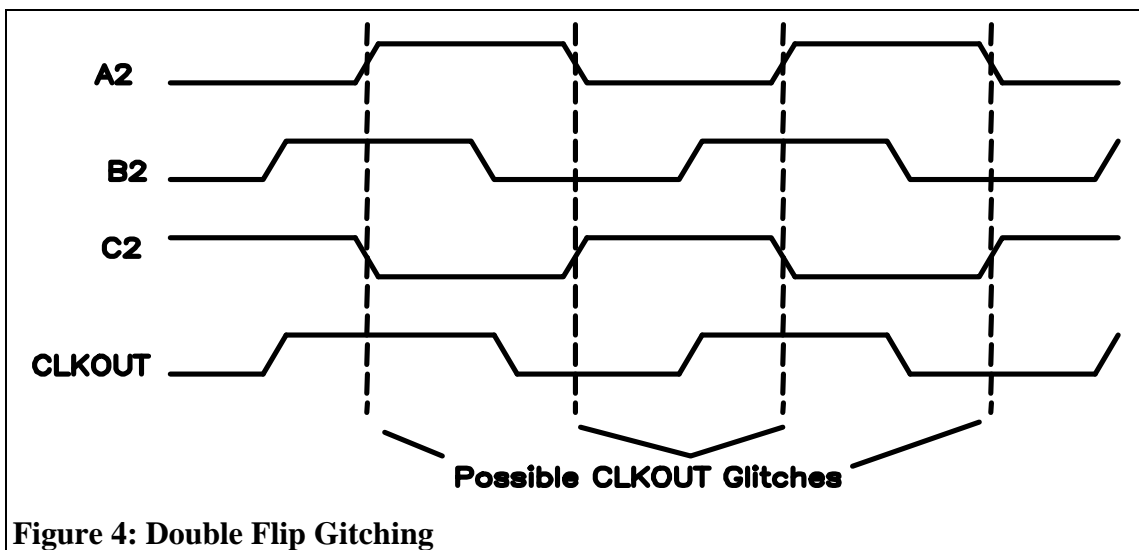
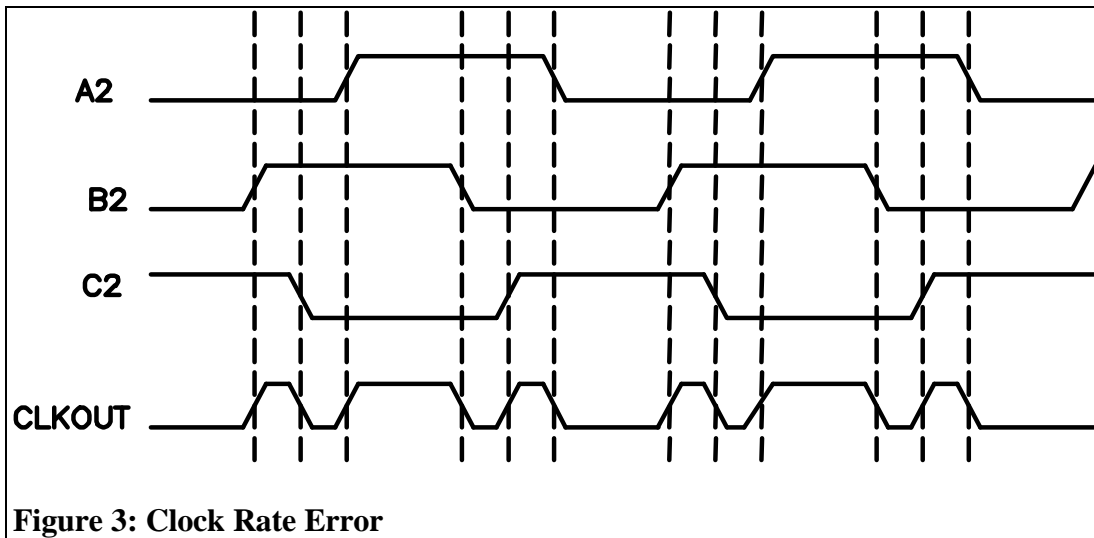
Analysis of the Figure 1 clock voting scheme shows that SEUs can cause phase shifts in the individual clock chains that remain until the chains are reset by the RESET signal. Phase shifts can cause four types of anomalous clock operation:

- **Clock Rate Error:** Some combinations of phase shifts resulting from 3 bit flips can cause the output clock to have 3 times the expected frequency;
- **Double Flip Glitching:** Some combinations of phase shifts resulting from 2 bit flips can cause glitching on the output clock;
- **Output Phase Shifting:** Some phase shifts resulting from double bit flips could potentially cause anomalous operation of circuitry that uses the voted clock or the individual clock chain MSBs before voting;
- **Single Flip Glitching:** Some single bit flips can also cause output glitching.



**Figure 2: Clocks with Phase Shifts Yielding Phase Shifted Output**

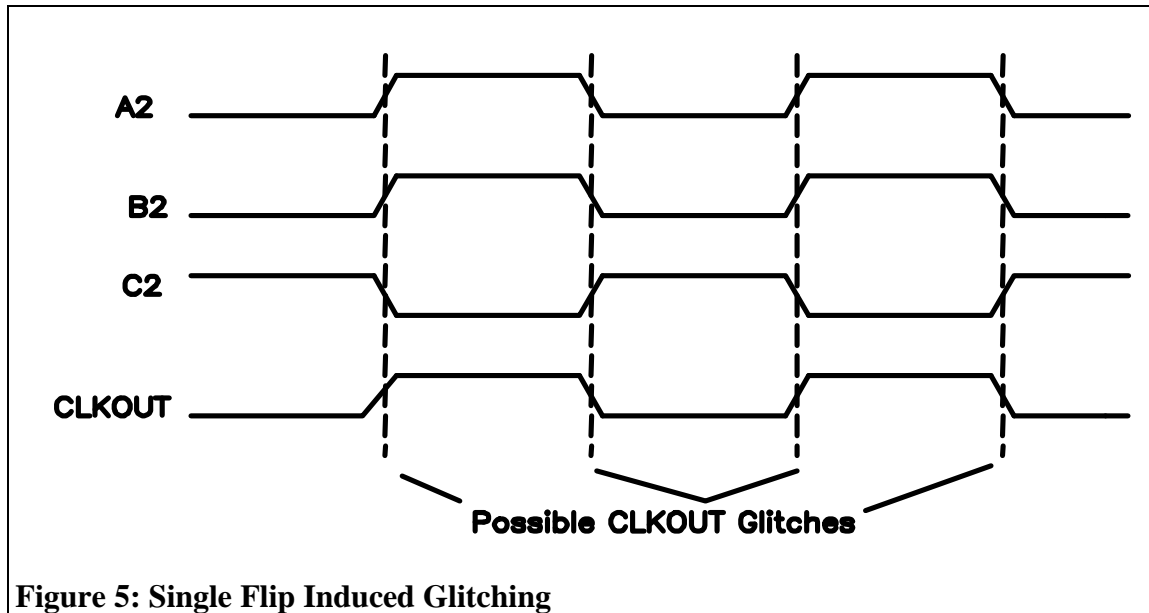
Figure 2 shows the MSBs and resulting output clock with a combination of phase shifts which shifts the phase of the output clock, assuming the original phase is that of clock A. Note that even though the individual clock chains are shifted in phase relative to each other, the output clock has the correct frequency and duty cycle. An example of a combination of phase shifts which will produce an output rate error is shown in Figure 3. Clearly such a clock will cause any circuit driven by it to operate incorrectly. Figure 4 shows the type of glitching that can occur after 2 bit flips, resulting from clocks A and C rising and falling out of phase. Figure 5 shows glitching that can result from one flip.



This memo first derives a mathematical theory by which the behavior of these clocks can be described, then determines the probabilities of the various types of anomalous behavior.

## 2. Mathematical Theory

Define an  $n$ -bit voted clock as three clock chains A, B, and C whose bits are labeled from 0 to  $n-1$ , and whose most significant bits,  $A_{n-1}$ ,  $B_{n-1}$ , and  $C_{n-1}$  are voted as in Figure 1. All flip-flops in the clocks are assumed to be falling edge triggered.



Phase shifts are introduced by successive SEUs flipping various bits in the counter chains. The amount of phase shift depends on which bit in the chain is flipped. In order to calculate the probability of anomalous clock operation, the effects of the flipping of the various bits must be quantified. While the behavior of the clocks may seem intuitively obvious, some rigorous proofs clarify the SEU effects and provide a foundation from which the cases producing anomalous behavior can be easily deduced. In the following, the bits of a counter are indicated by  $b_0, \dots, b_{n-1}$ , and  $b^*$  indicates the inverse of  $b$ .

**Theorem 2.1** A flipped bit undergoes a  $180^\circ$  phase shift

**Proof** The flipping of a bit  $b$  can be defined as its SEU induced transition from the state  $b$  to the state  $b^*$ . Since all of the bits are the outputs of falling edge triggered flip-flops, the next state of  $b$  after the next falling edge would be  $b^*$ . The transitions of  $b$  if flipped would be

$$b \rightarrow b^* (\text{SEU}) \rightarrow b (\text{clock edge 1}) \rightarrow b^* (\text{clock edge 2})$$

rather than

$$b \rightarrow b^* (\text{clock edge 1}) \rightarrow b (\text{clock edge 2}).$$

Hence  $b$  is  $180^\circ$  out of its original phase after being flipped.

The  $180^\circ$  phase shift can be considered as an advance in angle, in that the next falling edge will come sooner than it otherwise would, either because the flip causes a falling edge, or because a falling edge (caused by an input clock edge) and a rising edge (caused by the flip) occur in the same input clock cycle. Define a function  $\phi_j(i)$  as the phase shift in bit  $b_j$  induced by a flip in bit  $b_i$ .

**Theorem 2.2**  $\varphi_j(i) = \frac{180^\circ}{2^{j-i}}$  for  $j \geq i$ .

**Proof** For  $j \geq i$ , the frequencies of bits  $b_j$  and  $b_i$  are related by  $f(b_j) = \frac{f(b_i)}{2^{j-i}}$ . The frequency of bit  $b_j$  can be defined as its change of angle  $\theta_j$  per unit time. Then,  $\frac{\Delta\theta_j}{\Delta t} = \frac{\Delta\theta_i}{2^{j-i} \Delta t}$ , or  $\Delta\theta_j = \frac{\Delta\theta_i}{2^{j-i}}$ . Since a flip in bit  $b_i$  causes in it a  $180^\circ$  phase shift, or angle advancement as discussed above, the effect on bit  $b_j$  is  $\varphi_j(i) = \frac{180^\circ}{2^{j-i}}$ .

Recall that each of the counter chains represents an unsigned binary number having a instantaneous decimal value of  $v = \sum_{i=0}^{n-1} b_i 2^i$  where  $b_i \in \{0,1\}$ , and has a maximum possible value of  $2^n - 1$ .

**Theorem 2.3** A flip in bit  $b_i$  is equivalent to adding  $2^i$  to the value of the counter.

**Proof** If the flip changes  $b_i$  from 0 to 1, then the effect on the counter's value can be seen by inspection of the above equation for  $v$ . For the falling transition, note that a 1 to 0 transition on bit  $b_i$  can be forced by clock-independent binary addition of the current counter bits as a binary number and the binary number in which all bits are 0 except for bit  $i$ , which has decimal value  $2^i$ .

**Theorem 2.4** Phase shifts are additive and commutative, i.e.,  $\varphi_j(i_1, i_2) = \varphi_j(i_1) + \varphi_j(i_2)$ , and  $\varphi_j(i_1, i_2) = \varphi_j(i_2, i_1)$ .

**Proof** Since bit flips are equivalent to addition, these follow trivially from the associative and commutative laws of addition.

### 3. Calculating the Probabilities of Anomalous Operation

In many cases, divide chain counters are reset only by POR (power-on reset), meaning that the effects of bit flips could last for several years. For this reason, the probabilities calculated in this section are shown for a period of from 0.1 to 16 years. The formulas derived herein can be used to calculate counter reliability for any time period.

#### 3.1 Clock Rate Error

Examination of Figure 3 shows that there is no time during which all of the clock bits are simultaneously high. The phase relationships by which rate error is produced are seen to be:

- (1)  $0 < \Phi(\text{An-1}, \text{Bn-1}) < 180^\circ$
  - (2)  $180^\circ < \Phi(\text{An-1}, \text{Cn-1}) < \Phi(\text{An-1}, \text{Bn-1}) + 180^\circ$
- where  $\Phi(\text{An-1}, \text{Bn-1})$  is the phase difference between clock bits An-1 and Bn-1.

The sequences of SEUs that will produce anomalous operation can be easily deduced from the above theory, and it will be shown that 3 SEUs are required to produce this effect. Phase relationship (1) states that  $0 < \Phi(\text{An-1}, \text{Bn-1}) < 180^\circ$ . A flip in the MSB of a counter, bit n-1, causes a  $180^\circ$  phase shift, so a flip in any lower bit  $B_i$ ,  $0 \leq i \leq n-2$ , in counter B will cause it to have a phase shift of less than  $180^\circ$  with respect to A. Phase relationship (2) states that  $180^\circ < \Phi(\text{An-1}, \text{Cn-1}) < \Phi(\text{An-1}, \text{Bn-1}) + 180^\circ$ . This will be effected by a flip in bit Cn-1 and a flip in bit Cj for  $0 \leq j < n-2$ . No flips are required in counter A. From the above, it is seen that the flips may arrive in any time order and are permanent because the values of the flipped counters are changed (until the counters are reset).

Having determined the combinations of bit flips that will cause anomalous operation, calculating the probability is relatively straight forward. First, we will note that an n-bit voted counter contains  $3n$  bits, so that the number of ways 3 bits can be flipped is  $(3n)^3 = 27n^3$ . This is because there are  $3n$  bits to choose for the first flip, and also  $3n$  bits to choose for the second and third flips, since the same bit could be flipped 3 times.

The number of ways the 3 flips could cause anomalous operation can be calculated by simply listing all the ways and counting them. First, bit Cn-1 must be flipped. Then, if bit B<sub>j</sub> is flipped, bit C<sub>i</sub> must be flipped where  $i < j$ . The possible cases are listed in the table below for a 10 bit counter.

B <sub>j</sub> flipped	Possible C <sub>i</sub> flipped	Possible Ways
8	7,6,5,4,3,2,1, or 0	8
7	6,5,4,3,2,1, or 0	7
6	5,4,3,2,1, or 0	6
5	4,3,2,1, or 0	5
4	3,2,1, or 0	4
3	2,1, or 0	3
2	1 or 0	2
1	0 only	1
Total Number of Ways		36

It can be shown that the total number of ways is equivalent to the sum of the first n-2 digits, the formula for which is  $\frac{(n-2)(n-1)}{2}$ . There are 6 ways the counters A, B, and C could be chosen so that one is not flipped, one is flipped once, and one is flipped twice. Thus the total number of ways the anomalous configuration of flips could be had is

36\*6=216 for the 10 bit counter, or 3(n-2)(n-1) for the general case. Finally, the probability of having 3 flips that produce anomalous operation is

$$P_{rate} = \frac{3(n-2)(n-1)}{27n^3} = \frac{(n-2)(n-1)}{9n^3}$$

Let  $\lambda$  represent the SEU rate in errors per bit day, and assume  $\lambda = 1E-6$ . Bit flips can be considered to follow an exponential distribution because the rate does not vary with the age of the parts. Therefore, the reliability of a given bit, i.e., the probability of it not flipping over a specified period of time  $t$ , is given by  $R=e^{-\lambda t}$ . For an  $n$  bit voted counter, the reliability is  $R^{3n}=e^{-3n\lambda t}$ , and the probability of having a flip is  $P_f=1-R^{3n}$ . The probability of having 3 flips is  $P_f^3$ . Given this, an equation can be written to give the reliability  $R_{rate}$  of a counter relative to clock rate error for a given  $\lambda$ ,  $t$ , and  $n$ :

$$R_{rate} = 1 - P_{rate} P_f^3 = 1 - P_{rate} (1 - R^{3n})^3 = 1 - \frac{(n-2)(n-1)(1 - e^{-3n\lambda t})^3}{9n^3}.$$

The curves shown in the following figures show the reliability versus time in years. The reliability is graphed as  $-\log(-\ln(R))$  which is related to  $R$  as shown in the following table.

R	$-\log(-\ln(R))$	R	$-\log(-\ln(R))$
0.9000000000	0.98	0.9999990000	6.00
0.9900000000	2.00	0.9999990000	7.00
0.9990000000	3.00	0.9999999000	8.00
0.9999000000	4.00	0.9999999900	9.00
0.9999900000	5.00	0.9999999999	10.00

Thus the value graphed very nearly gives the number of “9s” in the reliability number. The value of  $R$  for a given value  $y$  read from the graph can be found by the inverse function  $R = \exp(-10^{-y})$ . Figure 6 shows curves of  $R_{rate}$  for  $n=3$  and  $10$  for  $\lambda=1E-6$ .

### 3.2 Double-Flip Glitching

Figure 4 shows how clock glitches could be created by 2 bit flips. One clock chain must be shifted  $180^\circ$  with respect to one other, and the third clock must be shifted by between more than  $0^\circ$  to less than  $180^\circ$  with respect to the unshifted clock. From the above theory, we can deduce that if clock A is not flipped, clock B has its MSB flipped, and clock C has any bit other than its MSB flipped, the criteria will be satisfied. For a particular choice of clocks A, B, and C, there are  $n-2$  ways that this can be done: bit  $B_{n-1}$  must be flipped, and any of bits  $C_0$  to  $C_{n-2}$  may be flipped. There are 6 ways that clocks A, B, and C can be chosen, giving a total of  $6(n-2)$  ways that the bits could be flipped.

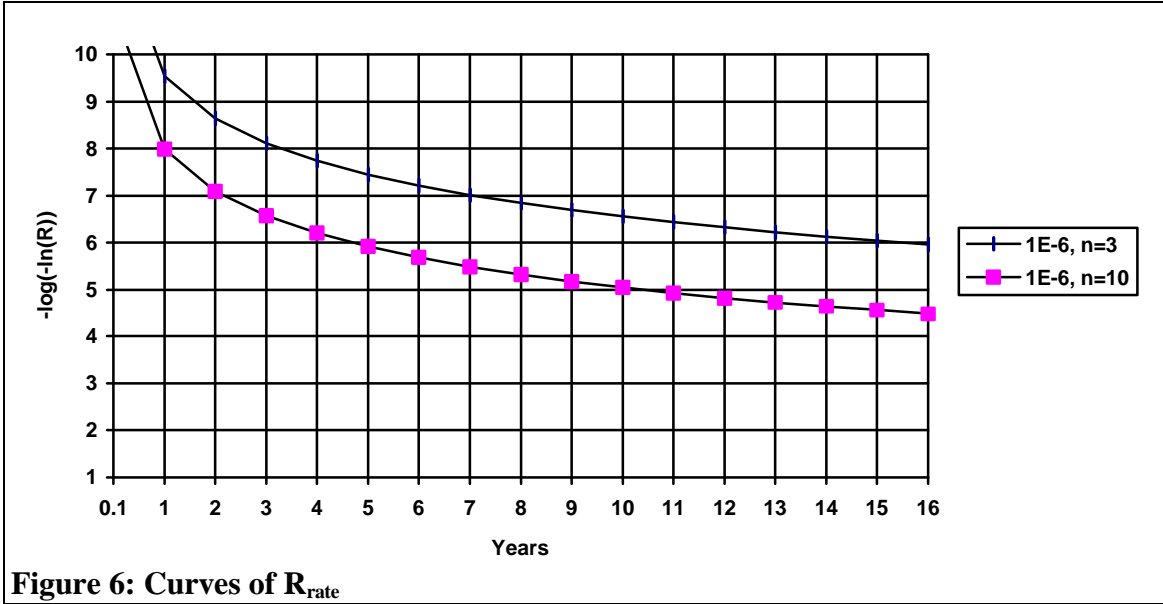


Figure 6: Curves of R<sub>rate</sub>

The number of ways that 2 flips can be had in the counter is  $(3n)^2$ , so the probability that 2 flips will cause glitching is  $P_{\text{glitch}2} = \frac{6(n-2)}{9n^2}$ . The probability  $P_f$  of bit

flips was given above, from which the reliability  $R_{\text{glitch}2}$  of the counter relative to double bit glitching is given by

$$R_{\text{glitch}2} = 1 - P_{\text{glitch}2} P_f^2 = 1 - \frac{2(n-2)(1 - e^{-3n\lambda t})^2}{3n^2}$$

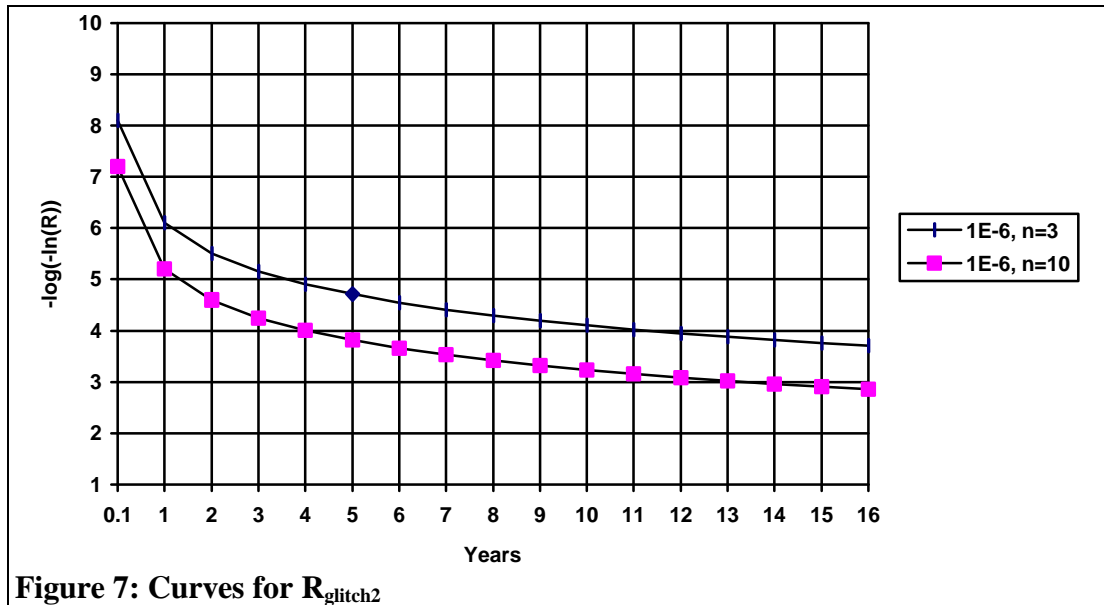


Figure 7: Curves for R<sub>glitch2</sub>

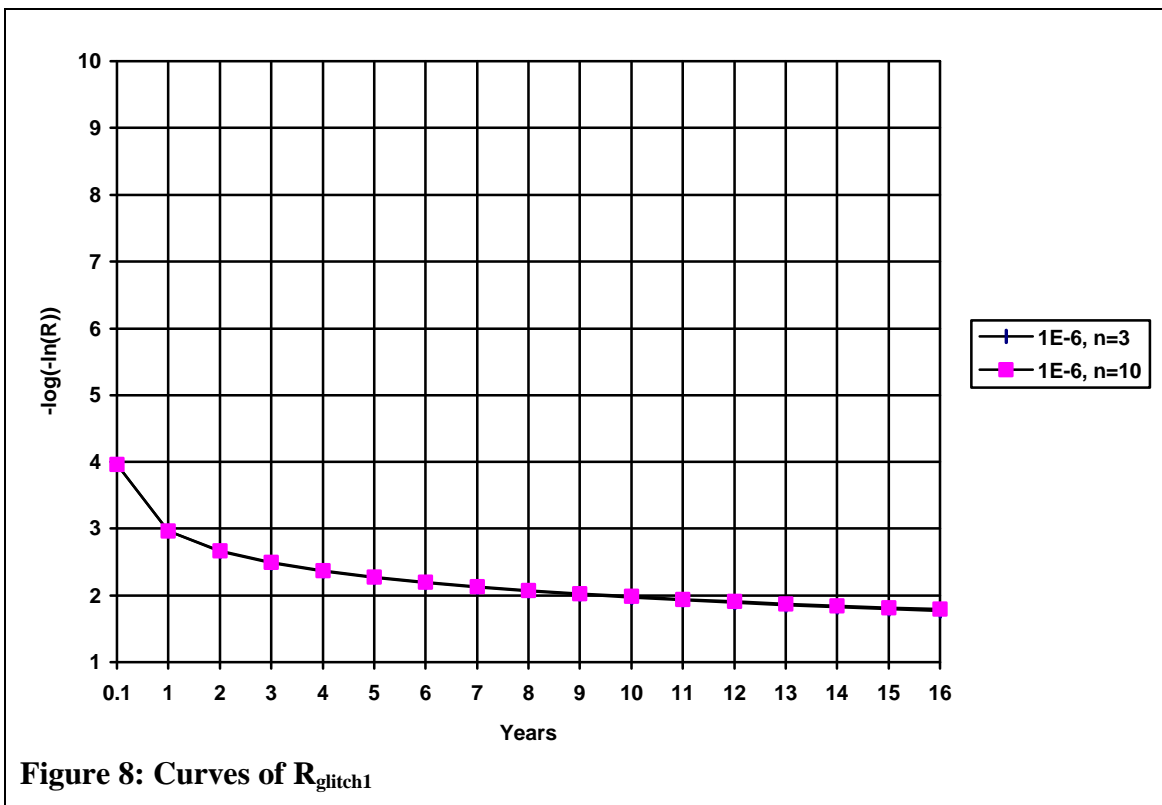
The curves for  $R_{\text{glitch}2}$  are shown in Figure 7.

### 3.3 Single-Flip Glitching

Single bit glitching requires that the MSB of one counter chain be flipped. There are 3 ways that this can happen, and the total number of possible single bit flips is  $3n$ , so the probability  $P_{\text{glitch}1}$  of single bit glitching is  $P_{\text{glitch}2} = \frac{3}{3n} = \frac{1}{n}$ . The reliability of a counter relative to single bit glitching is given by

$$R_{\text{glitch}1} = 1 - P_{\text{glitch}1} P_f = 1 - \frac{1 - e^{-3n\lambda t}}{n}$$

It can be argued that single-flip glitching is less probable than double-flip glitching because in the former case two clock MSBs are in phase, so that there will always be two edges rising or falling in opposition to the one that is  $180^\circ$  out of phase. Still, the potential for glitches depends on the relative timing of the individual bits. Curves of  $R_{\text{glitch}1}$  are shown in Figure 8.



### 3.4 Double-Flip Phase Shifting

A single bit flip in a voted counter on any bit other than the MSB will have no effect on its operation, as the phase shift induced will be overridden by the vote of the unflipped chains. Two bit flips, however, can induce shifts in the phase of the output (Figure 2). The criticality of this depends on the circuitry which the clock drives.

Output phase shifts will be induced if one chain is unflipped while each of the other two are flipped so as to have unequal phase shifts. The number of ways an n-bit counter chain can be flipped in other than the MSB is n-1. There are thus n-2 ways the third chain can be flipped with an unequal phase shift, since the same numbered bit cannot be chosen in both chains. Since there are 6 ways the flipped counters can be chosen, the total number of bit flips inducing output phase shifts is 6(n-2)(n-1). There are (3n)<sup>2</sup> possible two bit flips, giving the probability of having two bit flips inducing output phase shifts

being  $P_{\text{phase}} = \frac{2(n-2)(n-1)}{3n^2}$ . The reliability of a counter with respect to phase shifts is

thus  $R_{\text{phase}} = 1 - P_{\text{phase}} P_f^2 = 1 - \frac{2(n-2)(n-1)(1 - e^{-3n\lambda t})^2}{3n^2}$ . Curves of  $R_{\text{phase}}$  are shown in

Figure 9.

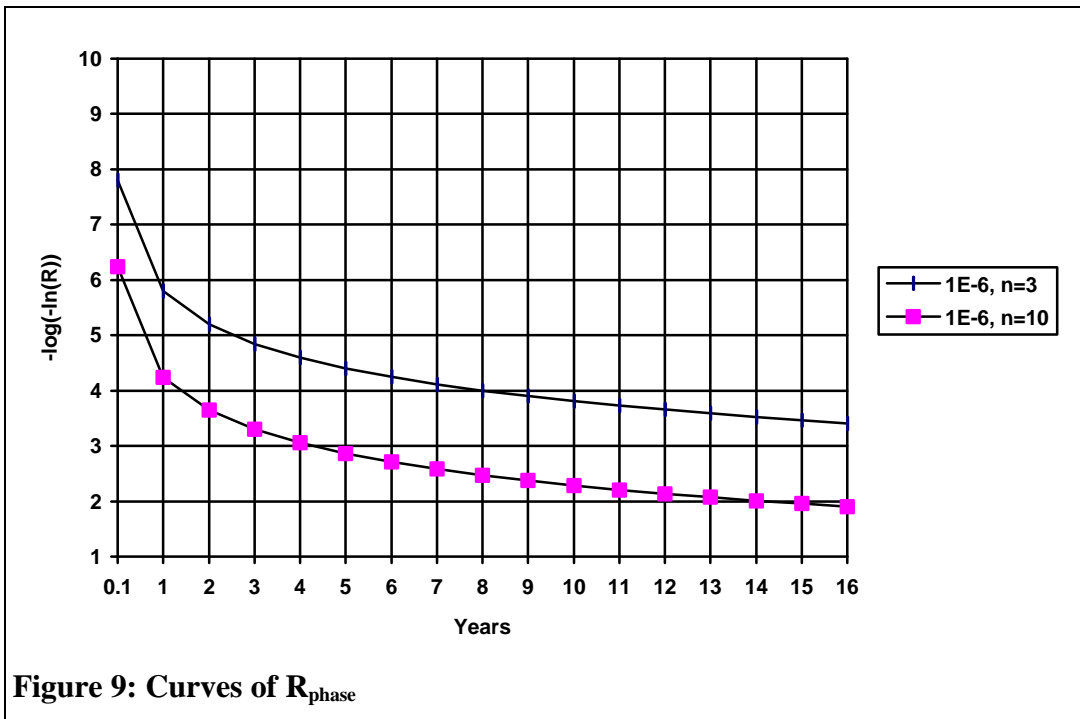
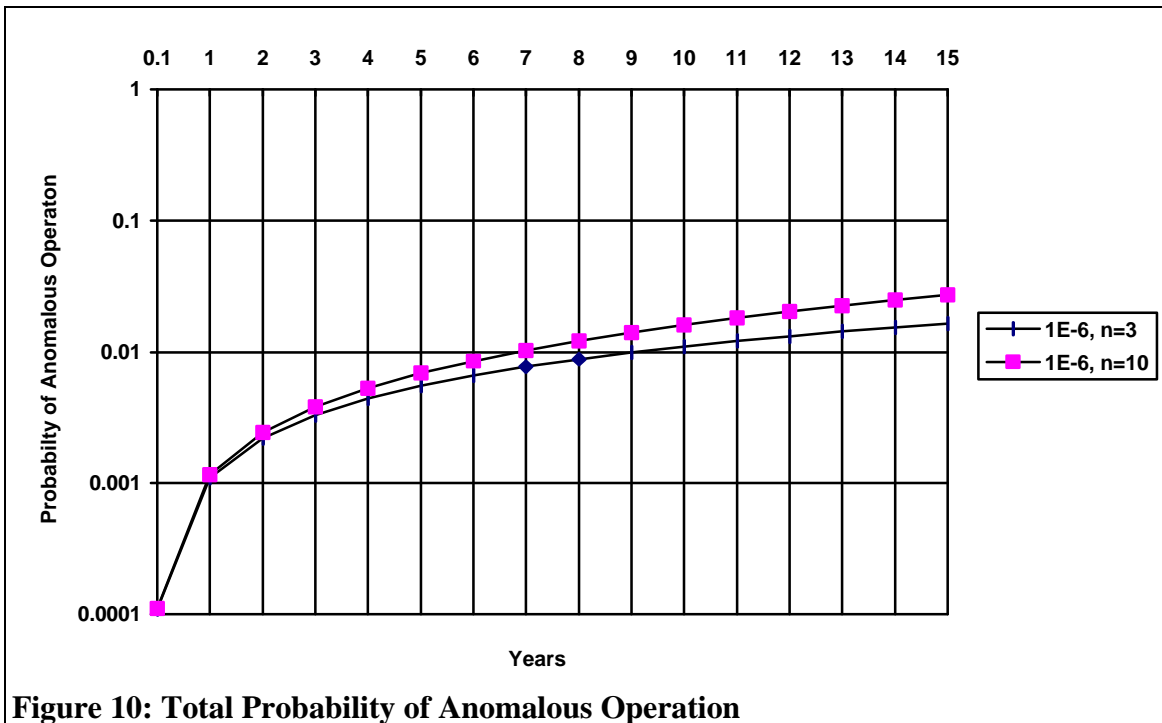


Figure 9: Curves of  $R_{\text{phase}}$

### 3.5 Total Counter Reliability

Allowing that the 4 types of anomalous operation discussed above are mutually exclusive, the total reliability of the counter relative to such anomalies is the product of the

individual reliabilities. Curves of the total reliability are shown in Figure 10, in terms of the probability of anomalous operation.



It is important to note that we have calculated reliabilities based on the minimum number of bit flips that can produce a given effect. Although larger numbers of flips are less probable, the effect is to make the numbers calculated here to be upper bounds of reliability for the counters.

#### 4. Conclusion

This paper has presented the theory behind and methods of calculating the probability of various types of anomalous operation that could be exhibited by voted ripple counters. It is observed that the combined probability of anomalous operation is fairly high, as seen in Figure 10. Anomalous behavior of such counters can be avoided by limiting the time period they are allowed to run without being reset. The time period chosen would depend on the SEU susceptibility of the individual flip-flops, the system effects resulting from the various types of anomalous behavior, and the SEU immunity requirements of the mission.