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Reliability Analysis of Programmed UTMC Amorphous Silicon Antifuse PROMs Following Post-Program Conditioning

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Abstract

Life test data were obtained on UTMC Microelectronic Systems 64K and 256K programmable read-only memories (PROMs) following post-program conditioning (PPC). PPC is used to enhance the reliability (and radiation tolerance) of the UTMC PROMs following programming. To date, temperature-only life-test data show a mean time to failure (MTTF) for the 64K PROM of 3,442 years and a MTTF of 860 years for the 256K PROM (using a 60% confidence limit at 55°C).

Introduction

The UTMC Microelectronic Systems (UTMC) 64K and 256K programmable read-only memories (PROM) use an amorphous silicon (α-Si) based antifuse. In the unprogrammed state the antifuse has a high resistance, typically $>10^9\Omega$. Following programming with a series of voltage pulses, a low resistance filament is created. The PROMs each use a 2-transistor/2-antifuse structure for each cell. Following programming, each cell has one programmed (low-resistance) antifuse and one unprogrammed (high-resistance) antifuse. For reliable operation, therefore, the programmed antifuse must stay in a low resistance state and the unprogrammed antifuse must stay in a high resistance state for the life of the product.

The reliability of the unprogrammed antifuse structures were determined through a design of experiments (DOE) approach which used accelerated voltage stressing to calculate a failure rate [1]. To determine the reliability of the programmed antifuse a thermally activated test method was used. PROMs were programmed with an “AA55” pattern (considered a worst case test pattern for these devices), conditioned with 64 hours of unbiased bake followed by 64 hours of voltage stressing. The combination of unbiased bake and voltage stressing following programming is called post-programming conditioning (PPC). The conditioned PROMs were then subjected to an extended life test at 150°C with a 5.5V dynamic stress pattern.

To date, a total of 391 programmed PROMs have been placed under life-test (185 256K PROMs and 181 64K PROMs), from 7 different lots of material. The details of the PPC followed by the life-test results are discussed below.

Post-Programming Conditioning

PPC was developed and implemented by UTMC to ensure a higher reliability one-time programmable device. PPC also ensures that these PROMs will survive a full 1Mrad(Si) of total ionizing dose [2].

The UTMC PPC is a two step procedure, which consists of an unbiased bake followed by a dynamic voltage stress. The unbiased bake is used to anneal any α-Si that was damaged during programming. Through several experiments, we found that 64hrs of unbiased bake at 200°C was sufficient to return the α-Si damaged by pulsed voltage stressing (simulating programming pulses) back to a sufficiently high resistance state (within a few percent of the original antifuse resistance). Our annealing results for the α-Si are consistent with results found by Wong and Gordon [3] where they determined a 0.8eV thermal activation energy for the anneal. Based on the estimated 0.8eV thermal activation energy, table 1 can be used to find the time to anneal programming damage for various temperatures.

Once the programming damage is removed from the α-Si, a dynamic voltage stress is applied to force a maximum amount of current through the programmed (or partially programmed) antifuse. Note that the α-Si is annealed prior to conditioning so that the current is forced to flow almost entirely through the programmed fuse (since the programmed fuse is surrounded by high-resistance α-Si and not lower resistance damaged α-Si). The current flowing through the programmed antifuse during the dynamic voltage stressing portion of the PPC contributes to the final formation of the programmed fuse and leads to a dramatic increase in the final reliability. The final reliability of the programmed fuse is related to the ratio of programming current (I_p) to the use or stress current (I_s), i.e., the time-to-failure of the programmed fuse is proportional to I_s/I_p [4,5]. Tables 2 and 3 show the voltages and frequencies, and figure 1 shows the waveforms applied to each pin for the dynamic voltage-stressing portion of the PPC.

Table 1. Time to Anneal α-Si as a function of Anneal Temperature

Bake Temperature	Time for 64-Hour 200 °C Equivalent Anneal (Hours)
175.0	191.4
177.5	170.6
180.0	152.3
182.5	136.1
185.0	121.8
187.5	109.1
190.0	97.8
192.5	87.8
195.0	79.0
197.5	71.1
200.0	64.0

Table 2. Post-Programming Burn-In Conditions

V_{DD}	7.0V
Temperature	150 °C
Time	64 Hours

Table 3. Signals applied to each pin during post-programming dynamic voltage stressing. Note that for the 64K PROM pin 1 (A14) and pin 26 (A13) are not connected.

Pin Number	Signal Name	Burn-In Pattern	Pin Number	Signal Name	Burn-In Pattern
1	A14	12.2HZ	15	DQ3	6.1HZ
2	A12	48.8HZ	16	DQ4	6.1HZ
3	A7	1.56KHZ	17	DQ5	6.1HZ
4	A6	3.13KHZ	18	DQ6	6.1HZ
5	A5	6.25KHZ	19	DQ7	6.1HZ
6	A4	12.5KHZ	20	CEB	GND
7	A3	25KHZ	21	A10	195HZ
8	A2	50KHZ	22	OEB	VDD
9	A1	100KHZ	23	A11	97.7HZ
10	A0	200KHZ	24	A9	391HZ
11	DQ0	6.1HZ	25	A8	781HZ
12	DQ1	6.1HZ	26	A13	24.4HZ
13	DQ2	6.1HZ	27	PEB	400KHZ
14	VSS	GND	28	VDD	VDD

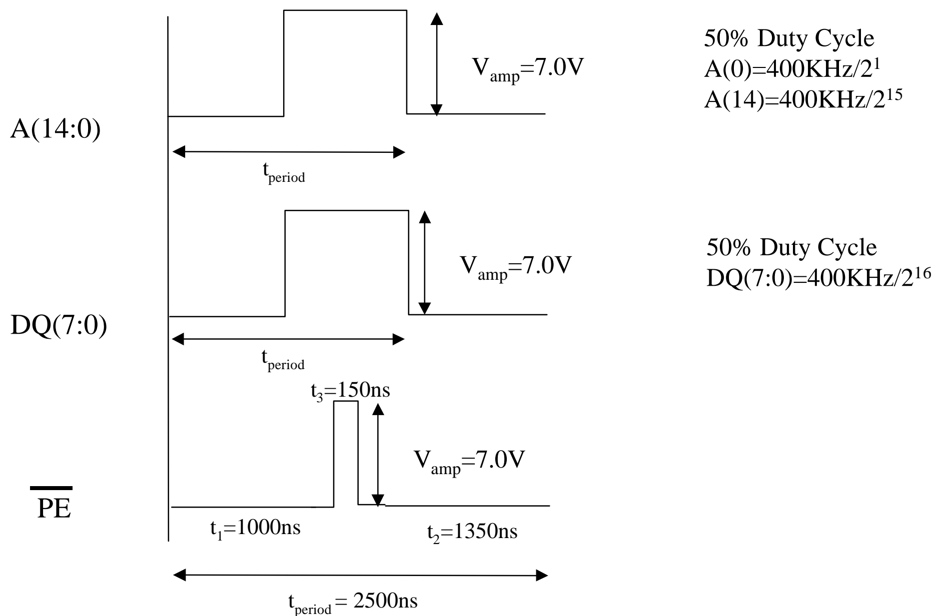

Figure 1. Dynamic burn-in timing.

Life-Test Results

The life-test was performed with a dynamic voltage-stressing pattern that continually read the contents of the memory, similar to actual worst-case use conditions. The life-test was performed at 150°C with 5.5V applied to V_{dd}. Table 4 summarizes the results of the life-test.

The first column of table 4 shows the part tested (64K vs. 256K) and the assembly designation. The second column shows the lot from which the material was obtained, and the third column shows the total number of parts in that particular life test segment. The 4th column shows the total number of hours of life-test stressing, while the 5th column shows the total cumulative number of hours the PROMs have received. The 6th column shows the total number of stressing hours (number of units multiplied by the total stressing time) at 55°C (using a 0.4eV thermal activation energy).

The 7th column shows the number of equivalent 64K PROM hours, i.e., a 256K PROM is treated as 4 64K PROMs. The bottom of column 7 shows that the total number of equivalent 64K PROM life-test hours is over 40 million device hours. The 8th column shows the recorded failures and the 9th column gives a brief note as to the cause of the failure.

Table 4. Summary of life-test data for the UTMC PROMs.

Test Units (w/ PPC II)	Lot Number	Units	Life Test Hours at 150C	Cummulative Life Test Hours at 150C	Device Hours (55C equivalent)	64K PROM Device Hours (Equivalent)	Bit Failures	Comments
64K PROM (WO7430)	QS52561	114	500.9	500	11968.74	1.36E+06	0	
64K PROM (WO7430)	QS52561	114	562.2	1063.1	13433.47	1.53E+06	0	
64K PROM (WO7430)	QS52561	136	504.1	1567.2	12045.20	1.64E+06	0	
64K PROM (WO7430)	QS52561	136	516.7	2083.9	12346.27	1.68E+06	0	
64K PROM (WO7430)	QS52561	136	1024.4	3108.3	24477.49	3.33E+06	1	*bin 14, noisy outputs, unrelated to antifuse
256K PROM (0NYD)	AS20605 AS20606 AS22622	161	258.1	258.1	6167.16	3.97E+06	0	
256K PROM (0NYD)	AS20605 AS20606 AS22622	161	279.8	537.9	6685.67	4.31E+06	0	
256K PROM (0NYD)	AS20605 AS20606 AS22622	138	518.1	1056	12379.72	6.83E+06	1	*bin12, antifuse failure
256K PROM (0NYD)	AS20605 AS20606 AS22622	160	690.9	1746.9	16508.68	1.06E+07	0	
256K PROM (0NYD)	AS20605 AS20606 AS22622	160	211.8	1958.7	5060.85	3.24E+06	0	
64K PROM (0NVXCGPC)	AS13627	23	500.2	500.2	11952.01	2.75E+05	0	
64K PROM (0NHK)	AS13627	22	584.3	584.3	13961.54	3.07E+05	0	
256K PROM (0NVPRS)	AS19696 AS22633	24	501.8	501.8	11990.24	1.15E+06	0	
256K PROM (0NYD)	AS20605 AS20606 AS22622	166	3371.8	6916.8	80567.35	5.35E+07	0	
Total					**239544.39**	**9.37E+07**	**2**	

Calculating Failure Rates

We can calculate the maximum likelihood estimator (MLE) mean-time-to-failure (MTTF) for the 64K and 256K PROMs by dividing the total device hours (55°C equivalent) by the total number of failures. To calculate the MTTF at the 60% confidence level we use the chi-square (χ^2) distribution for a time truncated test. Table 5 uses the life-test data shown above in table 4 to calculate the MTTFs and failures-in-time (FITs) for the UTMC PROMs. Note that the FIT rate is determined by dividing $1x10^9$ hours by the respective MTTF (adjusted in hours).

Table 5 MTTF and FIT rates for the UTMC 64K and 256K PROMs (at 55 °C equivalent) based on the life-test data shown in figure 4.

64K PROM MLE MTTF	5,344 years
64K PROM 60% lower confidence limit MTTF	3,442 years
256K PROM MLE MTTF	1,336 years
256KBit PROM 60% lower confidence limit MTTF	860 years
64KBit PROM MLE FIT	21
64KBit PROM 60% upper confidence limit FIT	33
256KBit PROM MLE FIT	85
256KBit PROM 60% upper confidence limit FIT	133

Summary and Conclusions

UTMC developed and implemented a post-programming conditioning procedure for amorphous silicon based antifuses. Life-test data obtained by UTMC show a dramatic increase in the reliability of programmed UTMC 64K and 256K PROMs.

The UTMC PROMS use a 2 transistor/2 antifuse cell. Following programming one antifuse will be at low resistance and the other will remain in its original high resistance state. PPC is necessary to increase the reliability of the programmed antifuse within the cell. As discussed above, the reliability of the programmed antifuse is given by I_p/I_s. In this relatively high-density memory product, I_p is limited by the drive of the transistors tied to the word lines. Although the reliability can't be improved by increasing the ratio of I_p to I_s (without a design change and concomitant loss of density) we were able to successfully increase the reliability of the programmed antifuse by extending the time programming current flows through the antifuses. Since the PPC procedure has been implemented we have observed only a single antifuse related life-test failure in 2.6×10^{12} antifuse hours. Life-test data collection is continuing and updated reliability numbers will be available from UTMC on an ongoing basis

References

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